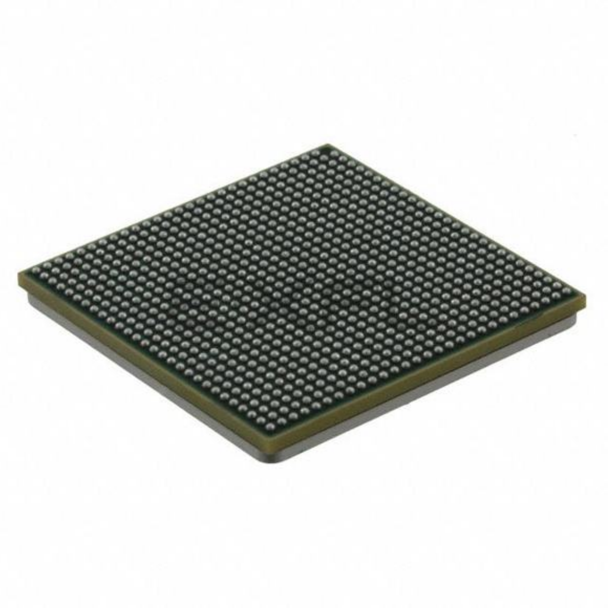
NXP USA Inc. - MPC8548ECPXAQGD Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548ecpxaqgd

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

Table 4. Device Power Dissipation

CCB Frequency[1]	Core Frequency	SLEEP[2]	Typical-65[3]	Typical-105[4]	Maximum[5]	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.
2. SLEEP is based on V_{DD} = 1.1 V, T_j = 65°C.
3. Typical-65 is based on V_{DD} = 1.1 V, T_j = 65°C, running Dhrystone.
4. Typical-105 is based on V_{DD} = 1.1 V, T_j = 105°C, running Dhrystone.
5. Maximum is based on V_{DD} = 1.1 V, T_j = 105°C, running a smoke test.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit
Core and platform PLL lock times	—	100	µs
Local bus PLL lock time	—	50	µs
PCI/PCI-X bus PLL lock time	—	50	µs

5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	—	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.
2. VDD itself is not vulnerable to false ESD triggering; however, as per Section 22.2, “PLL Power Supply Filtering,” the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[*n*]/$\overline{\text{MCK}}$[*n*] crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAS}	1.48 1.95 2.40	— — —	ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHAX}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}$[*n*] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCS}	1.48 1.95 2.40	— — —	ns	3
$\overline{\text{MCS}}$[*n*] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	t_{DDKHCX}	1.48 1.95 2.40	— — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDS}, t_{DDKLDS}	538 700 900	— — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	t_{DDKHDX}, t_{DDKLDX}	538 700 900	— — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 22. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.13	3.47	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	—

Notes:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Figure 11 shows the MII transmit AC timing diagram.

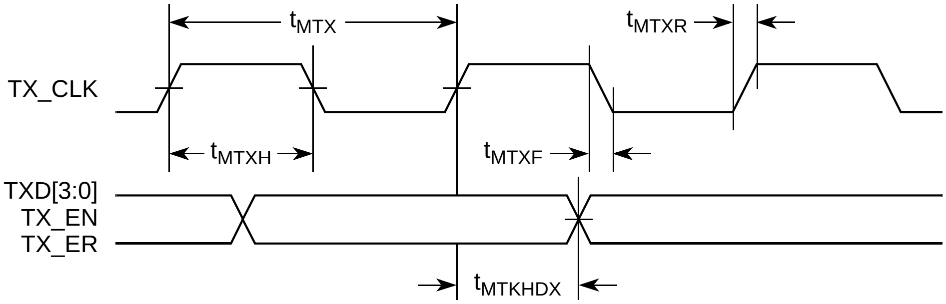

Figure 11. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 29. MII Receive AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%–80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 provides the AC test load for eTSEC.

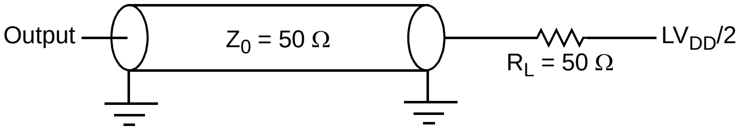

Figure 12. eTSEC AC Test Load

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	–0.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	–0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–3.7	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–3.7	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[*n*]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

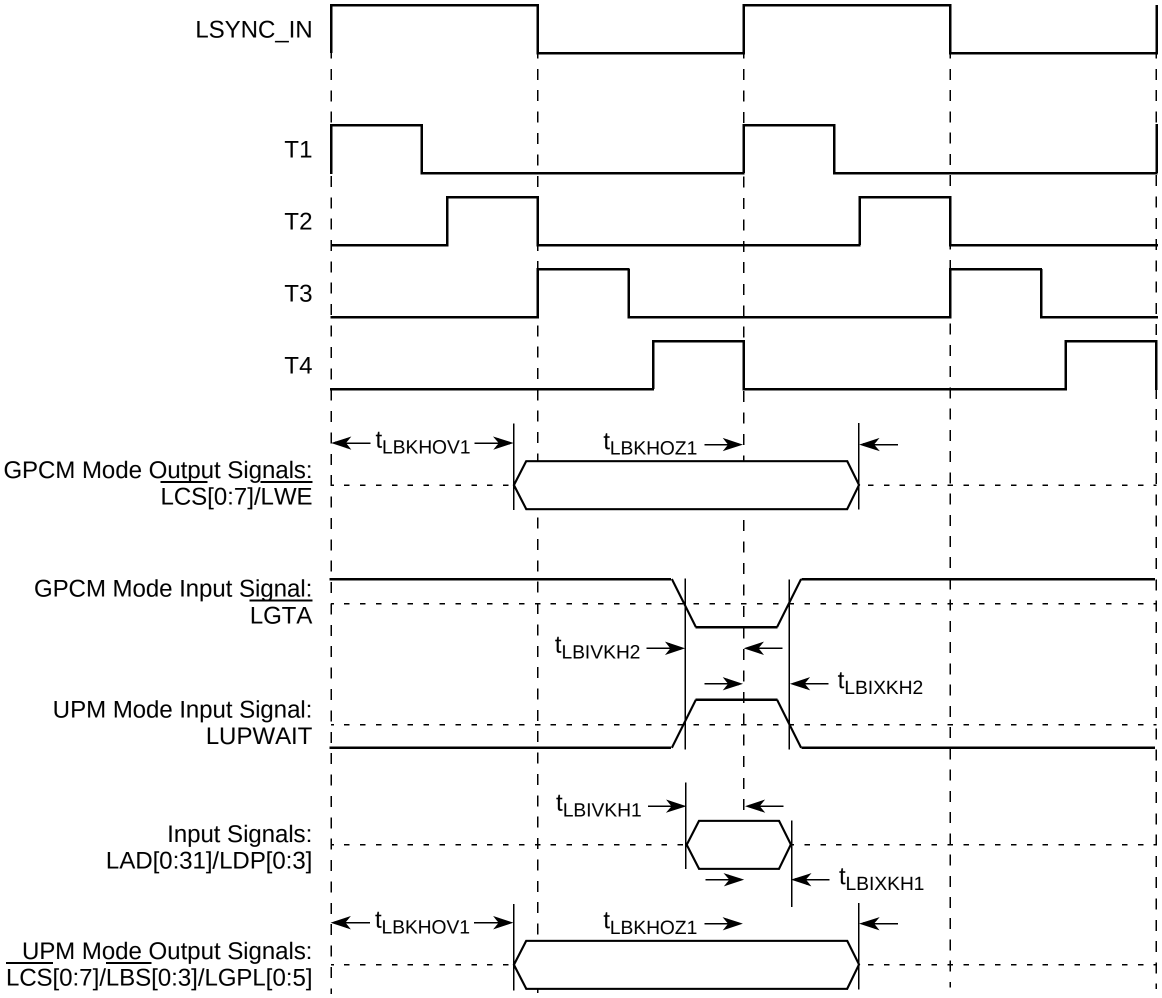

Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Figure 31 provides the $\overline{\text{TRST}}$ timing diagram.

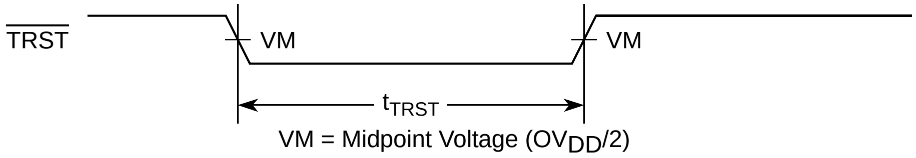

Figure 31. $\overline{\text{TRST}}$ Timing Diagram

Figure 32 provides the boundary-scan timing diagram.

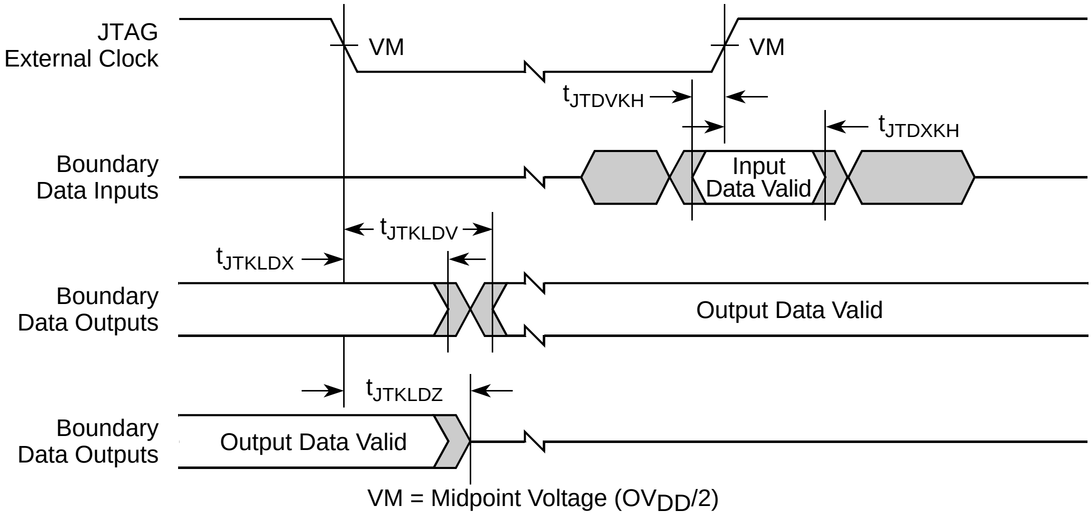

Figure 32. Boundary-Scan Timing Diagram

Figure 34 shows the AC timing diagram for the I^{2}C bus.

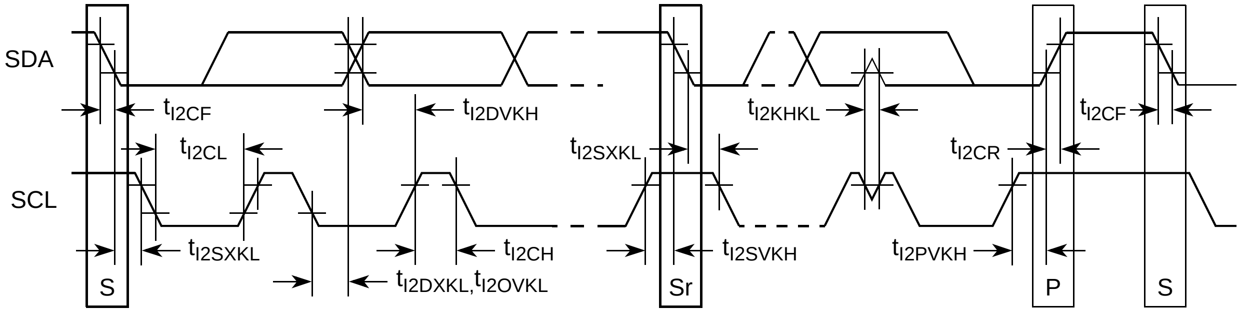

Figure 34. I^{2}C Bus AC Timing Diagram

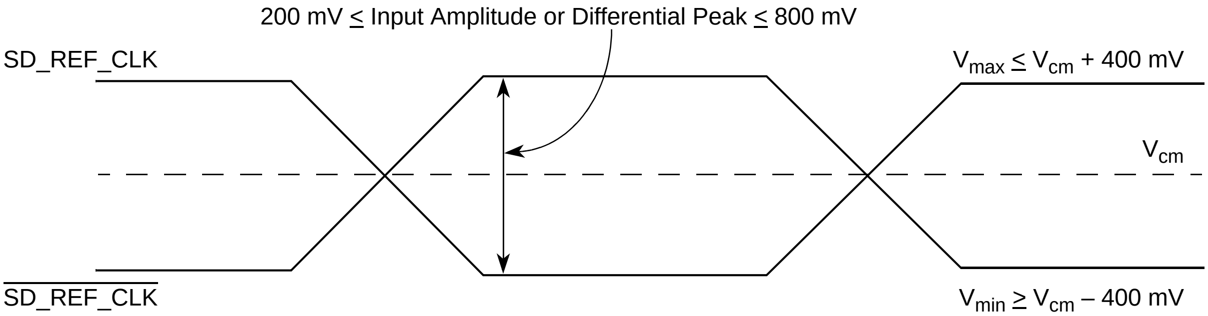

Figure 41. Differential Reference Clock Input DC Requirements (External AC-Coupled)

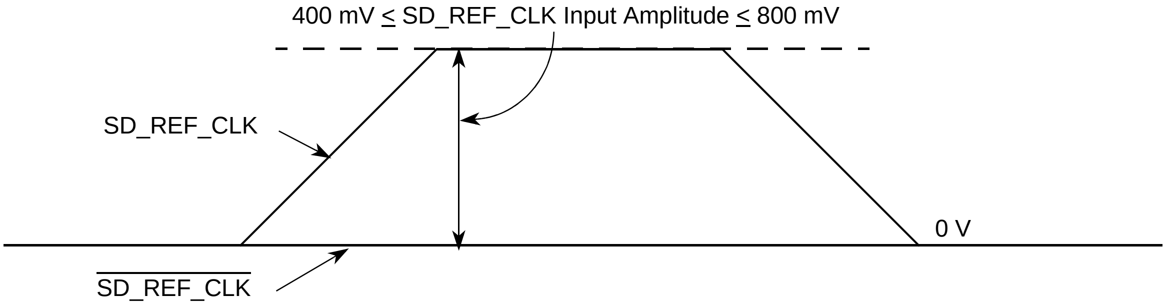

Figure 42. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing with Other Differential Signaling Levels

- With on-chip termination to SGND_SRDSn (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 43 through Figure 46 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the SerDes reference clock receiver requirement provided in this document.

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B volts.
2. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$.
3. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 × (A – B) volts.

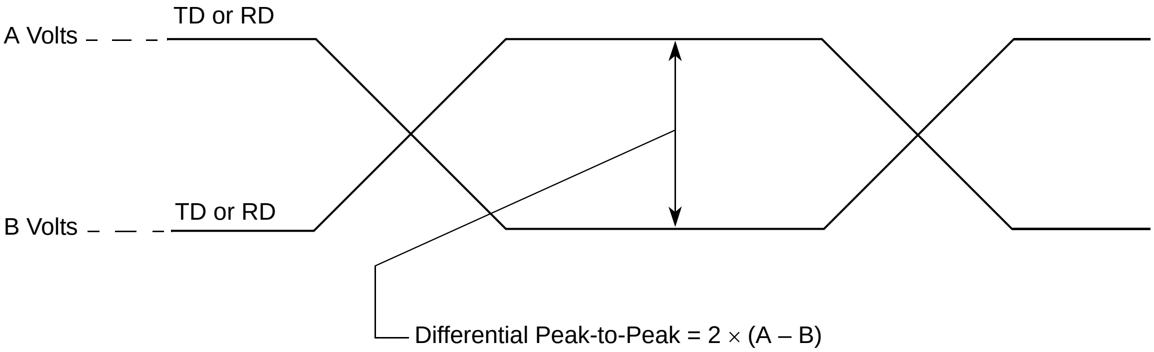

Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mVp-p. The differential output signal ranges between 500 and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
I^{2}C interface				
IIC1_SCL	AG22	I/O	OV_{DD}	4, 27
IIC1_SDA	AG21	I/O	OV_{DD}	4, 27
IIC2_SCL	AG15	I/O	OV_{DD}	4, 27
IIC2_SDA	AG14	I/O	OV_{DD}	4, 27
SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV_{DD}	—
$\overline{\text{SD\_RX}}$[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV_{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	—
$\overline{\text{SD\_TX}}$[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	—
SD_PLL_TPD	U28	O	XV_{DD}	24
SD_REF_CLK	T28	I	XV_{DD}	3
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV_{DD}	3
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV_{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV_{DD}	—
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV_{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV_{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV_{DD}	6, 19, 29
MDVAL	AE5	O	OV_{DD}	6
CLK_OUT	AE21	O	OV_{DD}	11

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_RX	L28	I	200 Ω to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω to GND	—
SD_PLL_TPA	U26	O	—	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74 provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 (One 32-Bit)				
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	—	—	110
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	O	OV_{DD}	—
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV_{DD}	111
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV_{DD}	17
Reserved	AF15, AD14, AE15, AD15	—	—	110
PCI1_C_$\overline{\text{BE}}$[3:0]	AF9, AD11, Y12, Y13	I/O	OV_{DD}	17
Reserved	W15	—	—	110
$\overline{\text{PCI1\_GNT}}$[4:1]	AG6, AE6, AF5, AH5	O	OV_{DD}	5, 9, 35
$\overline{\text{PCI1\_GNT0}}$	AG5	I/O	OV_{DD}	—
$\overline{\text{PCI1\_IRDY}}$	AF11	I/O	OV_{DD}	2
PCI1_PAR	AD12	I/O	OV_{DD}	—
$\overline{\text{PCI1\_PERR}}$	AC12	I/O	OV_{DD}	2
$\overline{\text{PCI1\_SERR}}$	V13	I/O	OV_{DD}	2, 4
$\overline{\text{PCI1\_STOP}}$	W12	I/O	OV_{DD}	2

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{MWE}}$	E7	O	GV_{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV_{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV_{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV_{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV_{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV_{DD}	—
MDIC[0:1]	A19, B19	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV_{DD}	—
LDP[0:3]	K21, C28, B26, B22	I/O	BV_{DD}	—
LA[27]	H21	O	BV_{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	O	BV_{DD}	5, 7, 9
$\overline{\text{LCS}}$[0:4]	J25, C20, J24, G26, A26	O	BV_{DD}	—
$\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$	D23	I/O	BV_{DD}	1
$\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$	G20	O	BV_{DD}	1
$\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$	E21	O	BV_{DD}	1
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/LSDDQM[0]	G25	O	BV_{DD}	5, 9
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/LSDDQM[1]	C23	O	BV_{DD}	5, 9
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/LSDDQM[2]	J21	O	BV_{DD}	5, 9
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/LSDDQM[3]	A24	O	BV_{DD}	5, 9
LALE	H24	O	BV_{DD}	5, 8, 9
LBCTL	G27	O	BV_{DD}	5, 8, 9
LGPL0/LSDA10	F23	O	BV_{DD}	5, 9
LGPL1/$\overline{\text{LSDWE}}$	G22	O	BV_{DD}	5, 9
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	B27	O	BV_{DD}	5, 8, 9
LGPL3/$\overline{\text{LSDCAS}}$	F24	O	BV_{DD}	5, 9
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	H23	I/O	BV_{DD}	—
LGPL5	E26	O	BV_{DD}	5, 9
LCKE	E24	O	BV_{DD}	—
LCLK[0:2]	E23, D24, H22	O	BV_{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV$_{DD}$	—
LSYNC_OUT	F28	O	BV$_{DD}$	—
DMA				
$\overline{\text{DMA\_DACK}}$[0:1]	AD3, AE1	O	OV$_{DD}$	5, 9, 108
$\overline{\text{DMA\_DREQ}}$[0:1]	AD4, AE2	I	OV$_{DD}$	—
$\overline{\text{DMA\_DDONE}}$[0:1]	AD2, AD1	O	OV$_{DD}$	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH16	I	OV$_{DD}$	—
$\overline{\text{MCP}}$	AG19	I	OV$_{DD}$	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV$_{DD}$	—
IRQ[8]	AF19	I	OV$_{DD}$	—
IRQ[9]/$\overline{\text{DMA\_DREQ3}}$	AF21	I	OV$_{DD}$	1
IRQ[10]/$\overline{\text{DMA\_DACK3}}$	AE19	I/O	OV$_{DD}$	1
IRQ[11]/$\overline{\text{DMA\_DDONE3}}$	AD20	I/O	OV$_{DD}$	1
$\overline{\text{IRQ\_OUT}}$	AD18	O	OV$_{DD}$	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV$_{DD}$	5, 9
EC_MDIO	AC8	I/O	OV$_{DD}$	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV$_{DD}$	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV$_{DD}$	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV$_{DD}$	5, 9
TSEC1_COL	R4	I	LV$_{DD}$	—
TSEC1_CRS	V5	I/O	LV$_{DD}$	20
TSEC1_GTX_CLK	U7	O	LV$_{DD}$	—
TSEC1_RX_CLK	U3	I	LV$_{DD}$	—
TSEC1_RX_DV	V2	I	LV$_{DD}$	—
TSEC1_RX_ER	T1	I	LV$_{DD}$	—
TSEC1_TX_CLK	T6	I	LV$_{DD}$	—
TSEC1_TX_EN	U9	O	LV$_{DD}$	30
TSEC1_TX_ER	T7	O	LV$_{DD}$	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV$_{DD}$	103

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV_{DD}	—
cfg_dram_type0/GPOUT6	R8	O	LV_{DD}	5, 9
GPOUT7	N6	O	LV_{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV_{DD}	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV_{DD}	15
cfg_dram_type1	R10	O	LV_{DD}	5, 9
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV_{DD}	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV_{DD}	—
TSEC3_GTX_CLK	W8	O	TV_{DD}	—
TSEC3_RX_CLK	W2	I	TV_{DD}	—
TSEC3_RX_DV	W1	I	TV_{DD}	—
TSEC3_RX_ER	Y2	I	TV_{DD}	—
TSEC3_TX_CLK	V10	I	TV_{DD}	—
TSEC3_TX_EN	V9	O	TV_{DD}	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV_{DD}	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV_{DD}	—
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV_{DD}	—
TSEC3_CRS	AA3	I/O	TV_{DD}	31
TSEC3_TX_ER	AB6	O	TV_{DD}	—
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV_{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV_{DD}	—
UART_SOUT[0:1]	AB7, AD8	O	OV_{DD}	—
I^2C interface				
IIC1_SCL	AG22	I/O	OV_{DD}	4, 27

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200 Ω (±1%) to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω (±1%) to GND	—
SD_PLL_TPA	U26	O	AVDD_SRDS	24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

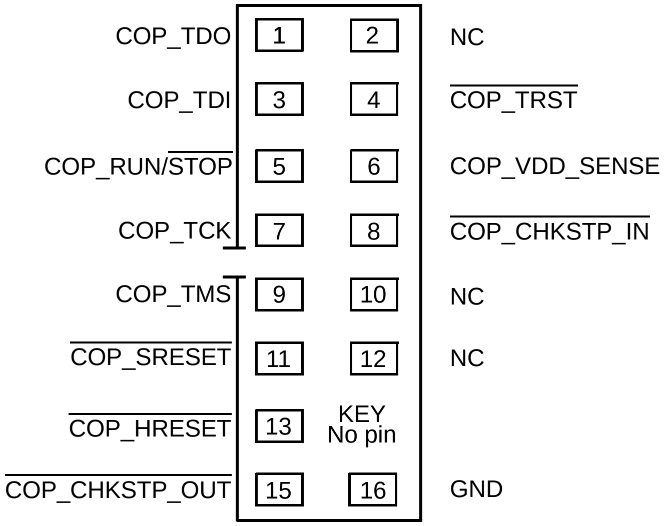

Figure 62. COP Connector Physical Pinout

- $\overline{\text{SD\_REF\_CLK}}$

NOTE

> It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (this prevents the oscillations and holds the receiver output in a fixed state) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD}. Pins V27 and M25 must be tied to GND through a 300-Ω resistor.

22.11 Guideline for PCI Interface Termination

PCI termination if PCI 1 or PCI 2 is not used at all.

Option 1

If PCI arbiter is enabled during POR:

- All AD pins are driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

If PCI arbiter is disabled during POR:

- All AD pins are in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-kΩ resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

22.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following is the termination recommendation:

- For LDP[0:3]—tie them to ground or the power supply rail via a 4.7-kΩ resistor.
- For LPBSE—tie it to the power supply rail via a 4.7-kΩ resistor (pull-up resistor).