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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

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Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8548ecpxaujb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

Power Characteristics

Power Characteristics 3

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Table 4. Device Power Dissipation

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.

2. SLEEP is based on V_{DD} = 1.1 V, T_i = 65°C.

3. Typical-65 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 65^{\circ}\text{C}$, running Dhrystone. 4. Typical-105 is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running Dhrystone. 5. Maximum is based on $V_{DD} = 1.1 \text{ V}$, $T_j = 105^{\circ}\text{C}$, running a smoke test.

4.3 eTSEC Gigabit Reference Clock Timing

The following table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the device.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
EC_GTX_CLK125 frequency	f _{G125}	—	125	—	MHz	
EC_GTX_CLK125 cycle time	t _{G125}	—	8	—	ns	
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t _{G125R} , t _{G125F}	_	_	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t _{G125H} /t _{G125}	45 47	_	55 53	%	2, 3

Table 6. EC_	GTX_CLK125	AC Timing	Specifications
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Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TV_{DD} = 2.5 V, and from 0.6 and 2.7 V for L/TV_{DD} = 3.3 V.

- 2. Timing is guaranteed by design and characterization.
- 3. EC_GTX_CLK125 is used to generate the GTX clock TSEC*n*_GTX_CLK for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-x controller is not the SYSCLK input, but instead the PCIn_CLK. The following table provides the PCI/PCI-X reference clock AC timing specifications for the device.

	Table 7.	PCIn_	CLK AC	Timing	S	pecifications
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At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
PCIn_CLK frequency	f _{PCICLK}	16	_	133	MHz	—
PCIn_CLK cycle time	t _{PCICLK}	7.5	_	60	ns	—
PCIn_CLK rise and fall time	t _{PCIKH} , t _{PCIKL}	0.6	1.0	2.1	ns	1, 2
PCIn_CLK duty cycle	t _{PCIKHKL} /t _{PCICLK}	40		60	%	2

Notes:

1. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.

2. Timing is guaranteed by design and characterization.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V
AC input high voltage	V _{IH}	MV _{REF} + 0.25	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC 533 MHz 400 MHz 333 MHz	^t ciskew	-300 -365 -390	300 365 390	ps	1, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

 The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} = ± (T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.



Figure 7. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 26.	GMII	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
GMII data TXD[7:0], TX_ER, TX_EN setup time	t _{GTKHDV}	2.5	_	_	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX}	0.5	_	5.0	ns
GTX_CLK data clock rise time (20%–80%)	t _{GTXR} ²	_	_	1.0	ns
GTX_CLK data clock fall time (80%–20%)	t _{GTXF} 2	—		1.0	ns

Notes:

The symbols used for timing specifications follow the pattern t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

2. Guaranteed by design.

A timing diagram for TBI receive appears in Figure 16.



Figure 16. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
Data to clock output skew (at transmitter)	t _{SKRGT} 5	-500 ⁶	0	500 ⁶	ps
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0	_	2.8	ns
Clock period ³	t _{RGT} 5	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 4}	t _{RGTH} /t _{RGT} 5	45	50	55	%
Rise time (20%–80%)	t _{RGTR} 5	_	_	0.75	ns
Fall time (20%–80%)	t _{RGTF} 5		—	0.75	ns

Table 33. RGMII and RTBI AC Timing Specifications

Notes:

 In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

5. Guaranteed by characterization.

6. In rev 1.0 silicon, due to errata, t_{SKRGT} is -650 ps (min) and 650 ps (max). See "eTSEC 10" in the device errata document.

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Figure 19 provides the AC test load for eTSEC.



Figure 19. eTSEC AC Test Load

Figure 20 shows the RMII receive AC timing diagram.



Figure 20. RMII Receive AC Timing Diagram

11 Programmable Interrupt Controller

In IRQ edge trigger mode, when an external interrupt signal is asserted (according to the programmed polarity), it must remain the assertion for at least 3 system clocks (SYSCLK periods).

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the JTAG interface.

Parameter	Symbol ¹	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($V_{IN}^{1} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V
Low-level output voltage (OV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	—	0.4	V

 Table 43. JTAG DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} in this case, represents the OV_{IN}

12.2 JTAG AC Electrical Specifications

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 32.

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	_
JTAG external clock cycle time	t _{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	6
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 0	_	ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	20 25		ns	4

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹

Table 53. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 11

Notes:

- 1. See the timing measurement conditions in the PCI-X 1.0a Specification.
- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
- 8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI-X 1.0a Specification.

10.Guaranteed by characterization.

11.Guaranteed by design.

This table provides the PCI-X AC timing specifications at 133 MHz. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV		3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7	_	ns	1, 11
SYSCLK to output high impedance	t _{PCKHOZ}		7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t _{PCIVKH}	1.2	_	ns	3, 5, 9, 11
Input hold time from SYSCLK	t _{PCIXKH}	0.5	_	ns	11
REQ64 to HRESET setup time	t _{PCRVRH}	10	_	clocks	12
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	12
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	10, 12
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10	_	clocks	12

Table 54. PCI-X AC Timing Specifications at 133 MHz

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD}_TX} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.



To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and SD_REF_CLK for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

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- The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.
- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
 - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with SD_REF_CLK either left unconnected or tied to ground.
 - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DCor AC-coupled into the unused phase (SD_REF_CLK) through the same source impedance as the clock input (SD_REF_CLK) in use.



Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

Table 57. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
L _{TX-SKEW}	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 50 must be used as the RX device when taking measurements (also see the receiver compliance eye diagram shown in Figure 49). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to $-{300 \text{ mV}}$ and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see Figure 50). Note: that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode Impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 50) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer must provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 49) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and \overline{TD}) or a receiver input (RD and \overline{RD}). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- 1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of A B volts.
- 2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{TD} V_{\overline{TD}}$.
- 3. The differential input signal of the receiver, V_{ID} , is defined as $V_{RD} V_{\overline{RD}}$.
- 4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A B to -(A B) volts.
- 5. The peak value of the differential transmitter output signal and the differential receiver input signal is A B volts.
- 6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A B)$ volts.



Figure 51. Differential Peak–Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long- and short-run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to Serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

18.6 Transmitter Specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than:

- -10 dB for (baud frequency)/10 < Freq(f) < 625 MHz, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \le \text{Freq}(f) \le \text{baud}$ frequency

The reference impedance for the differential return loss measurements is $100-\Omega$ resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Characteristic	Symbol	Ra	nge	Unit	Notos
Characteristic	Symbol	Min	Max	Unit	NOIES
Output voltage	Vo	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic jitter	J _D	_	0.17	UI p-p	_
Total jitter	J _T	_	0.35	UI p-p	_
Multiple output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 59. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Package Description

Table 72	. MPC8547E	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	_		2
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_		101
Reserved	AE25	_	_	2
Reserved	AG25	_	_	2
Reserved	AD24	_	_	2
Reserved	AF24	_		2
Reserved	AD27	_		2
Reserved	AD28, AE27, W17, AF26	_		2
Reserved	AH25	_		2
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11	0	GV _{DD}	—
MWE	E7	0	GV _{DD}	—
MCAS	H7	0	GV _{DD}	—
MRAS	L8	0	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	—
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	_
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	_
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	U20, V22, W20, Y22	_	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	0	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	—
SD_REF_CLK	T27	I	XV _{DD}	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
	General-Purpose Output			
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	_
	System Control			
HRESET	AG17	I	OV _{DD}	_
HRESET_REQ	AG16	0	OV _{DD}	29
SRESET	AG20	I	OV _{DD}	_
CKSTP_IN	AA9	I	OV _{DD}	_
CKSTP_OUT	AA8	0	OV _{DD}	2, 4
	Debug			
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29
MDVAL	AE5	0	OV _{DD}	6
CLK_OUT	AE21	0	OV _{DD}	11
	Clock			
RTC	AF16	I	OV _{DD}	—
SYSCLK	AH17	I	OV _{DD}	—
	JTAG			
ТСК	AG28	Ι	OV _{DD}	—
TDI	AH28	Ι	OV _{DD}	12
TDO	AF28	0	OV _{DD}	_
TMS	AH27	I	OV _{DD}	12
TRST	AH23	I	OV _{DD}	12

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
	Analog Signals			
MVREF	A18	l Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200 Ω (±1%) to GND	_
SD_IMP_CAL_TX	AB26	I	100 Ω (±1%) to GND	—
SD_PLL_TPA	U26	0	AVDD_SRDS	24

Table 74. MPC8543E Pinout Listing (continued)

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

• No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.



Figure 62. COP Connector Physical Pinout

23.2 Part Marking

Parts are marked as the example shown in Figure 64.



Notes:

TWLYYWW is final test traceability code. MMMMM is 5 digit mask number. CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States. YWWLAZ is assembly traceability code.

Figure 64. Part Marking for CBGA and PBGA Device

Rev. Number	Date	Substantive Change(s)
4	04/2009	 In Table 1, "Absolute Maximum Ratings ¹," and in Table 2, "Recommended Operating Conditions," moved text, "MII management voltage" from LV_{DD}/TV_{DD} to OV_{DD}, added "Ethernet management" to OVDD row of input voltage section. In Table 5, "SYSCLK AC Timing Specifications," added notes 7 and 8 to SYSCLK frequency and cycle
		 time. In Table 36, "MII Management DC Electrical Characteristics," changed all instances of LV_{DD}/OV_{DD} to OV_{DD}. Modified Section 16, "High-Speed Serial Interfaces (HSSI)," to reflect that there is only one SerDes. Modified DDR clk rate min from 133 to 166 MHz. Modified note in Table 75, "Processor Core Clocking Specifications (MPC8548E and MPC8547E), "." In Table 56, "Differential Transmitter (TX) Output Specifications," modified equations in Comments column, and changed all instances of "LO" to "LO." Also added note 8. In Table 57, "Differential Receiver (RX) Input Specifications," modified equations in Comments column, and in note 3, changed "TRX-EYE-MEDIAN-to-MAX-JITTER," to "T_{RX-EYE-MEDIAN-to-MAX-JITTER}." Modified Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds." Added a note on Section 4.1, "System Clock Timing," to limit the SYSCLK to 100 MHz if the core
		 frequency is less than 1200 MHz In Table 71, "MPC8548E Pinout ListingTable 72, "MPC8547E Pinout ListingTable 73, "MPC8545E Pinout ListingTable 74, "MPC8543E Pinout Listing," added note 5 to LA[28:31]. Added note to Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds."
3	01/2009	 [Section 4.6, "Platform Frequency Requirements for PCI-Express and Serial RapidIO." Changed minimum frequency equation to be 527 MHz for PCI x8. In Table 5, added note 7. Section 4.5, "Platform to FIFO Restrictions." Changed platform clock frequency to 4.2. Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." Added MII after GMII and add 'or 2.5 V' after 3.3 V. In Table 23, modified table title to include GMII, MII, RMII, and TBI. In Table 24 and Table 25, changed clock period minimum to 5.3. In Table 25, added a note
		 In Table 25, added a hole. In Table 26, Table 27, Table 28, Table 29, and Table 30, removed subtitle from table title. In Table 30 and Figure 15, changed all instances of PMA to TSEC<i>n</i>. In Section 8.2.5, "TBI Single-Clock Mode AC Specifications." Replaced first paragraph. In Table 34, Table 35, Figure 18, and Figure 20, changed all instances of REF_CLK to TSEC<i>n</i>_TX_CLK. In Table 36, changed all instances of OVpp to LVpp.
		 In Table 37, "MII Management AC Timing Specifications," changed MDC minimum clock pulse width high from 32 to 48 ns. Added new section, Section 16, "High-Speed Serial Interfaces (HSSI)." Section 16.1, "DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK." Added new paragraph. Section 17.1, "DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK." Added new paragraph. Added information to Figure 63, both in figure and in note. Section 22.3, "Decoupling Recommendations." Modified the recommendation.
		Table 87, "Part Numbering Nomenclature." In Silicon Version column added Ver. 2.1.2.

Table 88. Document Revision History (continued)