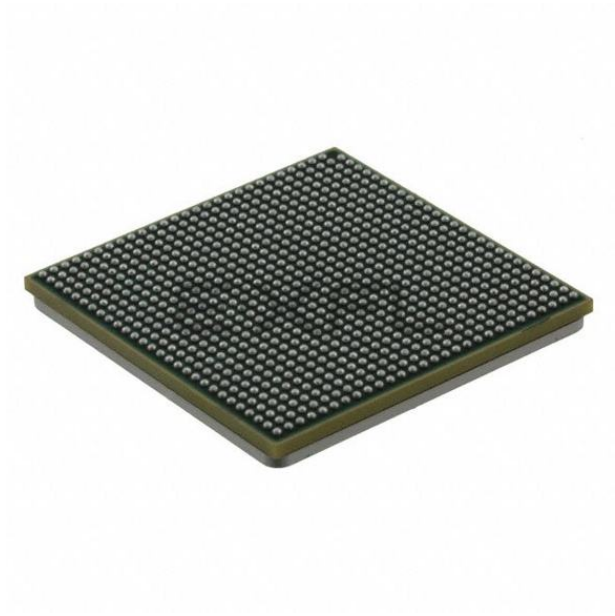

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.0GHz |
| Co-Processors/DSP | Signal Processing; SPE, Security; SEC |
| RAM Controllers | DDR, DDR2, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (4) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548ecvjaqgd |

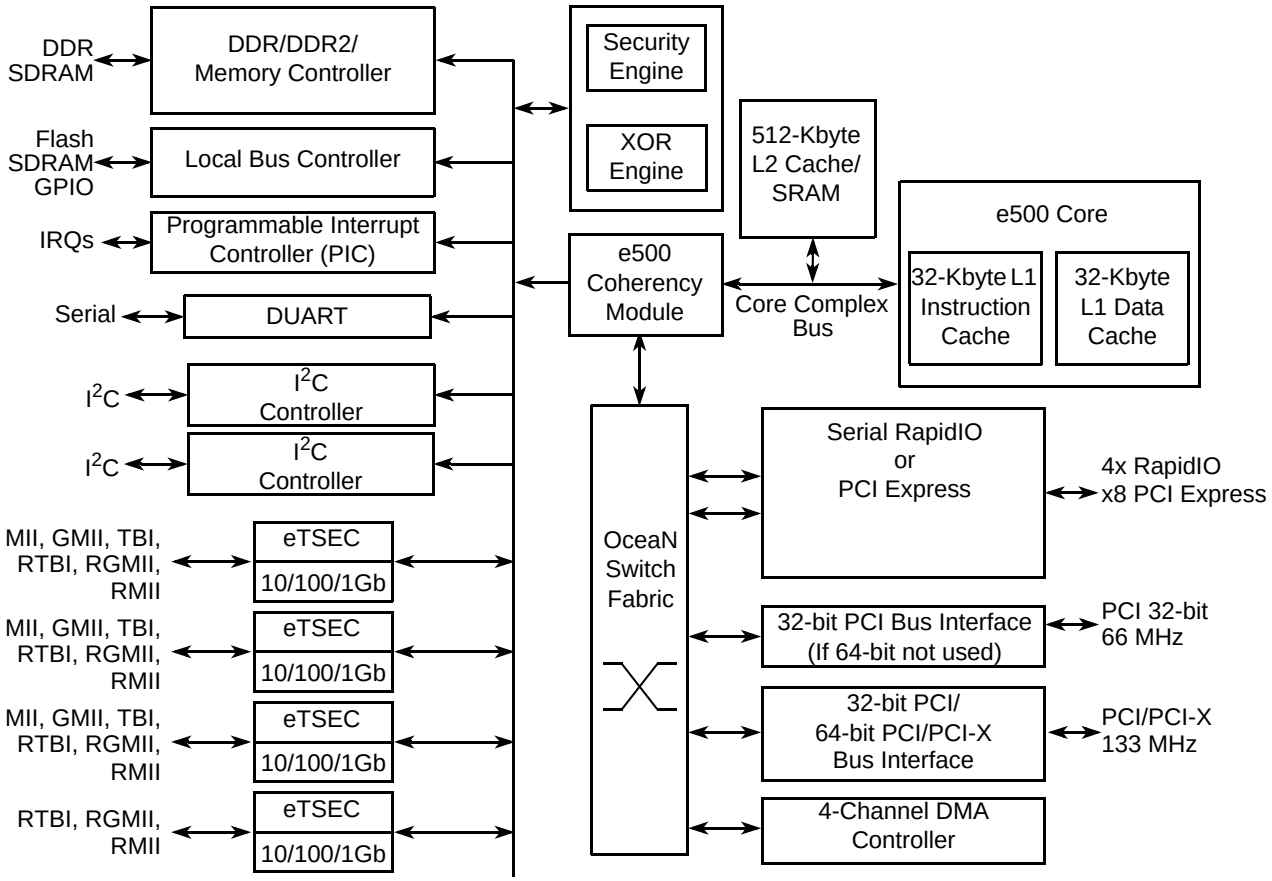


**Figure 1. Device Block Diagram**

## 1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance 32-bit core built on Power Architecture® technology.
  - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
  - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
  - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
  - 36-bit real addressing
  - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
  - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
  - Enhanced hardware and software debug support

  - Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL_2 compatible I/O (1.8-V SSTL_1.8 for DDR2)
- Support for battery-backed main memory

- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high-resolution timers/counters that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.
  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 2048 bits
    - Elliptic curve cryptography with $F_2m$ and F(p) modes and programmable field size up to 511 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES

## 4.3 eTSEC Gigabit Reference Clock Timing

The following table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the device.

**Table 6. EC_GTX_CLK125 AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 frequency | $f_{G125}$ | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | |
| EC_GTX_CLK125 rise and fall time<br>L/TVDD = 2.5 V<br>L/TVDD = 3.3 V | $t_{G125R}$, $t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle<br>GMII, TBI<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 2, 3 |

**Notes:**

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for $L/TV_{DD}$ = 2.5 V, and from 0.6 and 2.7 V for $L/TV_{DD}$ = 3.3 V.
2. Timing is guaranteed by design and characterization.
3. EC_GTX_CLK125 is used to generate the GTX clock TSEC*n*_GTX_CLK for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC*n*_ GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

## 4.4 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-x controller is not the SYSCLK input, but instead the PCI*n*_CLK. The following table provides the PCI/PCI-X reference clock AC timing specifications for the device.

**Table 7. PCI*n*_CLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| PCI*n*_CLK frequency | $f_{PCICLK}$ | 16 | — | 133 | MHz | — |
| PCI*n*_CLK cycle time | $t_{PCICLK}$ | 7.5 | — | 60 | ns | — |
| PCI*n*_CLK rise and fall time | $t_{PCIKH}$, $t_{PCIKL}$ | 0.6 | 1.0 | 2.1 | ns | 1, 2 |
| PCI*n*_CLK duty cycle | $t_{PCIKHKL}/t_{PCICLK}$ | 40 | — | 60 | % | 2 |

**Notes:**

1. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
2. Timing is guaranteed by design and characterization.

A timing diagram for TBI receive appears in Figure 16.

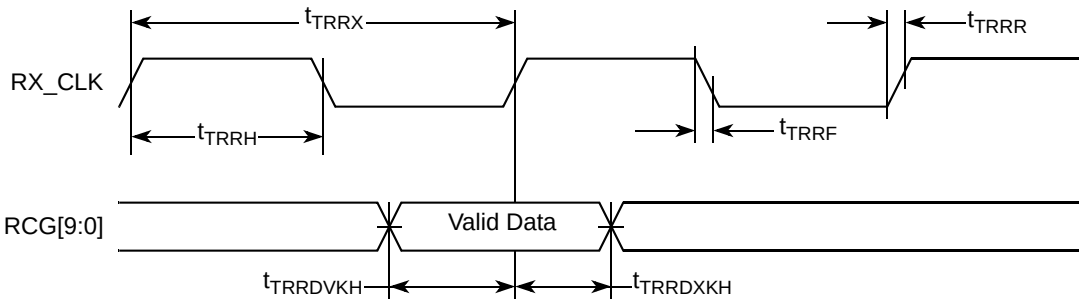


**Figure 16. TBI Single-Clock Mode Receive AC Timing Diagram**

## 8.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

**Table 33. RGMII and RTBI AC Timing Specifications**

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT}$[5] | –500[6] | 0 | 500[6] | ps |
| Data to clock input skew (at receiver) [2] | $t_{SKRGT}$ | 1.0 | — | 2.8 | ns |
| Clock period [3] | $t_{RGT}$[5] | 7.2 | 8.0 | 8.8 | ns |
| Duty cycle for 10BASE-T and 100BASE-TX[3, 4] | $t_{RGTH}/t_{RGT}$[5] | 45 | 50 | 55 | % |
| Rise time (20%–80%) | $t_{RGTR}$[5] | — | — | 0.75 | ns |
| Fall time (20%–80%) | $t_{RGTF}$[5] | — | — | 0.75 | ns |

**Notes:**

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of $t_{RGT}$ represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, $t_{RGT}$ scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three $t_{RGT}$ of the lowest speed transitioned between.
5. Guaranteed by characterization.
6. In rev 1.0 silicon, due to errata, $t_{SKRGT}$ is -650 ps (min) and 650 ps (max). See “eTSEC 10” in the device errata document.

**Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock | $t_{LBIXKL2}$ | –1.3 | — | ns | 4, 5 |
| LALE output transition to LAD/LDP output transition (LATCH hold time) | $t_{LBOTOT}$ | 1.5 | — | ns | 6 |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKLOV1}$ | — | –0.3 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | –0.1 | ns | 4 |
| Local bus clock to address valid for LAD | $t_{LBKLOV3}$ | — | 0 | ns | 4 |
| Local bus clock to LALE assertion | $t_{LBKLOV4}$ | — | 0 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | –3.7 | — | ns | 4 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | –3.7 | — | ns | 4 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 0.2 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 0.2 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by $t_{LBKHKT}$.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[*n*]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

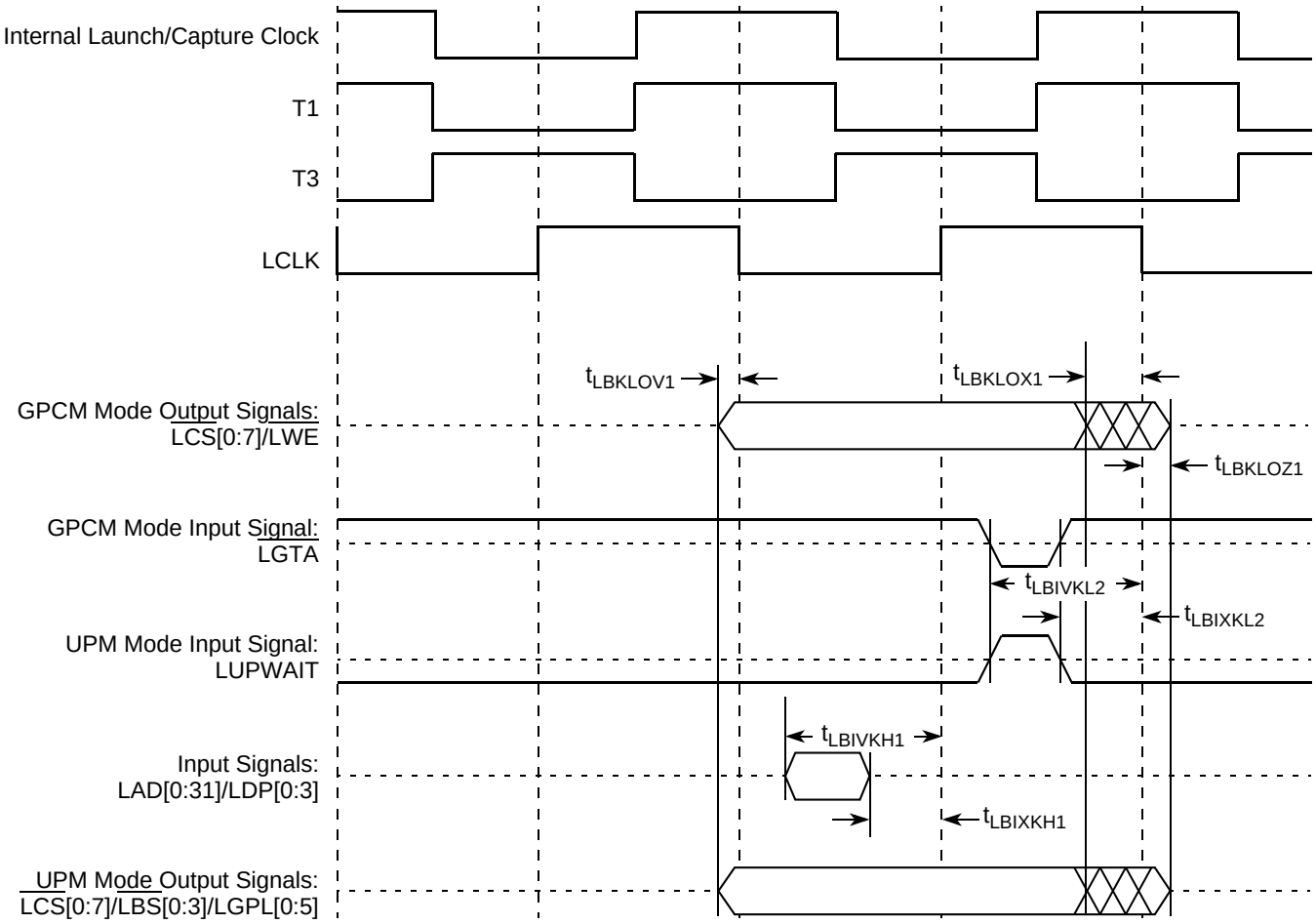


**Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)**

# 14 $GP_{OUT}/GP_{IN}$

This section describes the DC and AC electrical specifications for the $GP_{OUT}/GP_{IN}$ bus of the device.

## 14.1 $GP_{OUT}/GP_{IN}$ Electrical Characteristics

Table 47 and Table 48 provide the DC electrical characteristics for the $GP_{OUT}$ interface.

**Table 47. $GP_{OUT}$ DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 3.3 V | $BV_{DD}$ | 3.13 | 3.47 | V |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | $BV_{DD}$ – 0.2 | — | V |
| Low-level output voltage ($BV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.2 | V |

**Table 48. $GP_{OUT}$ DC Electrical Characteristics (2.5 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 2.5 V | $BV_{DD}$ | 2.37 | 2.63 | V |
| High-level output voltage ($BV_{DD}$ = min, $I_{OH}$ = –1 mA) | $V_{OH}$ | 2.0 | $BV_{DD}$ + 0.3 | V |
| Low-level output voltage ($BV_{DD}$ min, $I_{OL}$ = 1 mA) | $V_{OL}$ | GND – 0.3 | 0.4 | V |

Table 49 and Table 50 provide the DC electrical characteristics for the $GP_{IN}$ interface.

**Table 49. $GP_{IN}$ DC Electrical Characteristics (3.3 V DC)**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage 3.3 V | $BV_{DD}$ | 3.13 | 3.47 | V |
| High-level input voltage | $V_{IH}$ | 2 | $BV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current ($BV_{IN}$ [1] = 0 V or $BV_{IN}$ = $BV_{DD}$) | $I_{IN}$ | — | ±5 | μA |

**Note:**

1. The symbol $BV_{IN}$, in this case, represents the $BV_{IN}$ symbol referenced in Table 1.

## 16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected must provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver must be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes reference clocks are defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 17.2, “AC Requirements for PCI Express SerDes Clocks”
- Section 18.2, “AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK”

### 16.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ are designed to work with a spread spectrum clock (+0% to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

## 16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 47 shows the reference circuits for SerDes data lane’s transmitter and receiver.

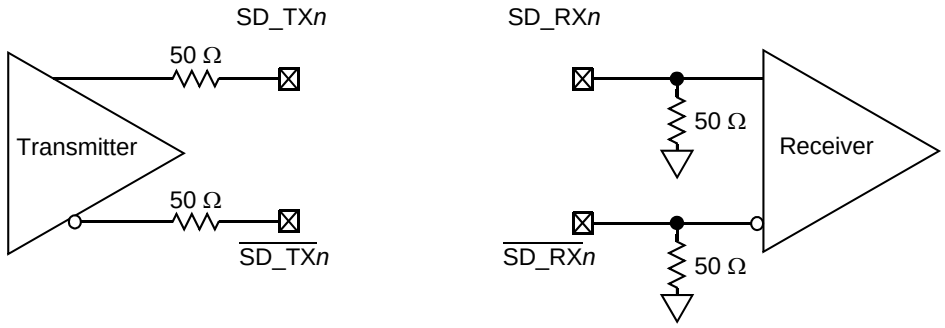


**Figure 47. SerDes Transmitter and Receiver Reference Circuits**

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO, or SGMII) in this document based on the application usage:

- Section 17, “PCI Express”
- Section 18, “Serial RapidIO”

Note that external an AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in the specification of each protocol section.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

**NOTE**

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.

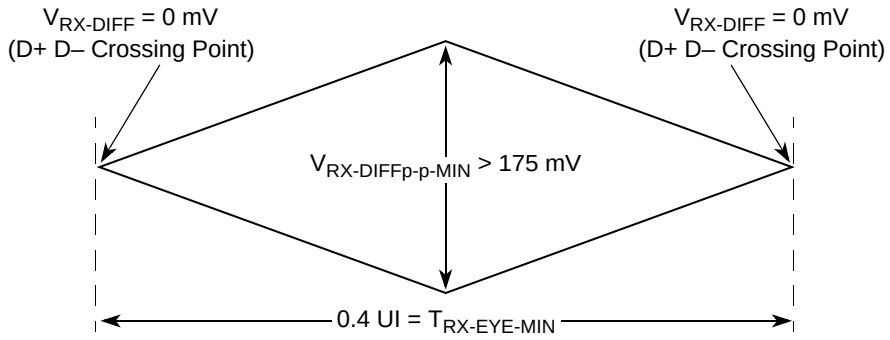


**Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification**

## 17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

**NOTE**

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

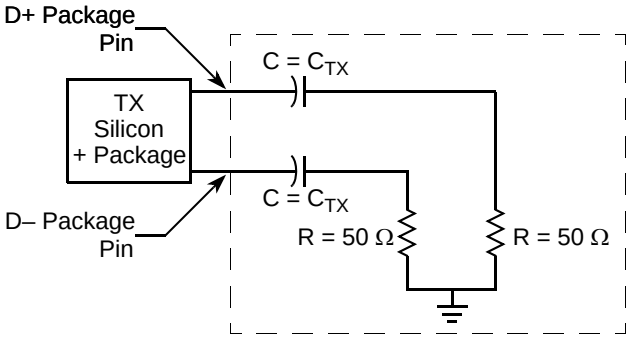


**Figure 50. Compliance Test/Measurement Load**

components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

**Table 66. Receiver AC Timing Specifications—1.25 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential input voltage | $V_{IN}$ | 200 | 1600 | mVp-p | Measured at receiver |
| Deterministic jitter tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total jitter tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple input skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit error rate | BER | — | $10^{-12}$ | — | — |
| Unit interval | UI | 800 | 800 | ps | ±100 ppm |

**Note:**
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

**Table 67. Receiver AC Timing Specifications—2.5 GBaud**

| Characteristic | Symbol | Range | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Differential input voltage | $V_{IN}$ | 200 | 1600 | mVp-p | Measured at receiver |
| Deterministic jitter tolerance | $J_D$ | 0.37 | — | UI p-p | Measured at receiver |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | 0.55 | — | UI p-p | Measured at receiver |
| Total jitter tolerance[1] | $J_T$ | 0.65 | — | UI p-p | Measured at receiver |
| Multiple input skew | $S_{MI}$ | — | 24 | ns | Skew at the receiver input between lanes of a multilane link |
| Bit error rate | BER | — | $10^{-12}$ | | — |
| Unit interval | UI | 400 | 400 | ps | ±100 ppm |

**Note:**
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

**Table 71. MPC8548E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{MWE}}$ | E7 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | H7 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | L8 | O | $GV_{DD}$ | — |
| MCKE[0:3] | F10, C10, J11, H11 | O | $GV_{DD}$ | 11 |
| $\overline{\text{MCS}}$[0:3] | K8, J8, G8, F8 | O | $GV_{DD}$ | — |
| MCK[0:5] | H9, B15, G2, M9, A14, F1 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:5] | J9, A15, G1, L9, B14, F2 | O | $GV_{DD}$ | — |
| MODT[0:3] | E6, K6, L7, M7 | O | $GV_{DD}$ | — |
| MDIC[0:1] | A19, B19 | I/O | $GV_{DD}$ | 36 |
| **Local Bus Controller Interface** | | | | |
| LAD[0:31] | E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21 | I/O | $BV_{DD}$ | — |
| LDP[0:3] | K21, C28, B26, B22 | I/O | $BV_{DD}$ | — |
| LA[27] | H21 | O | $BV_{DD}$ | 5, 9 |
| LA[28:31] | H20, A27, D26, A28 | O | $BV_{DD}$ | 5, 7, 9 |
| $\overline{\text{LCS}}$[0:4] | J25, C20, J24, G26, A26 | O | $BV_{DD}$ | |
| $\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$ | D23 | I/O | $BV_{DD}$ | 1 |
| $\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$ | G20 | O | $BV_{DD}$ | 1 |
| $\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$ | E21 | O | $BV_{DD}$ | 1 |
| $\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/LSDDQM[0] | G25 | O | $BV_{DD}$ | 5, 9 |
| $\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/LSDDQM[1] | C23 | O | $BV_{DD}$ | 5, 9 |
| $\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/LSDDQM[2] | J21 | O | $BV_{DD}$ | 5, 9 |
| $\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/LSDDQM[3] | A24 | O | $BV_{DD}$ | 5, 9 |
| LALE | H24 | O | $BV_{DD}$ | 5, 8, 9 |
| LBCTL | G27 | O | $BV_{DD}$ | 5, 8, 9 |
| LGPL0/LSDA10 | F23 | O | $BV_{DD}$ | 5, 9 |
| LGPL1/$\overline{\text{LSDWE}}$ | G22 | O | $BV_{DD}$ | 5, 9 |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$ | B27 | O | $BV_{DD}$ | 5, 8, 9 |
| LGPL3/$\overline{\text{LSDCAS}}$ | F24 | O | $BV_{DD}$ | 5, 9 |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE | H23 | I/O | $BV_{DD}$ | — |
| LGPL5 | E26 | O | $BV_{DD}$ | 5, 9 |
| LCKE | E24 | O | $BV_{DD}$ | — |
| LCLK[0:2] | E23, D24, H22 | O | $BV_{DD}$ | — |

**Table 72. MPC8547E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| SD_PLL_TPA | U26 | O | — | 24 |

**Note:** All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

**NOTE**

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

**Table 73. MPC8545E Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **PCI1 and PCI2 (One 64-Bit or Two 32-Bit)** | | | | |
| PCI1_AD[63:32]/PCI2_AD[31:0] | AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24 | I/O | $OV_{DD}$ | 17 |
| PCI1_AD[31:0] | AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15 | I/O | $OV_{DD}$ | 17 |
| PCI1_C_$\overline{BE}$[7:4]/PCI2_C_$\overline{BE}$[3:0] | AF15, AD14, AE15, AD15 | I/O | $OV_{DD}$ | 17 |
| PCI1_C_$\overline{BE}$[3:0] | AF9, AD11, Y12, Y13 | I/O | $OV_{DD}$ | 17 |
| PCI1_PAR64/PCI2_PAR | W15 | I/O | $OV_{DD}$ | — |
| $\overline{PCI1\_GNT}$[4:1] | AG6, AE6, AF5, AH5 | O | $OV_{DD}$ | 5, 9, 35 |
| $\overline{PCI1\_GNT0}$ | AG5 | I/O | $OV_{DD}$ | — |
| $\overline{PCI1\_IRDY}$ | AF11 | I/O | $OV_{DD}$ | 2 |
| PCI1_PAR | AD12 | I/O | $OV_{DD}$ | — |
| $\overline{PCI1\_PERR}$ | AC12 | I/O | $OV_{DD}$ | 2 |
| $\overline{PCI1\_SERR}$ | V13 | I/O | $OV_{DD}$ | 2, 4 |
| $\overline{PCI1\_STOP}$ | W12 | I/O | $OV_{DD}$ | 2 |
| $\overline{PCI1\_TRDY}$ | AG11 | I/O | $OV_{DD}$ | 2 |
| $\overline{PCI1\_REQ}$[4:1] | AH2, AG4, AG3, AH4 | I | $OV_{DD}$ | — |
| $\overline{PCI1\_REQ0}$ | AH3 | I/O | $OV_{DD}$ | — |
| PCI1_CLK | AH26 | I | $OV_{DD}$ | 39 |
| $\overline{PCI1\_DEVSEL}$ | AH11 | I/O | $OV_{DD}$ | 2 |

**Table 73. MPC8545E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{SD\_TX}}$[0:3] | M23, N21, P23, R21 | O | $XV_{DD}$ | — |
| Reserved | W26, Y28, AA26, AB28 | — | — | 40 |
| Reserved | W25, Y27, AA25, AB27 | — | — | 40 |
| Reserved | U20, V22, W20, Y22 | — | — | 15 |
| Reserved | U21, V23, W21, Y23 | — | — | 15 |
| SD_PLL_TPD | U28 | O | $XV_{DD}$ | 24 |
| SD_REF_CLK | T28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK}}$ | T27 | I | $XV_{DD}$ | — |
| Reserved | AC1, AC3 | — | — | 2 |
| Reserved | M26, V28 | — | — | 32 |
| Reserved | M25, V27 | — | — | 34 |
| Reserved | M20, M21, T22, T23 | — | — | 38 |
| **General-Purpose Output** | | | | |
| GPOUT[24:31] | K26, K25, H27, G28, H25, J26, K24, K23 | O | $BV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | AG17 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET\_REQ}}$ | AG16 | O | $OV_{DD}$ | 29 |
| $\overline{\text{SRESET}}$ | AG20 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_IN}}$ | AA9 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_OUT}}$ | AA8 | O | $OV_{DD}$ | 2, 4 |
| **Debug** | | | | |
| TRIG_IN | AB2 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY/$\overline{\text{QUIESCE}}$ | AB1 | O | $OV_{DD}$ | 6, 9, 19, 29 |
| MSRCID[0:1] | AE4, AG2 | O | $OV_{DD}$ | 5, 6, 9 |
| MSRCID[2:4] | AF3, AF1, AF2 | O | $OV_{DD}$ | 6, 19, 29 |
| MDVAL | AE5 | O | $OV_{DD}$ | 6 |
| CLK_OUT | AE21 | O | $OV_{DD}$ | 11 |
| **Clock** | | | | |
| RTC | AF16 | I | $OV_{DD}$ | — |
| SYSCLK | AH17 | I | $OV_{DD}$ | — |
| **JTAG** | | | | |
| TCK | AG28 | I | $OV_{DD}$ | — |
| TDI | AH28 | I | $OV_{DD}$ | 12 |

**Table 73. MPC8545E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $GV_{DD}$ | B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13 | Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V) | $GV_{DD}$ | — |
| $BV_{DD}$ | C21, C24, C27, E20, E25, G19, G23, H26, J20 | Power for local bus (1.8 V, 2.5 V, 3.3 V) | $BV_{DD}$ | — |
| $V_{DD}$ | M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19 | Power for core (1.1 V) | $V_{DD}$ | — |
| $SV_{DD}$ | L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27 | Core power for SerDes transceivers (1.1 V) | $SV_{DD}$ | — |
| $XV_{DD}$ | L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20 | Pad power for SerDes transceivers (1.1 V) | $XV_{DD}$ | — |
| AVDD_LBIU | J28 | Power for local bus PLL (1.1 V) | — | 26 |
| AVDD_PCI1 | AH21 | Power for PCI1 PLL (1.1 V) | — | 26 |
| AVDD_PCI2 | AH22 | Power for PCI2 PLL (1.1 V) | — | 26 |
| AVDD_CORE | AH15 | Power for e500 PLL (1.1 V) | — | 26 |
| AVDD_PLAT | AH19 | Power for CCB PLL (1.1 V) | — | 26 |
| AVDD_SRDS | U25 | Power for SRDSPLL (1.1 V) | — | 26 |
| SENSEVDD | M14 | O | $V_{DD}$ | 13 |
| SENSEVSS | M16 | — | — | 13 |
| **Analog Signals** | | | | |
| MVREF | A18 | I Reference voltage signal for DDR | MVREF | — |

**Table 74. MPC8543E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{MWE}}$ | E7 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | H7 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | L8 | O | $GV_{DD}$ | — |
| MCKE[0:3] | F10, C10, J11, H11 | O | $GV_{DD}$ | 11 |
| $\overline{\text{MCS}}$[0:3] | K8, J8, G8, F8 | O | $GV_{DD}$ | — |
| MCK[0:5] | H9, B15, G2, M9, A14, F1 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:5] | J9, A15, G1, L9, B14, F2 | O | $GV_{DD}$ | — |
| MODT[0:3] | E6, K6, L7, M7 | O | $GV_{DD}$ | — |
| MDIC[0:1] | A19, B19 | I/O | $GV_{DD}$ | 36 |
| **Local Bus Controller Interface** | | | | |
| LAD[0:31] | E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21 | I/O | $BV_{DD}$ | — |
| LDP[0:3] | K21, C28, B26, B22 | I/O | $BV_{DD}$ | — |
| LA[27] | H21 | O | $BV_{DD}$ | 5, 9 |
| LA[28:31] | H20, A27, D26, A28 | O | $BV_{DD}$ | 5, 7, 9 |
| $\overline{\text{LCS}}$[0:4] | J25, C20, J24, G26, A26 | O | $BV_{DD}$ | — |
| $\overline{\text{LCS5}}$/$\overline{\text{DMA\_DREQ2}}$ | D23 | I/O | $BV_{DD}$ | 1 |
| $\overline{\text{LCS6}}$/$\overline{\text{DMA\_DACK2}}$ | G20 | O | $BV_{DD}$ | 1 |
| $\overline{\text{LCS7}}$/$\overline{\text{DMA\_DDONE2}}$ | E21 | O | $BV_{DD}$ | 1 |
| $\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/LSDDQM[0] | G25 | O | $BV_{DD}$ | 5, 9 |
| $\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/LSDDQM[1] | C23 | O | $BV_{DD}$ | 5, 9 |
| $\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/LSDDQM[2] | J21 | O | $BV_{DD}$ | 5, 9 |
| $\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/LSDDQM[3] | A24 | O | $BV_{DD}$ | 5, 9 |
| LALE | H24 | O | $BV_{DD}$ | 5, 8, 9 |
| LBCTL | G27 | O | $BV_{DD}$ | 5, 8, 9 |
| LGPL0/LSDA10 | F23 | O | $BV_{DD}$ | 5, 9 |
| LGPL1/$\overline{\text{LSDWE}}$ | G22 | O | $BV_{DD}$ | 5, 9 |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$ | B27 | O | $BV_{DD}$ | 5, 8, 9 |
| LGPL3/$\overline{\text{LSDCAS}}$ | F24 | O | $BV_{DD}$ | 5, 9 |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE | H23 | I/O | $BV_{DD}$ | — |
| LGPL5 | E26 | O | $BV_{DD}$ | 5, 9 |
| LCKE | E24 | O | $BV_{DD}$ | — |
| LCLK[0:2] | E23, D24, H22 | O | $BV_{DD}$ | — |

**Table 80. Memory Bus Clocking Specifications (MPC8543E)**

| Characteristic | Maximum Processor Core Frequency | | Unit | Notes |
|---|---|---|---|---|
| | 800, 1000 MHz | | | |
| | Min | Max | | |
| Memory bus clock speed | 166 | 200 | MHz | 1, 2 |

**Notes:**

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

## 20.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 81:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI_CLK, see the *PCI 2.2 Specification*.

**Table 81. CCB Clock Ratio**

| Binary Value of LA[28:31] Signals | CCB:SYSCLK Ratio | Binary Value of LA[28:31] Signals | CCB:SYSCLK Ratio |
|---|---|---|---|
| 0000 | 16:1 | 1000 | 8:1 |
| 0001 | Reserved | 1001 | 9:1 |
| 0010 | 2:1 | 1010 | 10:1 |
| 0011 | 3:1 | 1011 | Reserved |
| 0100 | 4:1 | 1100 | 12:1 |
| 0101 | 5:1 | 1101 | 20:1 |
| 0110 | 6:1 | 1110 | Reserved |
| 0111 | Reserved | 1111 | Reserved |

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

## 22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

### 22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

- $\overline{\text{TRST}}$ must be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system

## 22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

### 22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

**NOTE**

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to $XV_{DD}$. Pins V27 and M25 must be tied to GND through a 300-Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

### 22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- $\overline{\text{SD\_TX}}$[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK

**Table 87. Part Numbering Nomenclature (continued)**

| MPC | *nnnn* | *t* | *pp* | *ff* | *c* | *r* |
|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Temperature** | **Package[1, 2, 3]** | **Processor Frequency[4]** | **Core Frequency** | **Silicon Version** |
| MPC | 8545E | Blank = 0 to 105°C<br>C = –40° to 105°C | HX = CBGA<br>VU = Pb-free CBGA<br>PX = PBGA<br>VT = Pb-free PBGA | AT = 1200<br>AQ = 1000<br>AN = 800 | G = 400 | Blank = Ver. 2.0 (SVR = 0x80390220)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x (SVR = 0x80390231) |
| | 8545 | | | | | Blank = Ver. 2.0 (SVR = 0x80310220)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x (SVR = 0x80310231) |
| | 8543E | | | AQ = 1000<br>AN = 800 | | Blank = Ver. 2.0 (SVR = 0x803A0020)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x (SVR = 0x803A0031) |
| | 8543 | | | | | Blank = Ver. 2.0 (SVR = 0x80320020)<br>A = Ver. 2.1.1<br>B = Ver. 2.1.2<br>D = Ver. 3.1.x (SVR = 0x80320031) |

**Notes:**

1. See Section 19, “Package Description,” for more information on available package types.
2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.
4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.

## 23.2 Part Marking

Parts are marked as the example shown in Figure 64.


**Notes:**

TWLYYWW is final test traceability code.
MMMMM is 5 digit mask number.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.
YWWLAZ is assembly traceability code.

**Figure 64. Part Marking for CBGA and PBGA Device**