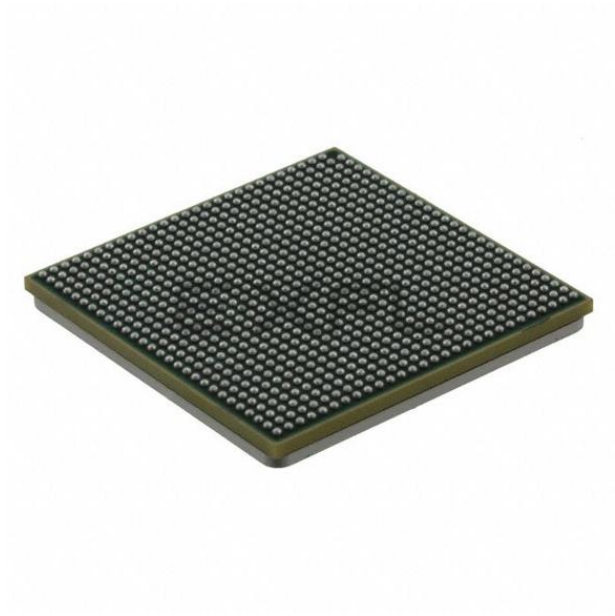


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

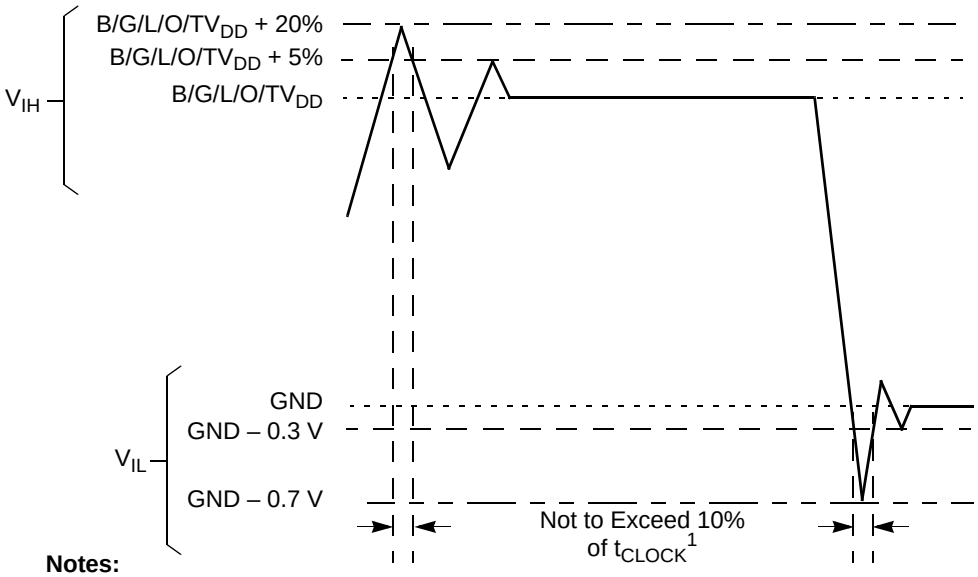
Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548ehxatg

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	Tj	0 to 105	°C	—

Notes:
1. This voltage is the input to the filter discussed in Section 22.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.



Notes:
1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI*n*_CLK or SYSCLK.
   For SerDes, t_{CLOCK} references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

4 Input Clocks

This section discusses the timing for the input clocks.

4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	t_{SYSCLK}	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.See Section 20.2, “CCB/SYSCLK PLL Ratio,” and Section 20.3, “e500 Core PLL Ratio,” for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver’s closed loop jitter bandwidth must be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
7. For spread spectrum clocking. Guidelines are + 0% to –1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[*n*] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8548E PowerQUICC III Integrated Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[*n*] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 3 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

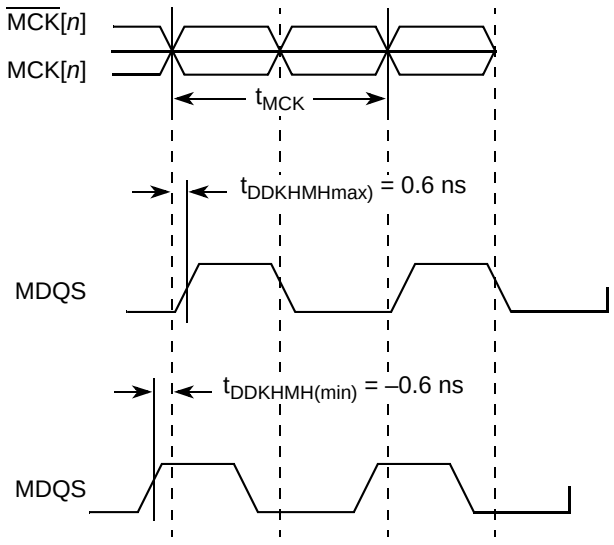


Figure 3. Timing Diagram for tDDKHMH

Table 23. GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND –0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	3

Notes:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports eTSECs 3 and 4.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performances and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.5, "Platform to FIFO Restrictions."

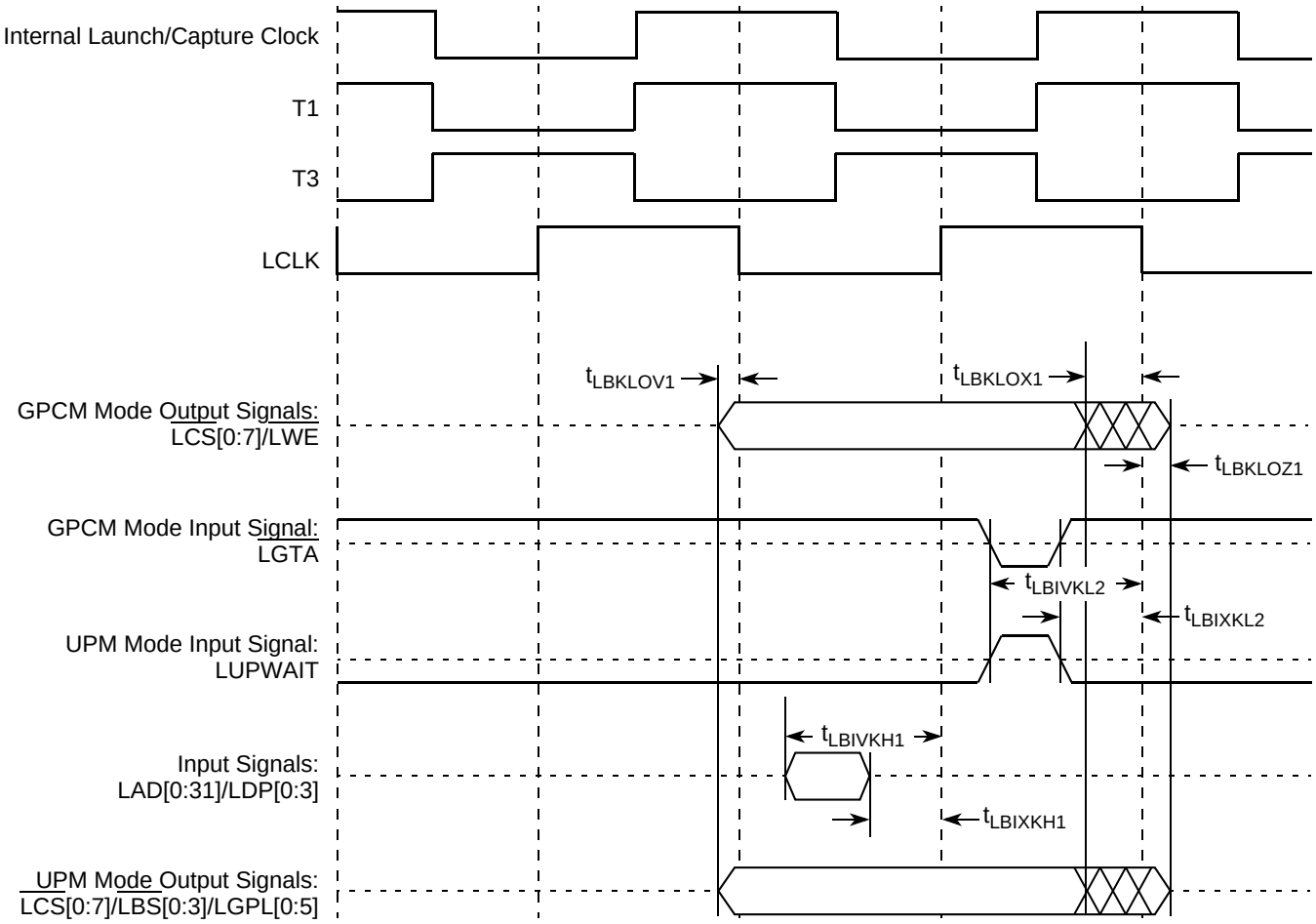


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 2	 20 10	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 29 provides the AC test load for TDO and the boundary-scan outputs.

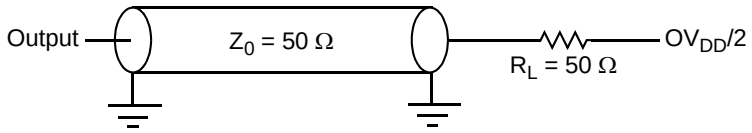


Figure 29. AC Test Load for the JTAG Interface

Figure 30 provides the JTAG clock input timing diagram.

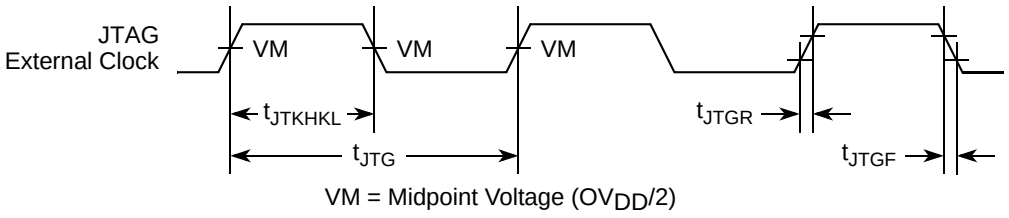


Figure 30. JTAG Clock Input Timing Diagram

16 High-Speed Serial Interfaces (HSSI)

The device features one Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express and/or serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for the description. The figure shows a waveform for either a transmitter output (SD_TX and $\overline{\text{SD\_TX}}$) or a receiver input (SD_RX and $\overline{\text{SD\_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- Single-ended swing
  The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.
- Differential output voltage, V_{OD} (or differential output swing):
  The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The V_{OD} value can be either positive or negative.
- Differential input voltage, V_{ID} (or differential input swing):
  The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX} - V_{\overline{SD\_RX}}$. The V_{ID} value can be either positive or negative.
- Differential peak voltage, V_{DIFFp}
  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
- Differential peak-to-peak, $V_{DIFFp-p}$
  Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
- Common mode voltage, V_{cm}
  The common mode voltage is equal to one half of the sum of the voltages between each conductor

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.

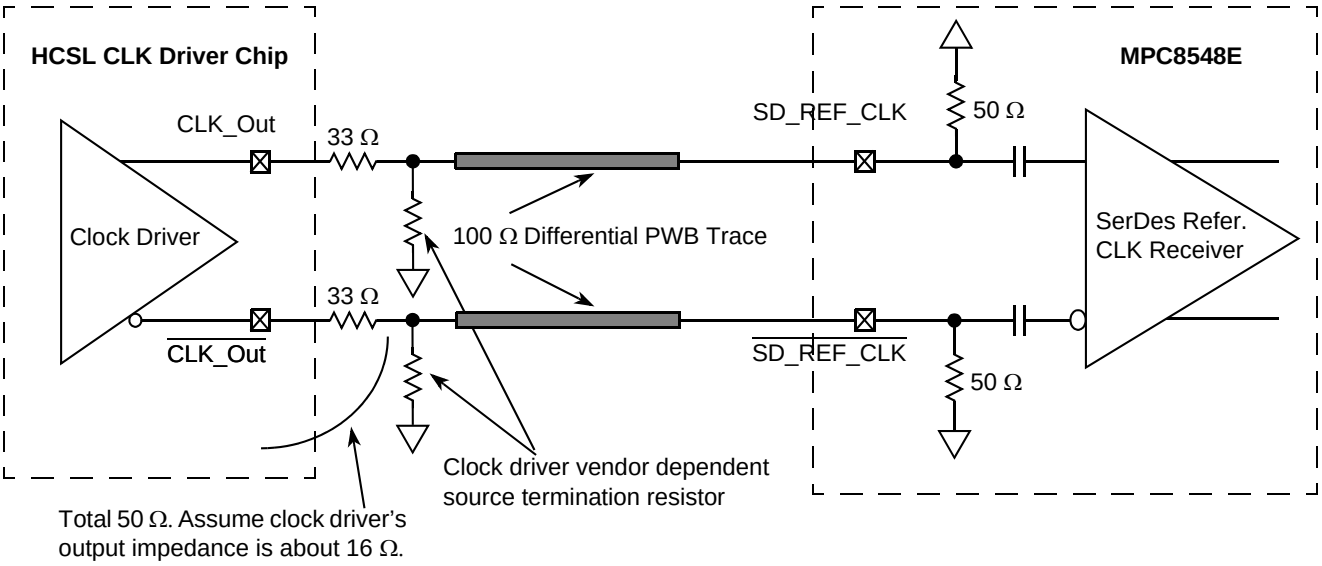


Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

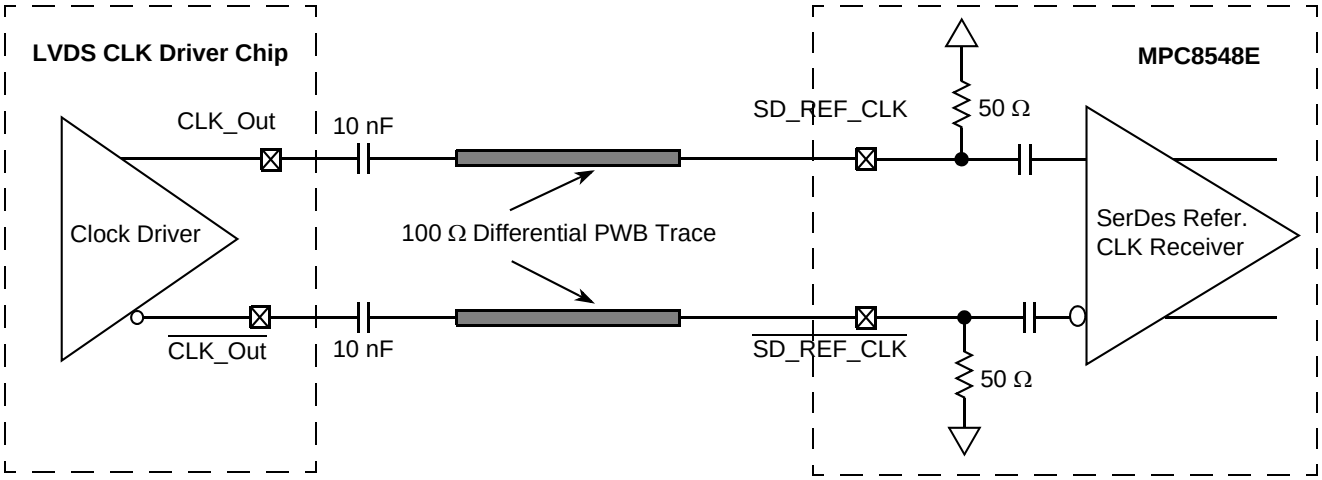


Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$T_{crosslink}$	Crosslink random timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 50 and measured over any 250 consecutive TX UIs. (Also see the transmitter compliance eye diagram shown in Figure 48.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 50 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications Rev 1.0a.*
7. See Section 4.2.6.3 of the *PCI Express Base Specifications Rev 1.0a.*
8. MPC8548E SerDes transmitter does not have CTX built in. An external AC coupling capacitor is required.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 48 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (for example, least squares and median deviation fits).

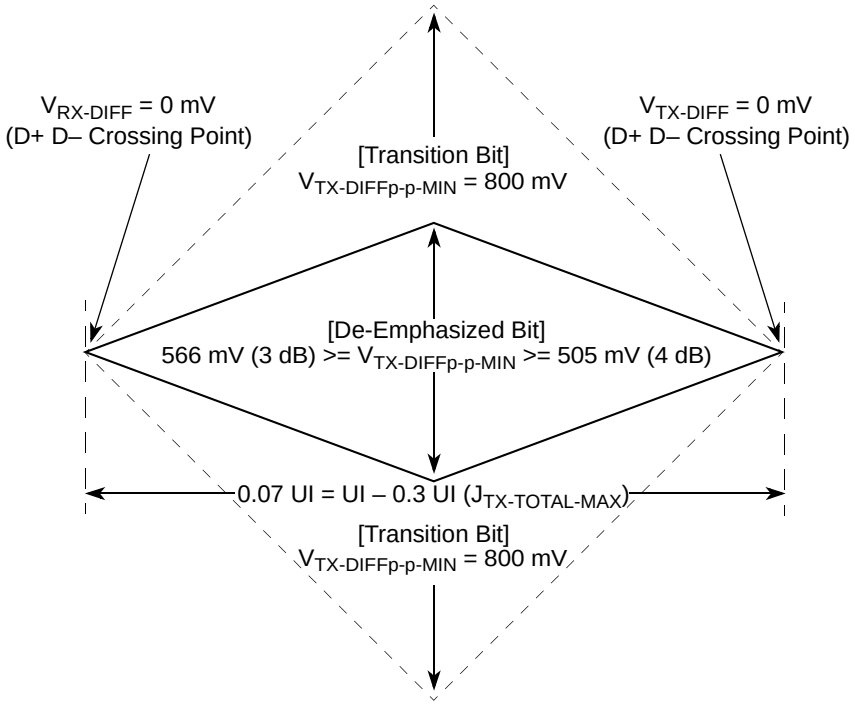


Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 57. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$. See Note 2.
T_{RX-EYE}	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.

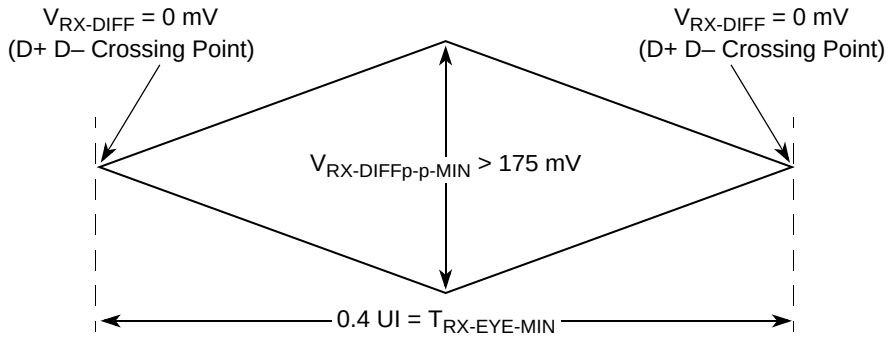


Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

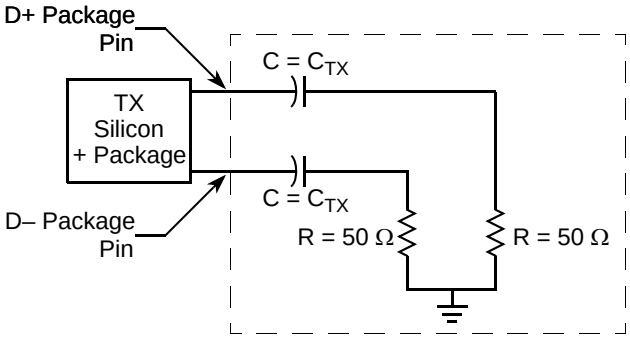


Figure 50. Compliance Test/Measurement Load

components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

Table 66. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}	—	—
Unit interval	UI	800	800	ps	±100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential input voltage	V_{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10^{-12}		—
Unit interval	UI	400	400	ps	±100 ppm

Note:
1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

19.2 Mechanical Dimensions of the HiCTE FC-CBGA and FC-PBGA with Full Lid

The following figures show the mechanical dimensions and bottom surface nomenclature for the MPC8548E HiCTE FC-CBGA and FC-PBGA packages.

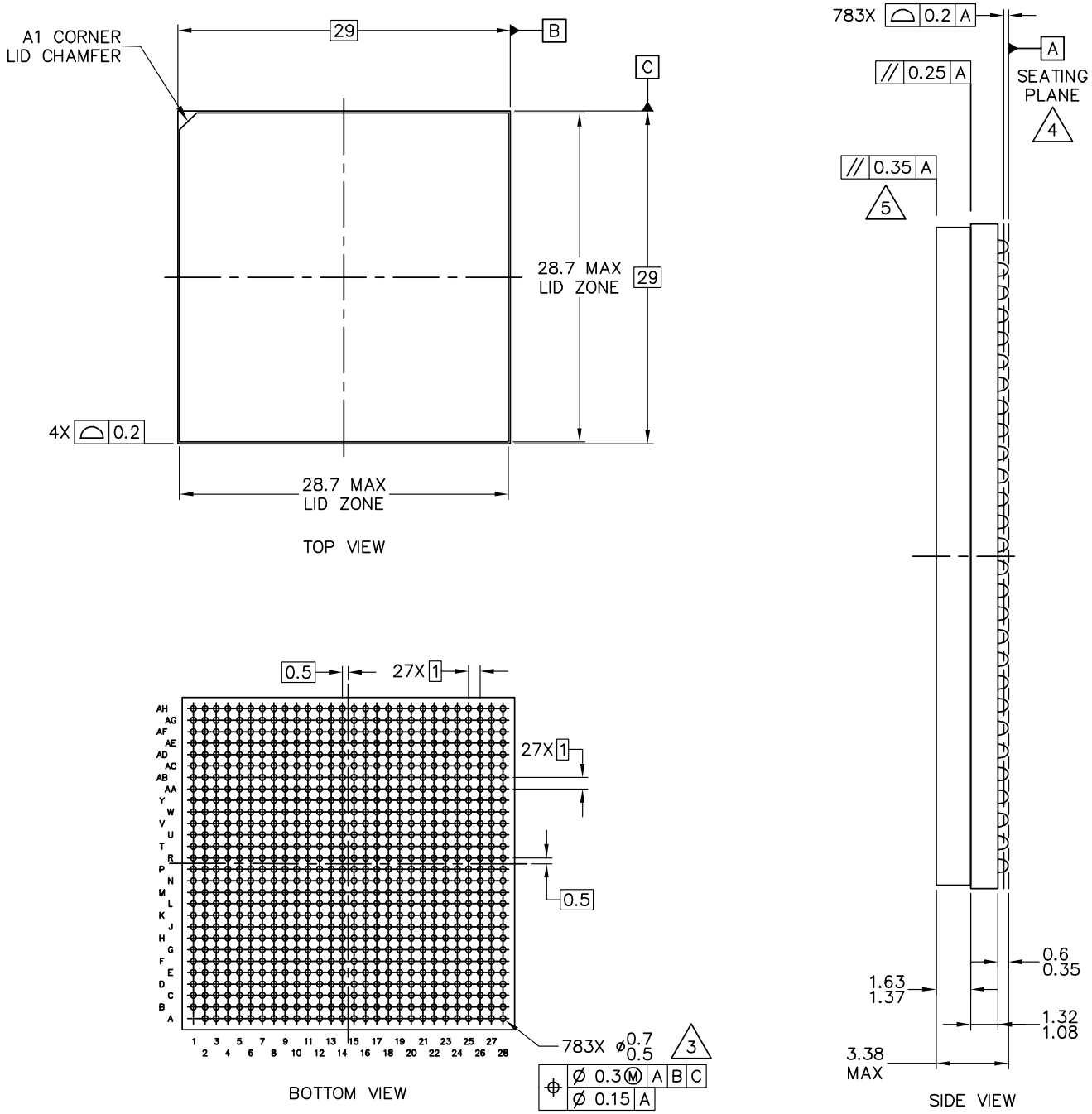


Figure 55. Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

25.These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal machine operation.

26.Independent supplies derived from board V_{DD}.

27.Recommend a pull-up resistor (~1 kΩ) be placed on this pin to OV_{DD}.

29. The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], TSEC4_TXD3/TSEC3_TXD7, HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP.

30.This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.

31.This pin is only an output in eTSEC3 FIFO mode when used as Rx flow control.

32.These pins must be connected to XV_{DD}.

33.TSEC2_TXD1, TSEC2_TX_ER are multiplexed as cfg_dram_type[0:1]. They must be valid at power-up, even before HRESET assertion.

34.These pins must be pulled to ground through a 300-Ω (±10%) resistor.

35.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as 'no connect' or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block drives the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.

36.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

38.These pins must be left floating.

39. If PCI1 or PCI2 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1_CLK or PCI2_CLK. Otherwise the processor will not boot up.

40.These pins must be connected to GND.

101.This pin requires an external 4.7-kΩ resistor to GND.

102.For Rev. 2.x silicon, DMA_DACK[0:1] must be 0b11 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

103.If these pins are not used as GPIN*n* (general-purpose input), they must be pulled low (to GND) or high (to LV_{DD}) through 2–10 kΩ resistors.

104.These must be pulled low to GND through 2–10 kΩ resistors if they are not used.

105.These must be pulled low or high to LV_{DD} through 2–10 kΩ resistors if they are not used.

106.For rev. 2.x silicon, DMA_DACK[0:1] must be 0b10 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

107.For rev. 2.x silicon, DMA_DACK[0:1] must be 0b01 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

108.For rev. 2.x silicon, DMA_DACK[0:1] must be 0b11 during POR configuration; for rev. 1.x silicon, the pin values during POR configuration are don't care.

109.This is a test signal for factory use only and must be pulled down (100 Ω – 1 kΩ) to GND for normal machine operation.

110.These pins must be pulled high to OV_{DD} through 2–10 kΩ resistors.

111.If these pins are not used as GPIN*n* (general-purpose input), they must be pulled low (to GND) or high (to OV_{DD}) through 2–10 kΩ resistors.

112.This pin must not be pulled down during POR configuration.

113.These should be pulled low or high to OV_{DD} through 2–10 kΩ resistors.

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	AF28	O	OV_{DD}	—
TMS	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	AH23	I	OV_{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	25
L2_TSTCLK	AE22	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AH14	I	OV_{DD}	25
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV_{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV_{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV_{DD}	—

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GV_{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV_{DD}	—
BV_{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—
V_{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V_{DD}	—
SV_{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV_{DD}	—
XV_{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV_{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V_{DD}	13
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AG28	I	OV_{DD}	—
TDI	AH28	I	OV_{DD}	12
TDO	AF28	O	OV_{DD}	—
TMS	AH27	I	OV_{DD}	12
$\overline{\text{TRST}}$	AH23	I	OV_{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV_{DD}	25
L2_TSTCLK	AE22	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV_{DD}	25
TEST_SEL	AH14	I	OV_{DD}	109
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV_{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV_{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV_{DD}	—

Table 87. Part Numbering Nomenclature (continued)

MPC	*nnnn*	*t*	*pp*	*ff*	*c*	*r*
Product Code	**Part Identifier**	**Temperature**	**Package[1, 2, 3]**	**Processor Frequency[4]**	**Core Frequency**	**Silicon Version**
MPC	8545E	Blank = 0 to 105°C C = –40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

Notes:

1. See Section 19, “Package Description,” for more information on available package types.
2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.
3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.
4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.

Table 88. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	04/2009	• In Table 1, "Absolute Maximum Ratings [1]," and in Table 2, "Recommended Operating Conditions," moved text, "MII management voltage" from LV_{DD}/TV_{DD} to OV_{DD}, added "Ethernet management" to OVDD row of input voltage section. • In Table 5, "SYSCLK AC Timing Specifications," added notes 7 and 8 to SYSCLK frequency and cycle time. • In Table 36, "MII Management DC Electrical Characteristics," changed all instances of LV_{DD}/OV_{DD} to OV_{DD}. • Modified Section 16, "High-Speed Serial Interfaces (HSSI)," to reflect that there is only one SerDes. • Modified DDR clk rate min from 133 to 166 MHz. • Modified note in Table 75, "Processor Core Clocking Specifications (MPC8548E and MPC8547E), "." • In Table 56, "Differential Transmitter (TX) Output Specifications," modified equations in Comments column, and changed all instances of "LO" to "L0." Also added note 8. • In Table 57, "Differential Receiver (RX) Input Specifications," modified equations in Comments column, and in note 3, changed "TRX-EYE-MEDIAN-to-MAX-JITTER," to "$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$." • Modified Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds." • Added a note on Section 4.1, "System Clock Timing," to limit the SYSCLK to 100 MHz if the core frequency is less than 1200 MHz • In Table 71, "MPC8548E Pinout ListingTable 72, "MPC8547E Pinout ListingTable 73, "MPC8545E Pinout ListingTable 74, "MPC8543E Pinout Listing," added note 5 to LA[28:31]. • Added note to Table 83, "Frequency Options of SYSCLK with Respect to Memory Bus Speeds."
3	01/2009	• [Section 4.6, "Platform Frequency Requirements for PCI-Express and Serial RapidIO." Changed minimum frequency equation to be 527 MHz for PCI x8. • In Table 5, added note 7. • Section 4.5, "Platform to FIFO Restrictions." Changed platform clock frequency to 4.2. • Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics." Added MII after GMII and add 'or 2.5 V' after 3.3 V. • In Table 23, modified table title to include GMII, MII, RMII, and TBI. • In Table 24 and Table 25, changed clock period minimum to 5.3. • In Table 25, added a note. • In Table 26, Table 27, Table 28, Table 29, and Table 30, removed subtitle from table title. • In Table 30 and Figure 15, changed all instances of PMA to TSEC*n*. • In Section 8.2.5, "TBI Single-Clock Mode AC Specifications." Replaced first paragraph. • In Table 34, Table 35, Figure 18, and Figure 20, changed all instances of REF_CLK to TSEC*n*_TX_CLK. • In Table 36, changed all instances of OV_{DD} to LV_{DD}/TV_{DD}. • In Table 37, "MII Management AC Timing Specifications," changed MDC minimum clock pulse width high from 32 to 48 ns. • Added new section, Section 16, "High-Speed Serial Interfaces (HSSI)." • Section 16.1, "DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK." Added new paragraph. • Section 17.1, "DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK." Added new paragraph. • Added information to Figure 63, both in figure and in note. • Section 22.3, "Decoupling Recommendations." Modified the recommendation. • Table 87, "Part Numbering Nomenclature." In Silicon Version column added Ver. 2.1.2.

Table 88. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	04/2008	• Removed 1:1 support on Table 82, “e500 Core to CCB Clock Ratio.” • Removed MDM from Table 18, “DDR SDRAM Input AC Timing Specifications.” MDM is an Output. • Figure 57, “PLL Power Supply Filter Circuit with PLAT Pins” (AVDD_PLAT). • Figure 58, “PLL Power Supply Filter Circuit with CORE Pins” (AVDD_CORE). • Split Figure 59, “PLL Power Supply Filter Circuit with PCI/LBIU Pins,” (formerly called just “PLL Power Supply Filter Circuit”) into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	• Adjusted maximum SYSCLK frequency down in Table 5, “SYSCLK AC Timing Specifications” per device erratum GEN-13. • Clarified notes to Table 6, “EC_GTX_CLK125 AC Timing Specifications.” • Added Section 4.4, “PCI/PCI-X Reference Clock Timing.” • Clarified descriptions and added PCI/PCI-X to Table 9, “PLL Lock Times.” • Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, “DDR and DDR2 SDRAM.” • Clarified Note 4 of Table 19, “DDR SDRAM Output AC Timing Specifications.” • Clarified the reference clock used in Section 7.2, “DUART AC Electrical Specifications.” • Corrected V_{IH}(min) in Table 22, “GMII, MII, RMII, and TBI DC Electrical Characteristics.” • Corrected V_{IL}(max) in Table 23, “GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics.” • Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. • Corrected V_{IH}(min) in Table 36, “MII Management DC Electrical Characteristics.” • Corrected t_{MDC}(min) in Table 37, “MII Management AC Timing Specifications.” • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKH2}$, $t_{LBIXKH1}$, and $t_{LBIXKH2}$ in Table 40, “Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled” and Table 40, “Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled.” • Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKL2}$, $t_{LBIXKH1}$, and $t_{LBIXKL2}$ in Table 42, “Local Bus Timing Parameters—PLL Bypassed.” Note that $t_{LBIVKL2}$ and $t_{LBIXKL2}$ were previously labeled $t_{LBIVKH2}$ and $t_{LBIXKH2}$. • Added LUPWAIT signal to Figure 23, “Local Bus Signals (PLL Enabled)” and Figure 24, “Local Bus Signals (PLL Bypass Mode).” • Added $\overline{\text{LGTA}}$ signal to Figure 25, Figure 26, Figure 27 and Figure 28. • Corrected LUPWAIT assertion in Figure 26 and Figure 28. • Clarified the PCI reference clock in Section 15.2, “PCI/PCI-X AC Electrical Specifications” • Added Section 17.1, “Package Parameters.” • Added PBGA thermal information in Section 21.2, “Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid.” • Updated.” • Updated Table 87, “Part Numbering Nomenclature.”
0	07/2007	• Initial Release