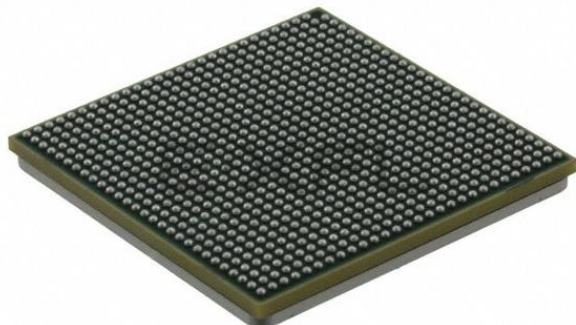




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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8548epxavhd

- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)

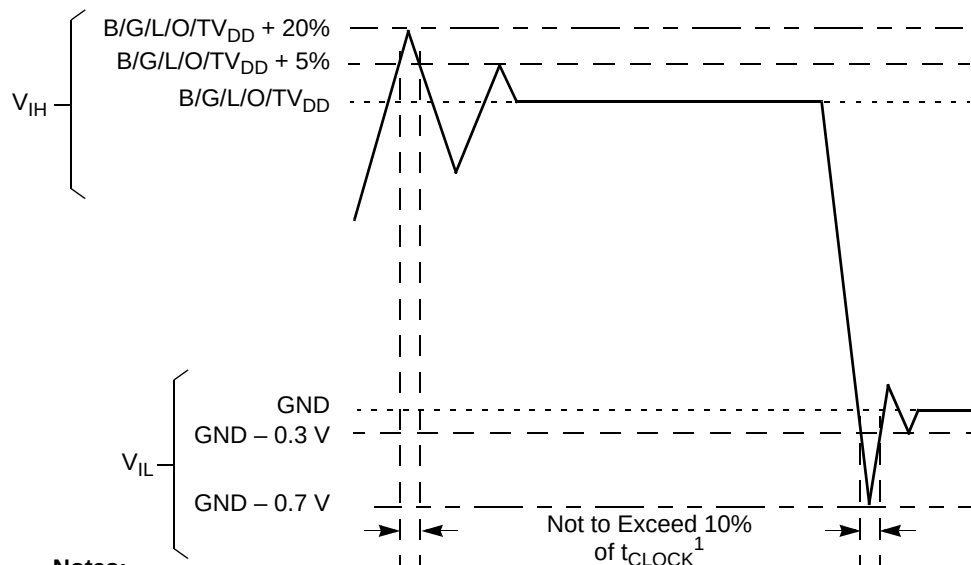
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Junction temperature range	T_j	0 to 105	°C	—

Notes:

1. This voltage is the input to the filter discussed in [Section 22.2, “PLL Power Supply Filtering,”](#) and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

The following figure shows the undershoot and overshoot voltages at the interfaces of this device.

**Notes:**

1. t_{CLOCK} refers to the clock period associated with the respective interface:
 For I²C and JTAG, t_{CLOCK} references SYSCLK.
 For DDR, t_{CLOCK} references MCLK.
 For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
 For LBIU, t_{CLOCK} references LCLK.
 For PCI, t_{CLOCK} references PCIn_CLK or SYSCLK.
 For SerDes, t_{CLOCK} references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3).

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.1 V. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in [Table 2](#). The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

3 Power Characteristics

The estimated typical power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in the following table.

Table 4. Device Power Dissipation

CCB Frequency ¹	Core Frequency	SLEEP ²	Typical-65 ³	Typical-105 ⁴	Maximum ⁵	Unit
400	800	2.7	4.6	7.5	8.1	W
	1000	2.7	5.0	7.9	8.5	W
	1200	2.7	5.4	8.3	8.9	
500	1500	11.5	13.6	16.5	18.6	W
533	1333	6.2	7.9	10.8	12.8	W

Notes:

1. CCB frequency is the SoC platform frequency, which corresponds to the DDR data rate.
2. SLEEP is based on $V_{DD} = 1.1\text{ V}$, $T_j = 65^\circ\text{C}$.
3. Typical-65 is based on $V_{DD} = 1.1\text{ V}$, $T_j = 65^\circ\text{C}$, running Dhrystone.
4. Typical-105 is based on $V_{DD} = 1.1\text{ V}$, $T_j = 105^\circ\text{C}$, running Dhrystone.
5. Maximum is based on $V_{DD} = 1.1\text{ V}$, $T_j = 105^\circ\text{C}$, running a smoke test.

4.3 eTSEC Gigabit Reference Clock Timing

The following table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the device.

Table 6. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t_{G125R}, t_{G125F}	—	—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125L}	45 47	—	55 53	%	2, 3

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TV_{DD} = 2.5 V, and from 0.6 and 2.7 V for L/TV_{DD} = 3.3 V.
2. Timing is guaranteed by design and characterization.
3. EC_GTX_CLK125 is used to generate the GTX clock TSEC_n_GTX_CLK for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the TSEC_n_GTX_CLK. See [Section 8.2.6, “RGMII and RTBI AC Timing Specifications,”](#) for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-x controller is not the SYCLK input, but instead the PCIn_CLK. The following table provides the PCI/PCI-X reference clock AC timing specifications for the device.

Table 7. PCIn_CLK AC Timing Specifications

At recommended operating conditions (see [Table 2](#)) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
PCIn_CLK frequency	f_{PCICLK}	16	—	133	MHz	—
PCIn_CLK cycle time	t_{PCICLK}	7.5	—	60	ns	—
PCIn_CLK rise and fall time	t_{PCIKH}, t_{PCIKL}	0.6	1.0	2.1	ns	1, 2
PCIn_CLK duty cycle	$t_{PCIKHKL}/t_{PCICLK}$	40	—	60	%	2

Notes:

1. Rise and fall times for SYCLK are measured at 0.6 and 2.7 V.
2. Timing is guaranteed by design and characterization.

Figure 8 shows the GMII transmit AC timing diagram.

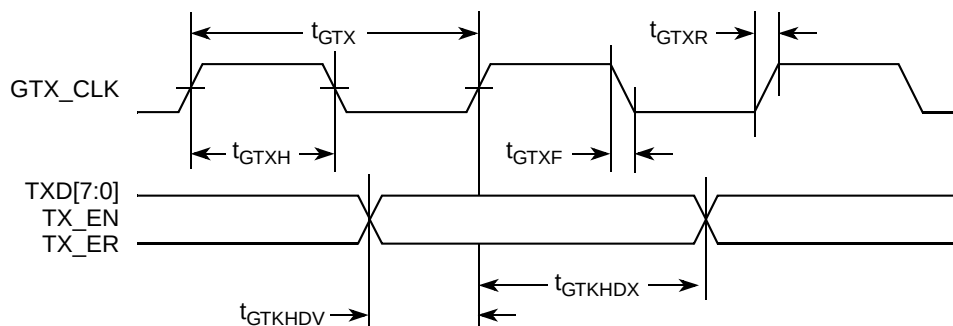


Figure 8. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 27. GMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	35	—	75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR}^2	—	—	1.0	ns
RX_CLK clock fall time (80%-20%)	t_{GRXF}^2	—	—	1.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 9 provides the AC test load for eTSEC.

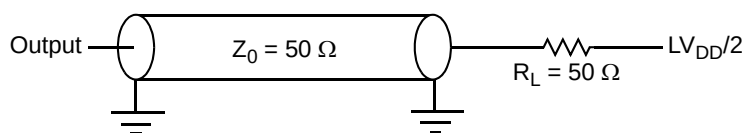


Figure 9. eTSEC AC Test Load

Figure 15 shows the TBI receive AC timing diagram.

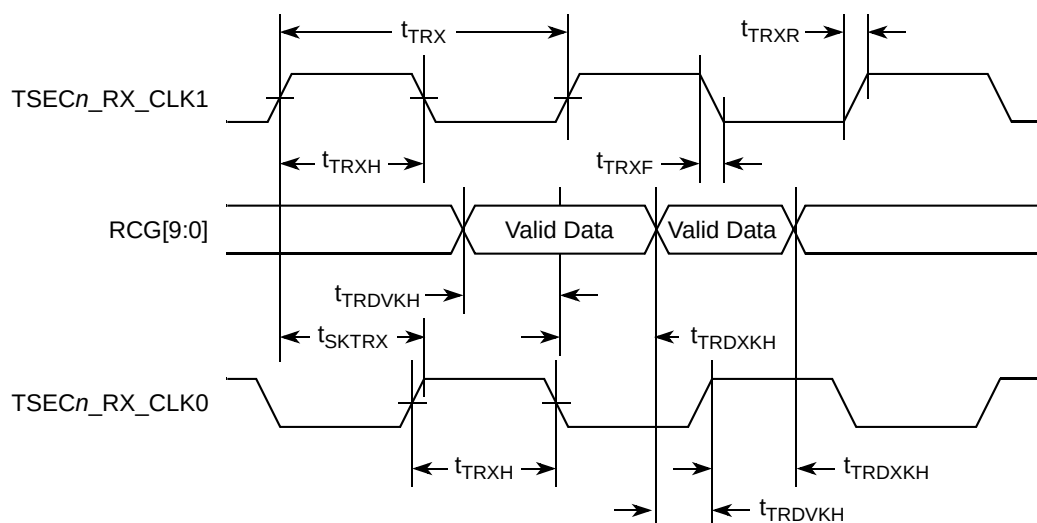


Figure 15. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSECn_RX_CLK pin (no receive clock is used on TSECn_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 32.

Table 32. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRRX}	7.5	8.0	8.5	ns
RX_CLK duty cycle	$t_{TRRH/TRRX}$	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	$t_{TRRDVKH}$	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	$t_{TRRDVKH}$	1.0	—	—	ns

Table 41 describes the timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Table 41. Local Bus Timing Parameters ($BV_{DD} = 2.5$ V)—PLL Enabled

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{LGTA}/UPWAIT$)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{LGTA}/LUPWAIT$)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{LGTA}/LUPWAIT$ input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.1	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.3	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.4	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.4	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Figure 22 provides the AC test load for the local bus.

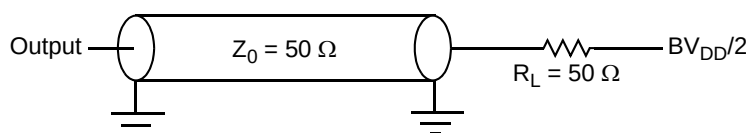


Figure 22. Local Bus AC Test Load

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz.
When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 23 through Figure 28 show the local bus signals.

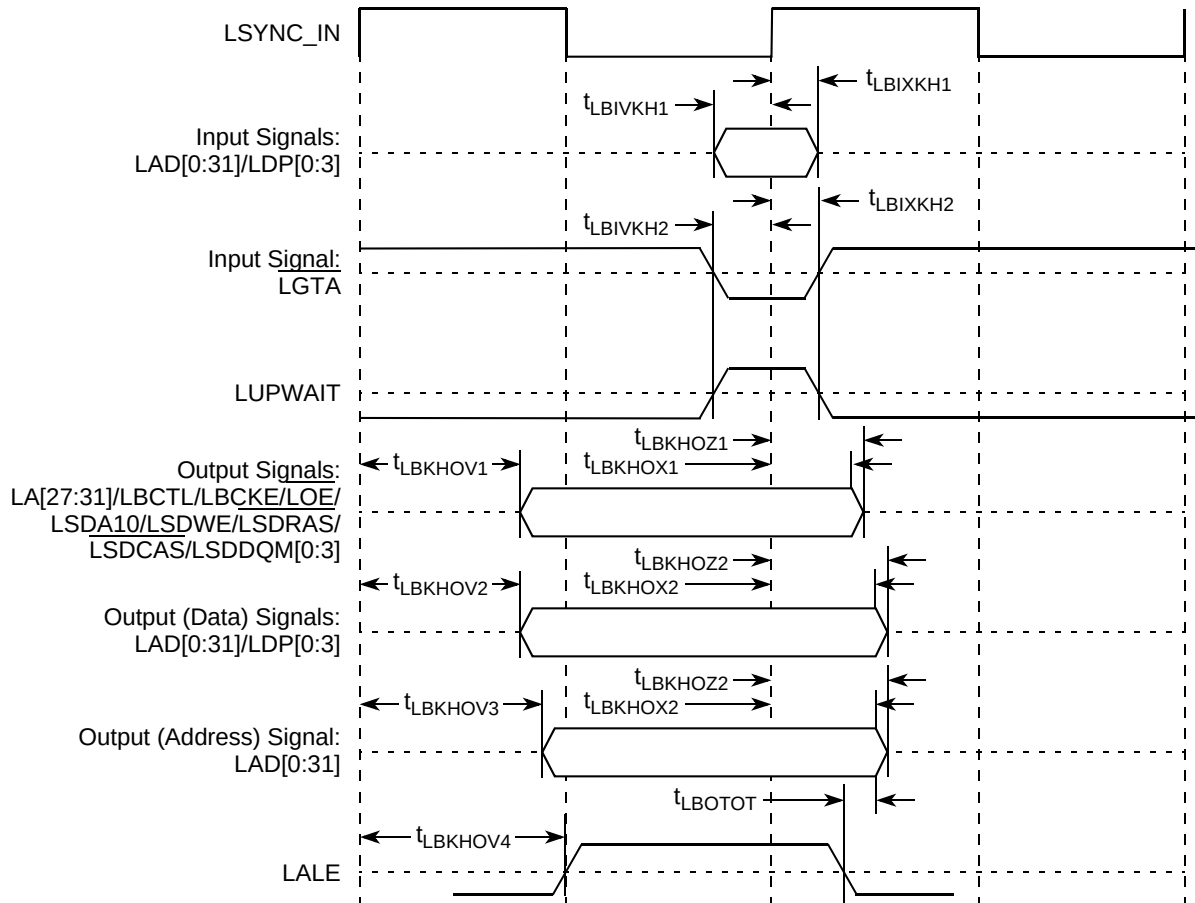


Figure 23. Local Bus Signals (PLL Enabled)

This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3\text{ V}$ with PLL disabled.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHK}	2.3	4.4	ns	8
Input setup to local bus clock (except $\overline{LGTA}/\overline{LUPWAIT}$)	$t_{LBIVKH1}$	6.2	—	ns	4, 5
$\overline{LGTA}/\overline{LUPWAIT}$ input setup to local bus clock	$t_{LBIVKL2}$	6.1	—	ns	4, 5
Input hold from local bus clock (except $\overline{LGTA}/\overline{LUPWAIT}$)	$t_{LBIXKH1}$	—1.8	—	ns	4, 5

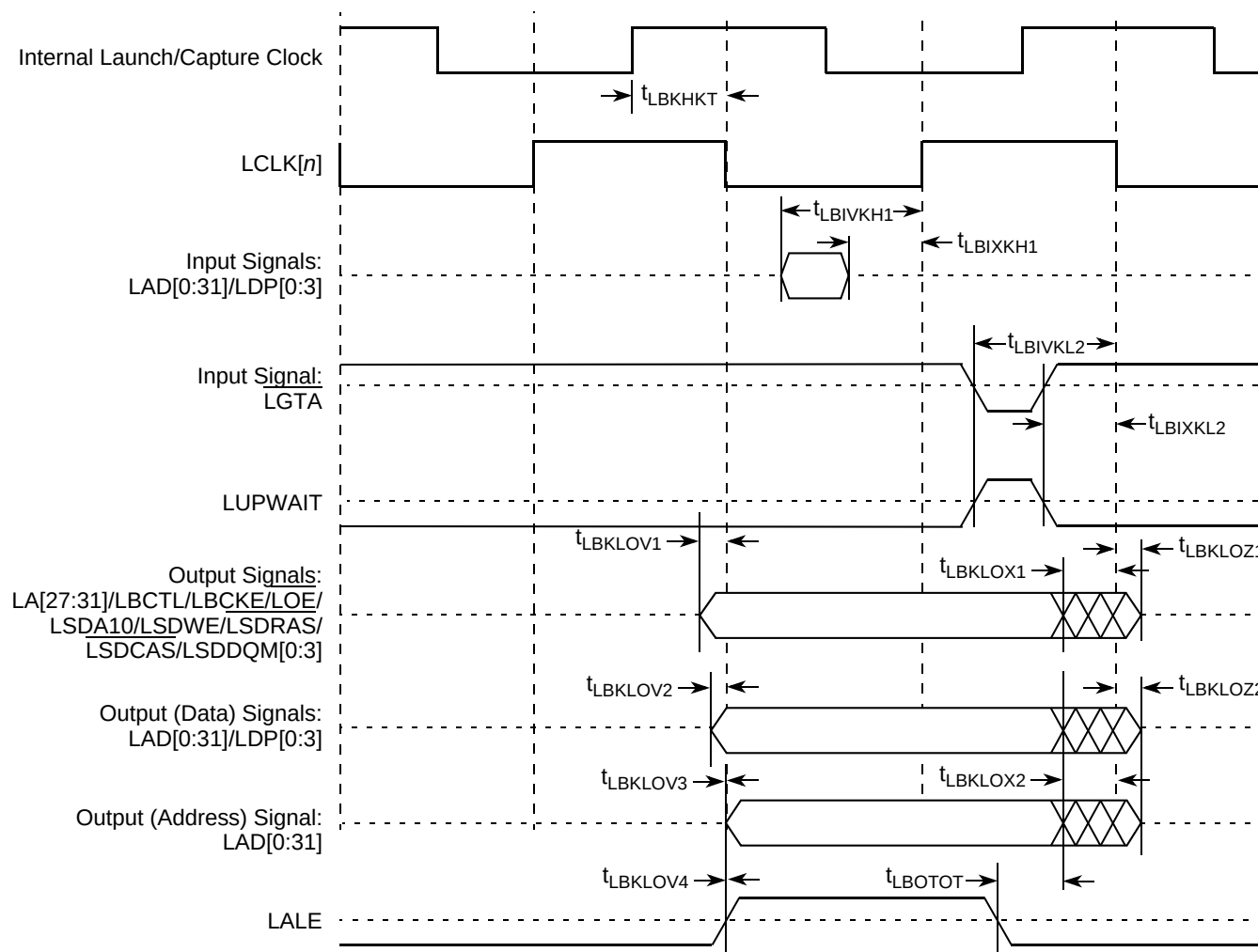


Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHK1} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of $\overline{LGTA}$ /LUPWAIT (which is captured on the rising edge of the internal clock).

Figure 34 shows the AC timing diagram for the I²C bus.

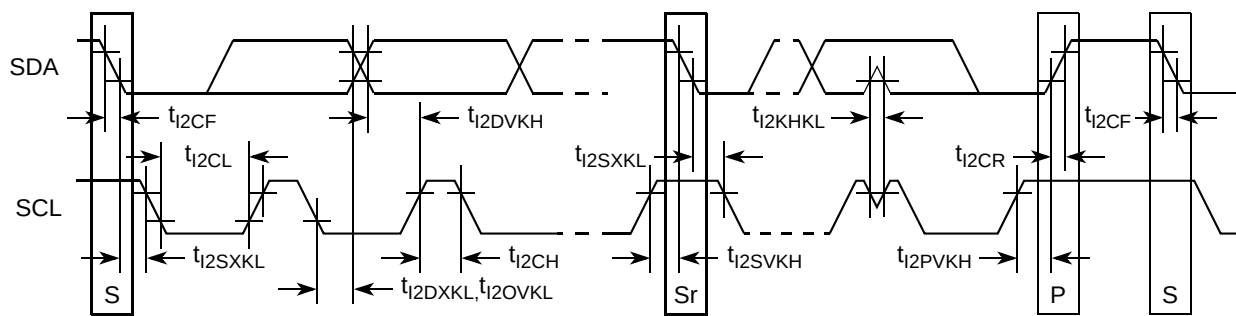


Figure 34. I²C Bus AC Timing Diagram

- The SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or $\overline{\text{SD_REF_CLK}}$) has a 50- Ω termination to SGND_SRDSn (xcorevss) followed by on-chip AC-coupling.
- The external reference clock driver must be able to drive this termination.
- The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range:
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (see the following bullet for more detail), since the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V ($0.4 \text{ V}/50 = 8 \text{ mA}$) while the minimum common mode input level is 0.1 V above SGND_SRDSn (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDSn (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement:
 - This requirement is described in detail in the following sections.

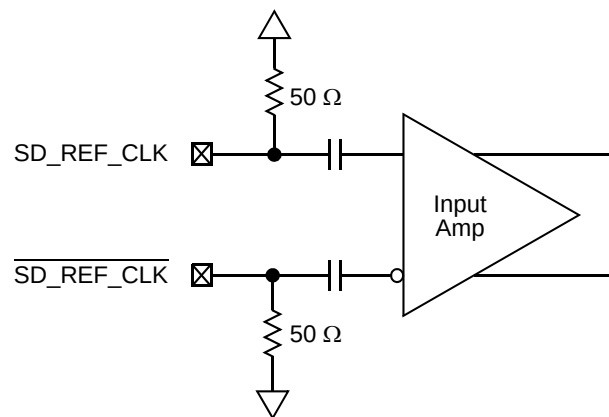


Figure 39. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below:

- Differential mode

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DC-CM}$	The TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	50	—		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
$RL_{TX-DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL_{TX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z_{TX-DC}	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC impedance during all states
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long- and short-run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to Serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

18.6 Transmitter Specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than:

- -10 dB for $(\text{baud frequency})/10 < \text{Freq}(f) < 625 \text{ MHz}$, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \leq \text{Freq}(f) \leq \text{baud frequency}$

The reference impedance for the differential return loss measurements is $100\text{-}\Omega$ resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Table 59. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	−0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	$\pm 100 \text{ ppm}$

Table 60. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	400	400	ps	±100 ppm

Table 61. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	500	1000	mVp-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	320	320	ps	±100 ppm

Table 62. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V_{DIFFPP}	800	1600	mVp-p	—
Deterministic jitter	J_D	—	0.17	UI p-p	—
Total jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit interval	UI	800	800	ps	±100 ppm

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	O	BV _{DD}	—
DMA				
DMA_DACK[0:1]	AD3, AE1	O	OV _{DD}	5, 9, 102
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	—
DMA_DDONE[0:1]	AD2, AD1	O	OV _{DD}	—
Programmable Interrupt Controller				
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	O	OV _{DD}	2, 4
Ethernet Management Interface				
EC_MDC	AB9	O	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	V11	I	LV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	O	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	O	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	T6	I	LV _{DD}	—
TSEC1_TX_EN	U9	O	LV _{DD}	30
TSEC1_TX_ER	T7	O	LV _{DD}	—

Table 72 provides the pin-out listing for the MPC8547E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 72. MPC8547E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 (One 64-Bit or One 32-Bit)				
PCI1_AD[63:32]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64	W15	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2
PCI1_FRAME	AE11	I/O	OV _{DD}	2
PCI1_IDSEL	AG9	I	OV _{DD}	—
PCI1_REQ64	AF14	I/O	OV _{DD}	2, 5, 10
PCI1_ACK64	V15	I/O	OV _{DD}	2
Reserved	AE28	—	—	2
Reserved	AD26	—	—	2
Reserved	AD25	—	—	2

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Local Bus Controller Interface				
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	—
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	—
LA[27]	H21	O	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	O	BV _{DD}	5, 7, 9
$\overline{\text{LCS}}[0:4]$	J25, C20, J24, G26, A26	O	BV _{DD}	—
$\overline{\text{LCS5/DMA_DREQ2}}$	D23	I/O	BV _{DD}	1
$\overline{\text{LCS6/DMA_DACK2}}$	G20	O	BV _{DD}	1
$\overline{\text{LCS7/DMA_DDONE2}}$	E21	O	BV _{DD}	1
$\overline{\text{LWE0/LBS0/LSDDQM}}[0]$	G25	O	BV _{DD}	5, 9
$\overline{\text{LWE1/LBS1/LSDDQM}}[1]$	C23	O	BV _{DD}	5, 9
$\overline{\text{LWE2/LBS2/LSDDQM}}[2]$	J21	O	BV _{DD}	5, 9
$\overline{\text{LWE3/LBS3/LSDDQM}}[3]$	A24	O	BV _{DD}	5, 9
LALE	H24	O	BV _{DD}	5, 8, 9
LBCTL	G27	O	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	O	BV _{DD}	5, 9
LGPL1/ $\overline{\text{LSDWE}}$	G22	O	BV _{DD}	5, 9
LGPL2/ $\overline{\text{LOE/LSDRAS}}$	B27	O	BV _{DD}	5, 8, 9
LGPL3/ $\overline{\text{LSDCAS}}$	F24	O	BV _{DD}	5, 9
LGPL4/ $\overline{\text{LGT\AA/LUPWAIT/LPBSE}}$	H23	I/O	BV _{DD}	—
LGPL5	E26	O	BV _{DD}	5, 9
LCKE	E24	O	BV _{DD}	—
LCLK[0:2]	E23, D24, H22	O	BV _{DD}	—
LSYNC_IN	F27	I	BV _{DD}	—
LSYNC_OUT	F28	O	BV _{DD}	—
DMA				
$\overline{\text{DMA_DACK}}[0:1]$	AD3, AE1	O	OV _{DD}	5, 9, 107
$\overline{\text{DMA_DREQ}}[0:1]$	AD4, AE2	I	OV _{DD}	—
$\overline{\text{DMA_DDONE}}[0:1]$	AD2, AD1	O	OV _{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH16	I	OV _{DD}	—
$\overline{\text{MCP}}$	AG19	I	OV _{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
JTAG				
TCK	AG28	I	OV _{DD}	—
TDI	AH28	I	OV _{DD}	12
TDO	AF28	O	OV _{DD}	—
TMS	AH27	I	OV _{DD}	12
TRST	AH23	I	OV _{DD}	12
DFT				
L1_TSTCLK	AC25	I	OV _{DD}	25
L2_TSTCLK	AE22	I	OV _{DD}	25
LSSD_MODE	AH20	I	OV _{DD}	25
TEST_SEL	AH14	I	OV _{DD}	109
Thermal Management				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
Power Management				
ASLEEP	AH18	O	OV _{DD}	9, 19, 29
Power and Ground Signals				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}	—
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	—

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200 Ω ($\pm 1\%$) to GND	—
SD_IMP_CAL_TX	AB26	I	100 Ω ($\pm 1\%$) to GND	—
SD_PLL_TPA	U26	O	AVDD_SRDS	24

Note: All note references in this table use the same numbers as those for [Table 71](#). See [Table 71](#) for the meanings of these notes.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

COP_TDO	1	2	NC
COP_TDI	3	4	$\overline{\text{COP_TRST}}$
COP_RUN/STOP	5	6	COP_VDD_SENSE
COP_TCK	7	8	$\overline{\text{COP_CHKSTP_IN}}$
COP_TMS	9	10	NC
$\overline{\text{COP_SRESET}}$	11	12	NC
$\overline{\text{COP_HRESET}}$	13	KEY No pin	
$\overline{\text{COP_CHKSTP_OUT}}$	15	16	GND

Figure 62. COP Connector Physical Pinout