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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548evjaqgd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview



Figure 1. Device Block Diagram

1.1 Key Features

The following list provides an overview of the device feature set:

- High-performance 32-bit core built on Power Architecture® technology.
 - 32-Kbyte L1 instruction cache and 32-Kbyte L1 data cache with parity protection. Caches can be locked entirely or on a per-line basis, with separate locking for instructions and data.
 - Signal-processing engine (SPE) APU (auxiliary processing unit). Provides an extensive instruction set for vector (64-bit) integer and fractional operations. These instructions use both the upper and lower words of the 64-bit GPRs as they are defined by the SPE APU.
 - Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
 - 36-bit real addressing
 - Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
 - Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte to 4-Gbyte page sizes.
 - Enhanced hardware and software debug support

- Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four controllers designed to comply with IEEE Std. 802.3[®], 802.3^u, 802.3^x, 802.3^z, 802.3^{ac}, and 802.3^{ab}
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations. See Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics," for more information.
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2[™], PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1TM virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound frames
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses

Overview

- Single inbound doorbell message structure
- Facility to accept port-write messages
- PCI Express interface
 - PCI Express 1.0a compatible
 - Supports x8,x4,x2, and x1 link widths
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Traffic class 0 only
 - Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
 - 8 PCI Express
 - 4 PCI Express and 4 serial RapidIO
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the eight counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- JTAG boundary scan, designed to comply with IEEE Std. 1149.1TM

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the device. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

The following table provides the absolute maximum ratings.

Table 1. Absolute	Maximum	Ratings	1
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	Characteristic	Symbol	Max Value	Unit	Notes
Core supply vo	bltage	V _{DD}	-0.3 to 1.21	V	—
PLL supply vol	tage	AV _{DD}	-0.3 to 1.21	V	—
Core power su	pply for SerDes transceivers	SV _{DD}	-0.3 to 1.21	V	—
Pad power sup	oply for SerDes transceivers	XV _{DD}	-0.3 to 1.21	V	—
DDR and DDR	2 DRAM I/O voltage	GV _{DD}	-0.3 to 2.75 -0.3 to 1.98	V	2
Three-speed E	thernet I/O voltage	LV _{DD} (for eTSEC1 and eTSEC2)	-0.3 to 3.63 -0.3 to 2.75	V	
		TV _{DD} (for eTSEC3 and eTSEC4)	-0.3 to 3.63 -0.3 to 2.75		3
PCI/PCI-X, DUART, system control and power management, I ² C, Ethernet MII management, and JTAG I/O voltage		OV _{DD}	-0.3 to 3.63	V	_
Local bus I/O voltage		BV _{DD}	-0.3 to 3.63 -0.3 to 2.75	V	—
Input voltage	DDR/DDR2 DRAM signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	4
	DDR/DDR2 DRAM reference	MV _{REF}	-0.3 to (GV _{DD} /2 + 0.3)	V	—
	Three-speed Ethernet I/O signals	LV _{IN} TV _{IN}	-0.3 to (LV _{DD} + 0.3) -0.3 to (TV _{DD} + 0.3)	V	4
	Local bus signals	BV _{IN}	-0.3 to (BV _{DD} + 0.3)	_	—
	DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	4
	PCI/PCI-X	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	4

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that $GV_{DD}(typ) = 2.5 \text{ V}$ for DDR SDRAM, and $GV_{DD}(typ) = 1.8 \text{ V}$ for DDR2 SDRAM.

6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	—
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{ОН}	-13.4	—	mA	—
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	—

Table 11. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM V_{DD} at all times.

2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} , and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail must track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

This table provides the DDR2 I/O capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 12. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[<i>n</i>]/MCK[<i>n</i>] crossing	t _{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t _{DDKHAS}	1.48 1.95 2.40		ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t ddkhax	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCS	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCX	1.48 1.95 2.40		ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	^t DDKHDS, ^t DDKLDS	538 700 900	 	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	^t ddkhdx, ^t ddkldx	538 700 900		ps	5
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5 imes t_{MCK}$ + 0.6	ns	6

DDR and DDR2 SDRAM

Table 19. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKHME}	-0.6	0.6	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- 2. All MCK/MCK referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the MPC8548E PowerQUICC III Integrated Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe must be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[*n*] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

NOTE

For the ADDR/CMD setup and hold specifications in Table 19, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 3 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).



Enhanced Three-Speed Ethernet (eTSEC)

Figure 10 shows the GMII receive AC timing diagram.



Figure 10. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

fable 2	28.	MII	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX} ²	_	400	_	ns
TX_CLK clock period 100 Mbps	t _{MTX}		40	_	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t _{MTXR} ²	1.0	_	4.0	ns
TX_CLK data clock fall (80%–20%)	t _{MTXF} ²	1.0		4.0	ns

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

2. Guaranteed by design.

Enhanced Three-Speed Ethernet (eTSEC)

Figure 13 shows the MII receive AC timing diagram.



Figure 13. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 30	. TBI	Transmit	AC	Timing	Specifications
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TCG[9:0] setup time GTX_CLK going high	t _{TTKHDV}	2.0	_	—	ns
TCG[9:0] hold time from GTX_CLK going high	t _{TTKHDX}	1.0	_	—	ns
GTX_CLK rise (20%–80%)	t _{TTXR} ²	_	_	1.0	ns
GTX_CLK fall time (80%–20%)	t _{TTXF} ²	_	_	1.0	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. Guaranteed by design.

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	3.13	3.47	V
Output high voltage ($OV_{DD} = Min, I_{OH} = -1.0 mA$)	V _{OH}	2.10	OV _{DD} + 0.3	V
Output low voltage (OV _{DD} =Min, I _{OL} = 1.0 mA)	V _{OL}	GND	0.50	V
Input high voltage	V _{IH}	2.0	—	V
Input low voltage	V _{IL}	—	0.90	V
Input high current ($OV_{DD} = Max, V_{IN}^{1} = 2.1 V$)	I _{IH}	—	40	μA
Input low current ($OV_{DD} = Max, V_{IN} = 0.5 V$)	I _{IL}	-600	—	μΑ

Table 36. MII Management DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t _{MDC}	120.5		1389	ns	—
MDC clock pulse width high	t _{MDCH}	32		—	ns	—
MDC to MDIO valid	t _{MDKHDV}	$16 \times t_{CCB}$		—	ns	5
MDC to MDIO delay	t _{MDKHDX}	(16 × t _{CCB} × 8) – 3		$(16 \times t_{\rm CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t _{MDDVKH}	5		—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0		—	ns	—
MDC rise time	t _{MDCR}	_	_	10	ns	4

Local Bus



Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).

14 GP_{OUT}/GP_{IN}

This section describes the DC and AC electrical specifications for the GP_{OUT}/GP_{IN} bus of the device.

14.1 GP_{OUT}/GP_{IN} Electrical Characteristics

Table 47 and Table 48 provide the DC electrical characteristics for the GP_{OUT} interface.

Parameter	Symbol	Min	Мах	Unit
Supply voltage 3.3 V	BV _{DD}	3.13	3.47	V
High-level output voltage ($BV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	BV _{DD} – 0.2	_	V
Low-level output voltage (BV _{DD} = min, I _{OL} = 2 mA)	V _{OL}	_	0.2	V

 Table 47. GP_{OUT} DC Electrical Characteristics (3.3 V DC)

 Table 48. GP_{OUT} DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level output voltage (BV _{DD} = min, I _{OH} = −1 mA)	V _{OH}	2.0	BV _{DD} + 0.3	V
Low-level output voltage (BV _{DD} min, I _{OL} = 1 mA)	V _{OL}	GND – 0.3	0.4	V

Table 49 and Table 50 provide the DC electrical characteristics for the GP_{IN} interface.

Table 49. GP_{IN} DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 3.3 V	BV _{DD}	3.13	3.47	V
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	I _{IN}	—	±5	μΑ

Note:

1. The symbol $\mathsf{BV}_{\mathsf{IN}}$, in this case, represents the $\mathsf{BV}_{\mathsf{IN}}$ symbol referenced in Table 1.

PCI/PCI-X

Figure 36 shows the PCI/PCI-X input AC timing conditions.



Figure 36. PCI/PCI-X Input AC Timing Measurement Conditions

Figure 37 shows the PCI/PCI-X output AC timing conditions.





Table 53 provides the PCI-X AC timing specifications at 66 MHz.

	Table 53	. PCI-X AC	Timing	Specifications	at 66	MHz
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Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV	_	3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7		ns	1, 10
SYSCLK to output high impedance	t _{PCKHOZ}	-	7	ns	1, 4, 8, 11
Input setup time to SYSCLK	t _{PCIVKH}	1.7	_	ns	3, 5
Input hold time from SYSCLK	t _{PCIXKH}	0.5	_	ns	10
REQ64 to HRESET setup time	t _{PCRVRH}	10	_	clocks	11
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	11
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	9, 11
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10	_	clocks	11

Table 53. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 11

Notes:

- 1. See the timing measurement conditions in the PCI-X 1.0a Specification.
- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
- 8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI-X 1.0a Specification.

10.Guaranteed by characterization.

11.Guaranteed by design.

This table provides the PCI-X AC timing specifications at 133 MHz. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV		3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7	_	ns	1, 11
SYSCLK to output high impedance	t _{PCKHOZ}		7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t _{PCIVKH}	1.2	_	ns	3, 5, 9, 11
Input hold time from SYSCLK	t _{PCIXKH}	0.5	_	ns	11
REQ64 to HRESET setup time	t _{PCRVRH}	10	_	clocks	12
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	12
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	10, 12
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10	_	clocks	12

Table 54. PCI-X AC Timing Specifications at 133 MHz

18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long- and short-run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to Serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

18.6 Transmitter Specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than:

- -10 dB for (baud frequency)/10 < Freq(f) < 625 MHz, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \le \text{Freq}(f) \le \text{baud}$ frequency

The reference impedance for the differential return loss measurements is $100-\Omega$ resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Characteristic	Symbol	Range		Unit	Notos
Characteristic	Symbol	Min	Max	Unit	NOIES
Output voltage	Vo	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic jitter	J _D	_	0.17	UI p-p	_
Total jitter	J _T	_	0.35	UI p-p	_
Multiple output skew	S _{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 59. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Package Description

Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
Thr	ee-Speed Ethernet Controller (Gigabit Ethe	rnet 2)					
TSEC2 RXDI7:01	P2. R2. N1. N2. P3. M2. M1. N3		LVpp	_			
TSEC2 TXD[7:0]	N9, N10, P8, N7, R9, N5, R8, N6	0		5, 9, 33			
	P1						
	R6			20			
TSEC2 GTX CLK	P6	0		20			
TSEC2 BX CLK	NA						
	P5						
TSEC2 BX ER	R1						
	P10						
	P7			20			
	P10	0		5 0 22			
Three Speed Ethernet Controller (Cignitis Ethernet 2)							
				5 0 00			
		0		5, 9, 29			
	¥1, VV3, VV5, VV4	1					
ISEC3_GIX_CLK	W8	0					
TSEC3_RX_CLK	W2		TV _{DD}	—			
TSEC3_RX_DV	W1		TV _{DD}				
TSEC3_RX_ER	Y2		TV _{DD}	—			
TSEC3_TX_CLK	V10	I	TV _{DD}	—			
TSEC3_TX_EN	V9	0	TV _{DD}	30			
Thr	ee-Speed Ethernet Controller (Gigabit Ethe	rnet 4)					
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	1, 5, 9, 29			
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	1			
TSEC4_GTX_CLK	AA5	0	TV _{DD}	—			
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV _{DD}	1			
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV _{DD}	1, 31			
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV _{DD}	1, 30			
· · · ·	DUART		•	•			
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—			
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—			
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—			
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	—			

Table 71. MPC8548E Pinout Listing (continued)

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes				
	I ² C interface			•				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27				
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27				
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27				
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27				
	SerDes			•				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}					
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—				
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}	—				
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}	—				
SD_PLL_TPD	U28	0	XV _{DD}	24				
SD_REF_CLK	T28	I	XV _{DD}	3				
SD_REF_CLK	T27	I	XV _{DD}	3				
Reserved	AC1, AC3	—	—	2				
Reserved	M26, V28	_	_	32				
Reserved	M25, V27	—	_	34				
Reserved	M20, M21, T22, T23	—	—	38				
	General-Purpose Output							
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—				
	System Control							
HRESET	AG17	I	OV _{DD}	_				
HRESET_REQ	AG16	0	OV _{DD}	29				
SRESET	AG20	I	OV _{DD}					
CKSTP_IN	AA9	I	OV _{DD}	—				
CKSTP_OUT	AA8	0	OV _{DD}	2, 4				
Debug								
TRIG_IN	AB2	I	OV _{DD}	—				
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29				
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9				
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29				
MDVAL	AE5	0	OV _{DD}	6				
CLK_OUT	AE21	0	OV _{DD}	11				

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	—
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	—
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 1)	•	•
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	Т6	I	LV _{DD}	—
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	T7	0	LV _{DD}	—
GPIN[0:7]	P2, R2, N1, N2, P3, M2, M1, N3	I	LV _{DD}	103
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	0	LV _{DD}	—
cfg_dram_type0/GPOUT6	R8	0	LV _{DD}	5, 9
GPOUT7	N6	0	LV _{DD}	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4			105

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
TDO	AF28	0	OV _{DD}	—		
TMS	AH27	I	OV _{DD}	12		
TRST	AH23	I	OV _{DD}	12		
DFT						
L1_TSTCLK	AC25	I	OV _{DD}	25		
L2_TSTCLK	AE22	I	OV _{DD}	25		
LSSD_MODE	AH20	I	OV_{DD}	25		
TEST_SEL	AH14	I	OV _{DD}	25		
Thermal Management						
THERM0	AG1	—	_	14		
THERM1	AH1	_	_	14		
Power Management						
ASLEEP	AH18	0	OV _{DD}	9, 19, 29		
Power and Ground Signals						
GND	 A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27 					
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}			
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	_		
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}			