



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
PowerPC e500
1 Core, 32-Bit
1.0GHz
Signal Processing; SPE, Security; SEC
DDR, DDR2, SDRAM
No
-
10/100/1000Mbps (4)
-
-
1.8V, 2.5V, 3.3V
0°C ~ 105°C (TA)
Cryptography, Random Number Generator
783-BBGA, FCBGA
783-FCBGA (29x29)
https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548evtaqgb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

 Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 512-Kbyte L2 cache/SRAM
 - Flexible configuration.
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and Flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be Flash cleared separately.
 - SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.
 - Three inbound windows plus a configuration window on PCI/PCI-X and PCI Express
 - Four inbound windows plus a default window on RapidIO[™]
 - Four outbound windows plus default translation for PCI/PCI-X and PCI Express
 - Eight outbound windows plus default translation for RapidIO with segmentation and sub-segmentation support
- DDR/DDR2 memory controller
 - Programmable timing supporting DDR and DDR2 SDRAM
 - 64-bit data interface
 - Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes
 - DRAM chip configurations from 64 Mbits to 4 Gbits with ×8/×16 data ports
 - Full ECC support
 - Page mode support
 - Up to 16 simultaneous open pages for DDR

- Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Four controllers designed to comply with IEEE Std. 802.3[®], 802.3^u, 802.3^x, 802.3^z, 802.3^{ac}, and 802.3^{ab}
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
 - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
 - Flexible configuration for multiple PHY interface configurations. See Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics," for more information.
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2[™], PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1TM virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound frames
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses

Overview

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO[™] interface unit
 - Supports RapidIO[™] Interconnect Specification, Revision 1.2
 - Both $1 \times$ and $4 \times$ LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC)."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	3.13	3.47	V
Output high voltage ($OV_{DD} = Min, I_{OH} = -1.0 mA$)	V _{OH}	2.10	OV _{DD} + 0.3	V
Output low voltage (OV _{DD} =Min, I _{OL} = 1.0 mA)	V _{OL}	GND	0.50	V
Input high voltage	V _{IH}	2.0	—	V
Input low voltage	V _{IL}	—	0.90	V
Input high current ($OV_{DD} = Max, V_{IN}^{1} = 2.1 V$)	I _{IH}	—	40	μA
Input low current ($OV_{DD} = Max, V_{IN} = 0.5 V$)	I _{IL}	-600	—	μΑ

Table 36. MII Management DC Electrical Characteristics

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	0.72	2.5	8.3	MHz	2, 3, 4
MDC period	t _{MDC}	t _{MDC} 120.5		1389	ns	—
MDC clock pulse width high	t _{MDCH}	32		—	ns	—
MDC to MDIO valid	t _{MDKHDV}	$16 \times t_{CCB}$		—	ns	5
MDC to MDIO delay	t _{MDKHDX}	(16 × t _{CCB} × 8) – 3		$(16 \times t_{\rm CCB} \times 8) + 3$	ns	5
MDIO to MDC setup time	t _{MDDVKH}	5		—	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0		—	ns	—
MDC rise time	t _{MDCR}	_	_	10	ns	4

Local Bus



Figure 24. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[*n*] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).

Local Bus



Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)



Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Parameter	Symbol	Min	Мах	Unit
Supply voltage 2.5 V	BV _{DD}	2.37	2.63	V
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.7	V
Input current ($BV_{IN}^{1} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	Ι _{ΙΗ}	_	10	μΑ

Table 50. GP_{IN} DC Electrical Characteristics (2.5 V DC)

Note:

1. The symbol $\mathsf{BV}_{\mathsf{IN}}$ in this case, represents the $\mathsf{BV}_{\mathsf{IN}}$ symbol referenced in Table 1.

15 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the device.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 51. PCI/PCI-X DC Electrical Characteristics¹

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	2
High-level output voltage ($OV_{DD} = min, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V _{OL}	—	0.4	V	—

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the PCI 2.2 Local Bus Specifications.

2. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for synchronous mode and by PCIn_CLK when it is configured for asynchronous mode.

This table provides the PCI AC timing specifications at 66 MHz.

Table 52.	. PCI AC	Timing	Specifications at	66 MH
-----------	----------	--------	-------------------	-------

Parameter	Symbol ¹	Min	Мах	Unit	Notes
CLK to output valid	t _{PCKHOV}	—	6.0	ns	2, 3
Output hold from CLK	t _{PCKHOX}	2.0	_	ns	2, 10
CLK to output high impedance	t _{PCKHOZ}	_	14	ns	2, 4, 11
Input setup to CLK	^t PCIVKH	3.0	_	ns	2, 5, 10
Input hold from CLK	t _{PCIXKH}	0	_	ns	2, 5, 10
REQ64 to HRESET ⁹ setup time	t _{PCRVRH}	$10 imes t_{SYS}$	_	clocks	6, 7, 11
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	7, 11
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	8, 11

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI/PCI-X timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI/PCI-X timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of SYSCLK or PCI_CLK*n* to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.
- 6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 20, "Clocking."
- 7. The setup and hold time is with respect to the rising edge of HRESET.
- 8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
- 9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
- 10. Guaranteed by characterization.
- 11.Guaranteed by design.

Figure 35 provides the AC test load for PCI and PCI-X.



Table 53. PCI-X AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol	Min	Max	Unit	Notes
HRESET to PCI-X initialization pattern hold time	t _{PCRHIX}	0	50	ns	6, 11

Notes:

- 1. See the timing measurement conditions in the PCI-X 1.0a Specification.
- 2. Minimum times are measured at the package pin (not the test point). Maximum times are measured with the test point and load circuit.
- 3. Setup time for point-to-point signals applies to REQ and GNT only. All other signals are bused.
- 4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time.
- 6. Maximum value is also limited by delay to the first transaction (time for HRESET high to first configuration access, t_{PCRHFV}). The PCI-X initialization pattern control signals after the rising edge of HRESET must be negated no later than two clocks before the first FRAME and must be floated no later than one clock before FRAME is asserted.
- 7. A PCI-X device is permitted to have the minimum values shown for t_{PCKHOV} and t_{CYC} only in PCI-X mode. In conventional mode, the device must meet the requirements specified in PCI 2.2 for the appropriate clock frequency.
- 8. Device must meet this specification independent of how many outputs switch simultaneously.

9. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the PCI-X 1.0a Specification.

10.Guaranteed by characterization.

11.Guaranteed by design.

This table provides the PCI-X AC timing specifications at 133 MHz. Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

Parameter	Symbol	Min	Max	Unit	Notes
SYSCLK to signal valid delay	^t PCKHOV		3.8	ns	1, 2, 3, 7, 8
Output hold from SYSCLK	t _{PCKHOX}	0.7	_	ns	1, 11
SYSCLK to output high impedance	t _{PCKHOZ}		7	ns	1, 4, 8, 12
Input setup time to SYSCLK	t _{PCIVKH}	1.2	_	ns	3, 5, 9, 11
Input hold time from SYSCLK	t _{PCIXKH}	0.5	_	ns	11
REQ64 to HRESET setup time	t _{PCRVRH}	10	_	clocks	12
HRESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	12
HRESET high to first FRAME assertion	t _{PCRHFV}	10	_	clocks	10, 12
PCI-X initialization pattern to HRESET setup time	^t PCIVRH	10	_	clocks	12

Table 54. PCI-X AC Timing Specifications at 133 MHz

High-Speed Serial Interfaces (HSSI)

- The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.
- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
 - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with SD_REF_CLK either left unconnected or tied to ground.
 - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DCor AC-coupled into the unused phase (SD_REF_CLK) through the same source impedance as the clock input (SD_REF_CLK) in use.



Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

PCI Express

Symbol	Parameter	Min	Nom	Max	Unit	Comments
V _{RX-CM-ACp}	AC peak common mode input voltage	_	_	150	mV	$\begin{split} & V_{RX\text{-}CM\text{-}ACp} = V_{RXD\text{+}} - V_{RXD\text{-}} /2 + V_{RX\text{-}CM\text{-}DC} \\ & V_{RX\text{-}CM\text{-}DC} = DC_{(avg)} \text{ of } V_{RX\text{-}D\text{+}} + V_{RX\text{-}D\text{-}} \div 2. \\ & See Note 2. \end{split}$
RL _{RX-DIFF}	Differential return loss	15	—	_	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. See Note 4.
RL _{RX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
Z _{RX-DIFF-DC}	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z _{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 \pm 20% tolerance). See Notes 2 and 5.
Z _{RX-HIGH-IMP-DC}	Powered down DC input impedance	200 k	—	_	Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
V _{RX-IDLE-DET-DIFFp-p}	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFF_{p-p}} = 2 \times V_{RX-D+} - V_{RX-D-} .$ Measured at the package pins of the receiver
T _{RX-IDLE-DET-DIFF-} ENTERTIME	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 57. Differential Receiver (RX) Input Specifications (continued)

Table 57. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
L _{TX-SKEW}	Total Skew			20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 50 must be used as the RX device when taking measurements (also see the receiver compliance eye diagram shown in Figure 49). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to $-{300 \text{ mV}}$ and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see Figure 50). Note: that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode Impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 50) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 50) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer must provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 49) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

PCI Express

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.



Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.



Figure 50. Compliance Test/Measurement Load

components are included in this requirement. The reference impedance for return loss measurements is $100-\Omega$ resistive for differential return loss and $25-\Omega$ resistive for common mode.

Characteristic	Symbol	Rai	Range		Notes
onaraoteristic	Cymbol	Min	Мах	onit	Notes
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver
Multiple input skew	S _{MI}	_	24	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	_	10 ⁻¹²	—	—
Unit interval	UI	800	800	ps	±100 ppm

Table 66	. Receiver	AC	Timing	Specification	ns—1.25 GBaud
----------	------------	----	--------	---------------	---------------

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Table 67. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notos	
Gharacteristic	Symbol	Min	Max	Unit	10163	
Differential input voltage	V _{IN}	200	1600	mVp-p	Measured at receiver	
Deterministic jitter tolerance	J _D	0.37	—	UI p-p	Measured at receiver	
Combined deterministic and random jitter tolerance	J _{DR}	0.55	—	UI p-p	Measured at receiver	
Total jitter tolerance ¹	J _T	0.65	—	UI p-p	Measured at receiver	
Multiple input skew	S _{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link	
Bit error rate	BER	—	10 ⁻¹²		—	
Unit interval	UI	400	400	ps	±100 ppm	

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

Serial RapidIO

802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

18.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12} . The eye pattern shall be measured with AC coupling and the compliance template centered at 0 V differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be $100-\Omega$ resistive $\pm 5\%$ differential to 2.5 GHz.

18.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter test pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

18.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ± 5% differential to 2.5 GHz.

18.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in Section 18.7, "Receiver Specifications," and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 54 and Table 69. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 18.7, "Receiver Specifications," is then added to the signal and the test load is replaced by the receiver being tested.

Table 71	. MPC8548E	Pinout Listing	(continued)
----------	------------	-----------------------	-------------

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
Clock						
RTC	AF16	I	OV _{DD}	—		
SYSCLK	AH17	I	OV _{DD}	—		
	JTAG					
ТСК	AG28	I	OV _{DD}	—		
TDI	AH28	I	OV _{DD}	12		
TDO	AF28	0	OV _{DD}	—		
TMS	AH27	ļ	OV _{DD}	12		
TRST	AH23	I	OV _{DD}	12		
	DFT					
L1_TSTCLK	AC25	I	OV _{DD}	25		
L2_TSTCLK	AE22	I	OV _{DD}	25		
LSSD_MODE	AH20	I	OV _{DD}	25		
TEST_SEL	AH14	I	OV _{DD}	25		
	Thermal Management					
THERM0	AG1	—	—	14		
THERM1	AH1	—	_	14		
	Power Management					
ASLEEP	AH18	0	OV _{DD}	9, 19, 29		
	Power and Ground Signals					
GND	 A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27 	_	_	_		
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}	—		

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MWE	E7	0	GV _{DD}	_
MCAS	H7	0	GV _{DD}	_
MRAS	L8	0	GV _{DD}	
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	_
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36
	Local Bus Controller Interface			
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV _{DD}	
LDP[0:3]	K21, C28, B26, B22	I/O	BV _{DD}	
LA[27]	H21	0	BV _{DD}	5, 9
LA[28:31]	H20, A27, D26, A28	0	BV _{DD}	5, 7, 9
LCS[0:4]	J25, C20, J24, G26, A26	0	BV _{DD}	_
LCS5/DMA_DREQ2	D23	I/O	BV _{DD}	1
LCS6/DMA_DACK2	G20	0	BV _{DD}	1
LCS7/DMA_DDONE2	E21	0	BV _{DD}	1
LWE0/LBS0/LSDDQM[0]	G25	0	BV _{DD}	5, 9
LWE1/LBS1/LSDDQM[1]	C23	0	BV _{DD}	5, 9
LWE2/LBS2/LSDDQM[2]	J21	0	BV _{DD}	5, 9
LWE3/LBS3/LSDDQM[3]	A24	0	BV _{DD}	5, 9
LALE	H24	0	BV _{DD}	5, 8, 9
LBCTL	G27	0	BV _{DD}	5, 8, 9
LGPL0/LSDA10	F23	0	BV _{DD}	5, 9
LGPL1/LSDWE	G22	0	BV _{DD}	5, 9
LGPL2/LOE/LSDRAS	B27	0	BV _{DD}	5, 8, 9
LGPL3/LSDCAS	F24	0	BV _{DD}	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV _{DD}	
LGPL5	E26	0	BV _{DD}	5, 9
LCKE	E24	0	BV _{DD}	
LCLK[0:2]	E23, D24, H22	0	BV _{DD}	_

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
JTAG							
ТСК	AG28	I	OV _{DD}	_			
TDI	AH28	I	OV _{DD}	12			
TDO	AF28	0	OV _{DD}	—			
TMS	AH27	I	OV _{DD}	12			
TRST	AH23	I	OV _{DD}	12			
	DFT	I					
L1_TSTCLK	AC25	I	OV _{DD}	25			
L2_TSTCLK	AE22	I	OV _{DD}	25			
LSSD_MODE	AH20	I	OV _{DD}	25			
TEST_SEL	AH14	I	OV _{DD}	109			
	Thermal Management						
THERM0	AG1		—	14			
THERM1	AH1		—	14			
	Power Management	I					
ASLEEP	AH18	0	OV _{DD}	9, 19, 29			
	Power and Ground Signals						
GND	 A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27 	_					
OV _{DD}	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV _{DD}	—			
LV _{DD}	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV _{DD}	_			

System Design Information

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

22.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 63 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 62, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 62 is common to all known emulators.

22.9.1 Termination of Unused Signals

Freescale recommends the following connections, when the JTAG interface and COP header are not used:

• TRST must be tied to HRESET through a 0 k Ω isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system