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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548hxatg

- Single inbound doorbell message structure
- Facility to accept port-write messages
- PCI Express interface
 - PCI Express 1.0a compatible
 - Supports x8,x4,x2, and x1 link widths
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Traffic class 0 only
 - Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
 - 8 PCI Express
 - 4 PCI Express and 4 serial RapidIO
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the eight counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- JTAG boundary scan, designed to comply with IEEE Std. 1149.1™

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

Figure 13 shows the MII receive AC timing diagram.

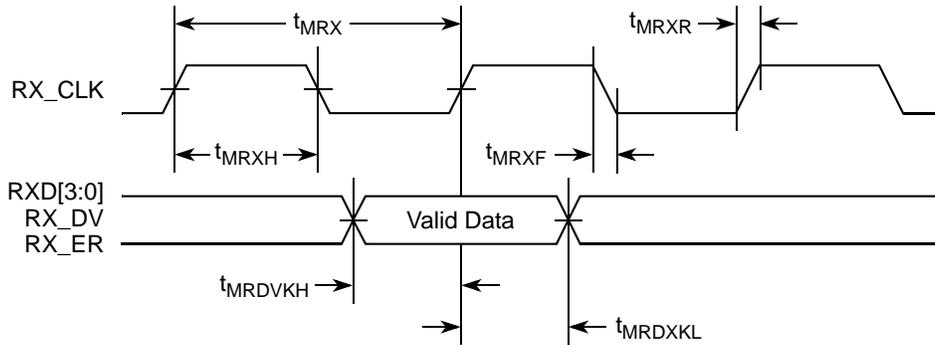


Figure 13. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 30. TBI Transmit AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX}	1.0	—	—	ns
GTX_CLK rise (20%–80%)	t_{TTXR}^2	—	—	1.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF}^2	—	—	1.0	ns

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Guaranteed by design.

Figure 19 provides the AC test load for eTSEC.

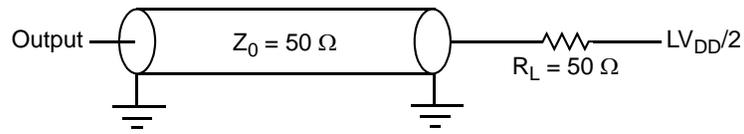


Figure 19. eTSEC AC Test Load

Figure 20 shows the RMII receive AC timing diagram.

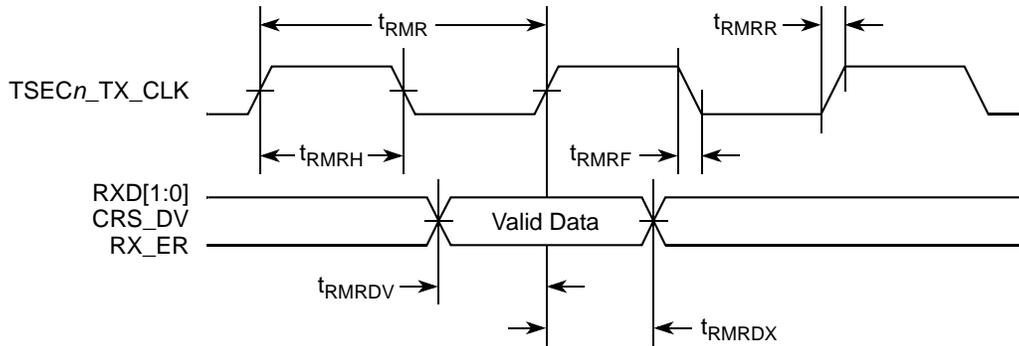


Figure 20. RMII Receive AC Timing Diagram

Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is $3.3\text{ V} \pm 5\%$.

Parameter	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—		10	ns	4

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f_{CCB}). The actual ECn_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) \div (2 \times Frequency Divider determined by MIIMCFG[MgmtClk] encoding selection). For example, if MIIMCFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, $f_{MDC} = 533 \div (2 \times 4 \times 8) = 533 \div 64 = 8.3\text{ MHz}$. That is, for a system running at a particular platform frequency (f_{CCB}), the ECn_MDC output clock frequency can be programmed between maximum $f_{MDC} = f_{CCB} \div 64$ and minimum $f_{MDC} = f_{CCB} \div 448$. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual for more detail.
- The maximum ECn_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
- Guaranteed by design.
- t_{CCB} is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.

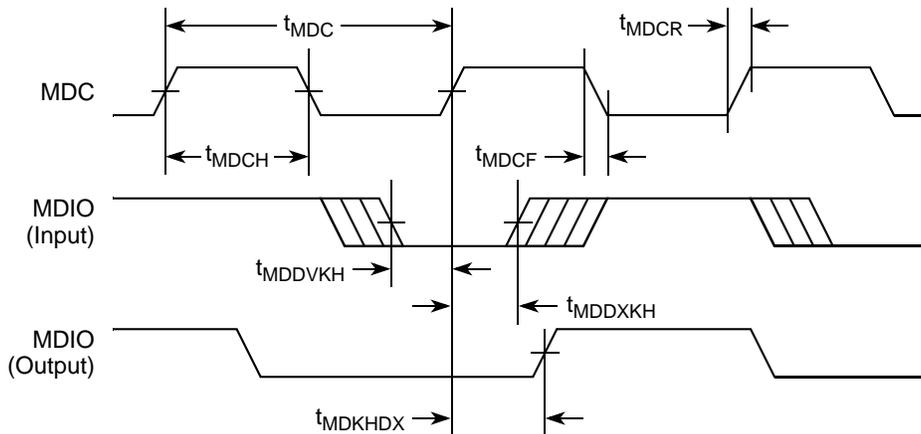


Figure 21. MII Management Interface Timing Diagram

of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SD_TX} + V_{\overline{SD_TX}} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset.

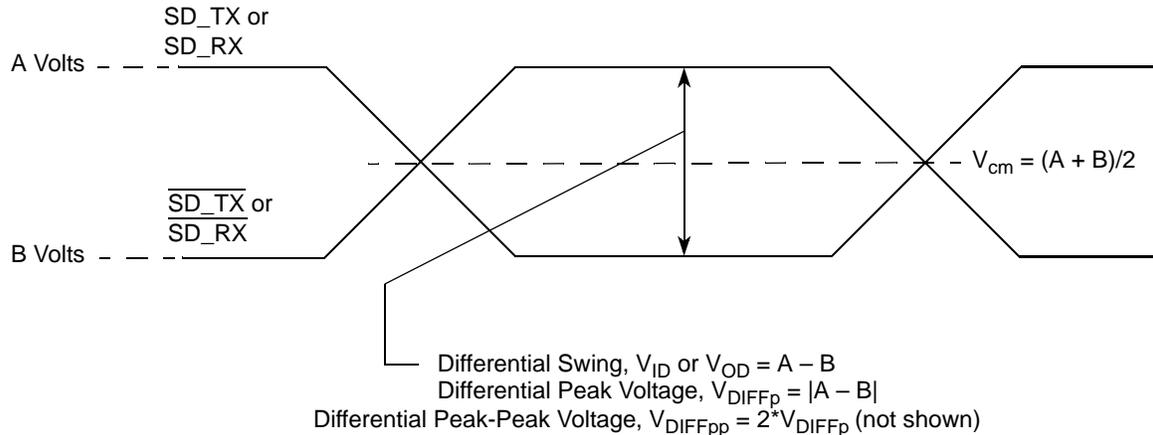


Figure 38. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and \overline{TD} , has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or \overline{TD}) is 500 mVp-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFpp}) is 1000 mVp-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and $\overline{SD_REF_CLK}$ for PCI Express and serial RapidIO.

The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 39 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes Reference clock receiver reference circuit structure:

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.

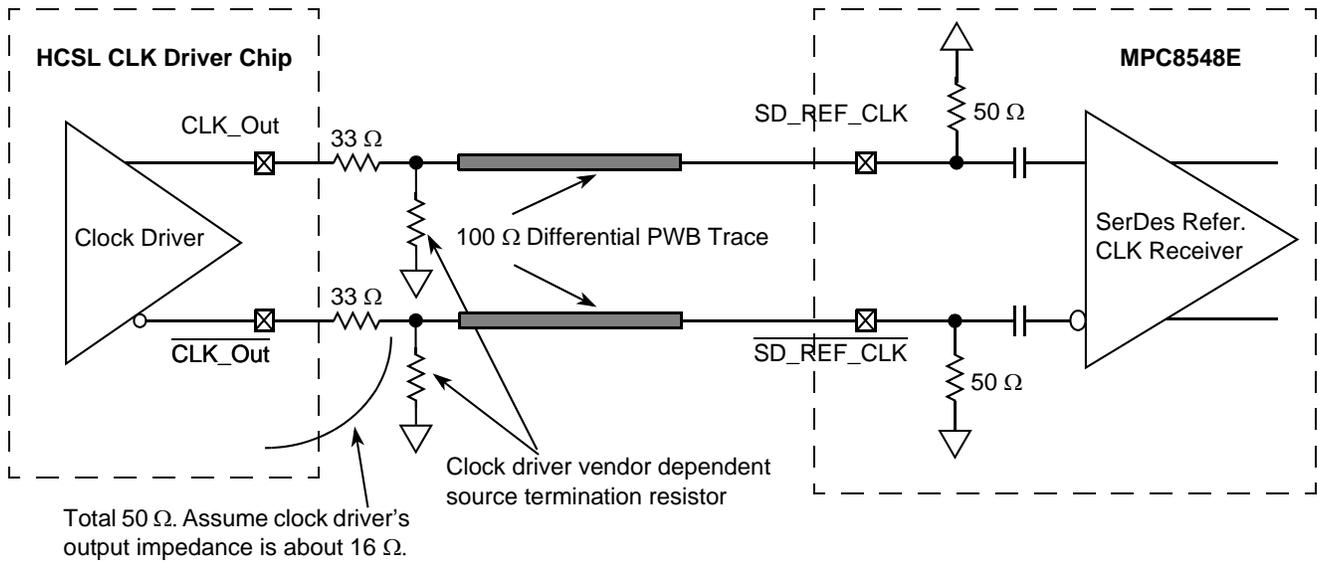


Figure 43. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

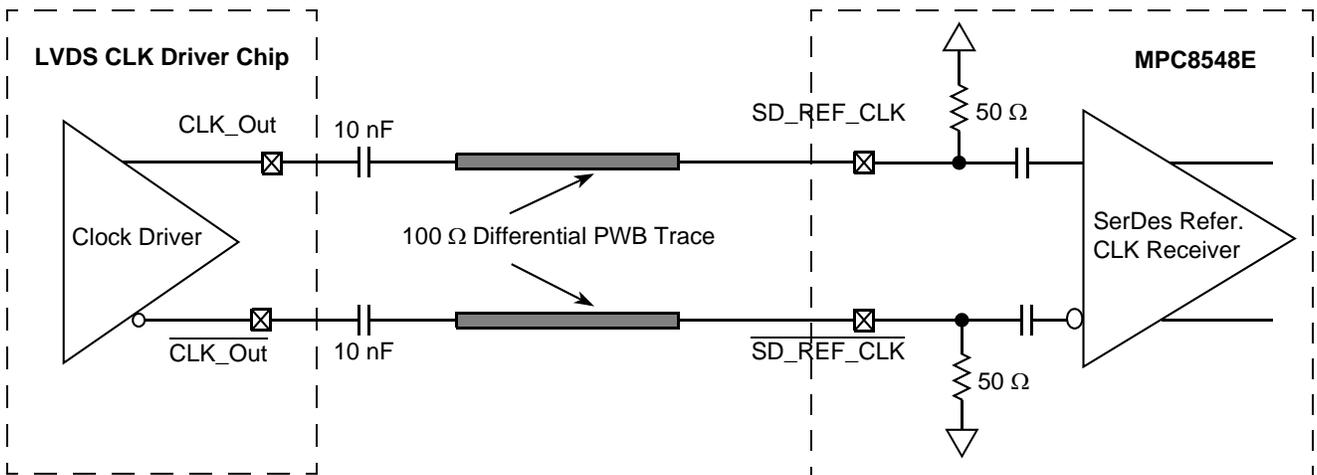


Figure 44. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior

Table 56. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $. See Note 2.
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D- TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(V_{TXD+} + V_{TXD-} /2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$. See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of dc common mode voltage during L0 and electrical idle	0	—	100	mV	$ V_{TX-CM-DC}(\text{during L0}) + V_{TX-CM-Idle-DC}(\text{during electrical idle}) \leq 100$ mV $V_{TX-CM-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [L0] $V_{TX-CM-Idle-DC} = \text{DC}_{(avg)}$ of $ V_{TX-D+} + V_{TX-D-} /2$ [electrical idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D-	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25$ mV $V_{TX-CM-DC-D+} = \text{DC}_{(avg)}$ of $ V_{TX-D+} $ $V_{TX-CM-DC-D-} = \text{DC}_{(avg)}$ of $ V_{TX-D-} $. See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \leq 20$ mV. See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.

Table 56. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-DC-CM}$	The TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	50	—		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
$RL_{TX-DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL_{TX-CM}	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z_{TX-DC}	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC impedance during all states
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.

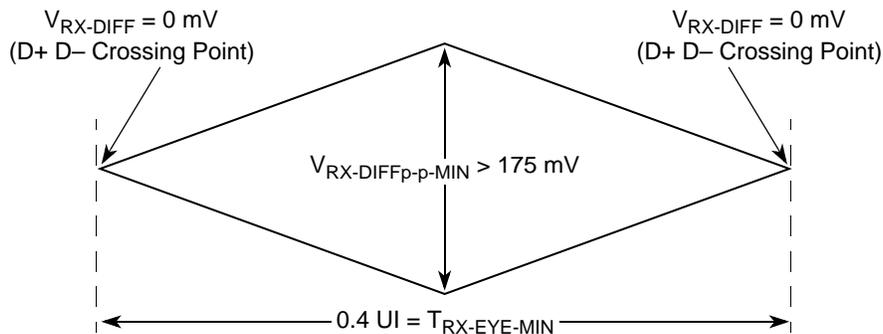


Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.

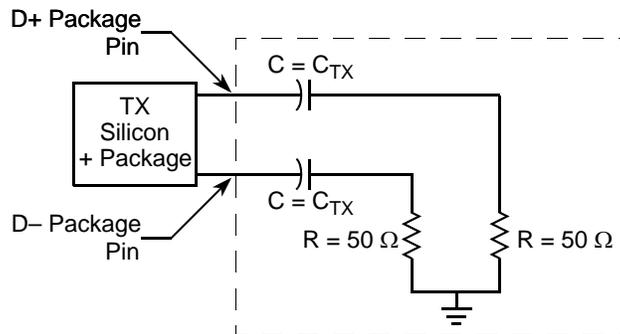


Figure 50. Compliance Test/Measurement Load

18.3 Signal Definitions

LP-serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 51 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A volts and B volts where $A > B$. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD, and $\overline{\text{RD}}$ each have a peak-to-peak swing of $A - B$ volts.
2. The differential output signal of the transmitter, V_{OD} , is defined as $V_{\text{TD}} - V_{\overline{\text{TD}}}$.
3. The differential input signal of the receiver, V_{ID} , is defined as $V_{\text{RD}} - V_{\overline{\text{RD}}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ volts.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is $A - B$ volts.
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A - B)$ volts.

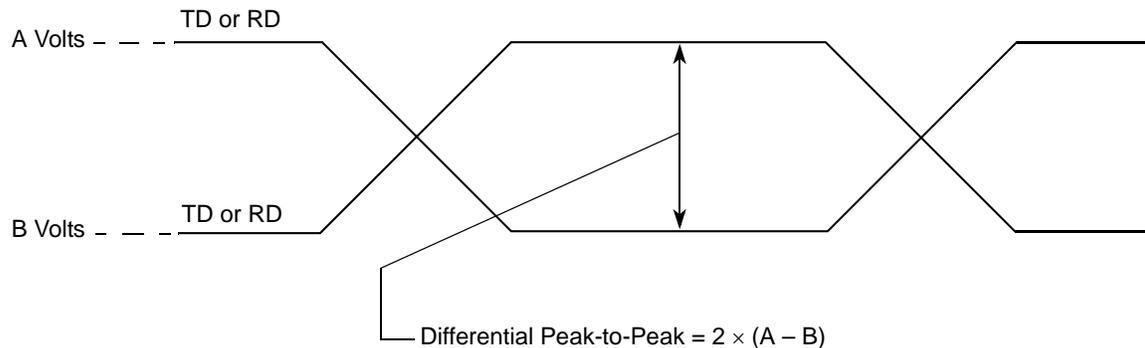


Figure 51. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mVp-p. The differential output signal ranges between 500 and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mVp-p.

18.4 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver. Effects such as inter-symbol interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
I²C interface				
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27
SerDes				
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV _{DD}	—
$\overline{\text{SD_RX}}[0:7]$	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV _{DD}	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV _{DD}	—
$\overline{\text{SD_TX}}[0:7]$	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV _{DD}	—
SD_PLL_TPD	U28	O	XV _{DD}	24
SD_REF_CLK	T28	I	XV _{DD}	3
$\overline{\text{SD_REF_CLK}}$	T27	I	XV _{DD}	3
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV _{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV _{DD}	—
$\overline{\text{HRESET_REQ}}$	AG16	O	OV _{DD}	29
$\overline{\text{SRESET}}$	AG20	I	OV _{DD}	—
$\overline{\text{CKSTP_IN}}$	AA9	I	OV _{DD}	—
$\overline{\text{CKSTP_OUT}}$	AA8	O	OV _{DD}	2, 4
Debug				
TRIG_IN	AB2	I	OV _{DD}	—
TRIG_OUT/READY/QUIESCE	AB1	O	OV _{DD}	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV _{DD}	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV _{DD}	6, 19, 29
MDVAL	AE5	O	OV _{DD}	6
CLK_OUT	AE21	O	OV _{DD}	11

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	L28	I	200Ω to GND	—
SD_IMP_CAL_TX	AB26	I	100Ω to GND	—
SD_PLL_TPA	U26	O	—	24

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5/DMA_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD} .
3. A valid clock must be provided at POR if $\text{TSEC4_TXD}[2]$ is set = 1.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of $\text{LA}[28:31]$ during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See [Section 20.2, "CCB/SYSCLK PLL Ratio."](#)
8. The value of LALE , LGPL2 , and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the [Section 20.3, "e500 Core PLL Ratio."](#)
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the $\text{V}_{\text{DD}}/\text{GND}$ planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor.
15. No connections must be made to these pins if they are not used.
16. These pins are not connected for any use.
17. PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins $\text{PCI_AD}[63:32]$ and $\text{PCI1_C_BE}[7:4]$).
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx flow control.
24. Do not connect.

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
$\overline{\text{MDQS}}$ [0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV _{DD}	—
MBA[0:2]	F7, J7, M11	O	GV _{DD}	—
$\overline{\text{MWE}}$	E7	O	GV _{DD}	—
$\overline{\text{MCAS}}$	H7	O	GV _{DD}	—
$\overline{\text{MRAS}}$	L8	O	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	O	GV _{DD}	11
$\overline{\text{MCS}}$ [0:3]	K8, J8, G8, F8	O	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV _{DD}	—
$\overline{\text{MCK}}$ [0:5]	J9, A15, G1, L9, B14, F2	O	GV _{DD}	—
MODT[0:3]	E6, K6, L7, M7	O	GV _{DD}	—
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV _{DD}	—
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	—
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	—
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV _{DD}	—
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV _{DD}	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V _{DD}	13
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A18	I Reference voltage signal for DDR	MVREF	—

Table 85. Package Thermal Characteristics for FC-PBGA (continued)

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-board	N/A	$R_{\theta JB}$	5	°C/W	3
Die junction-to-case	N/A	$R_{\theta JC}$	0.8	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.3 Heat Sink Solution

Every system application has different conditions that the thermal management solution must solve. As such, providing a recommended heat sink has not been found to be very useful. When a heat sink is chosen, give special consideration to the mounting technique. Mounting the heat sink to the printed-circuit board is the recommended procedure using a maximum of 10 lbs force (45 Newtons) perpendicular to the package and board. Clipping the heat sink to the package is not recommended.

22 System Design Information

This section provides electrical design recommendations for successful application of the device.

22.1 System Clocking

This device includes five PLLs, as follows:

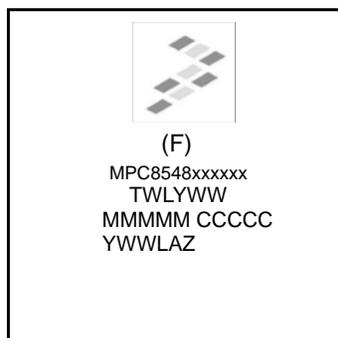
1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in [Section 20.2, “CCB/SYSCLK PLL Ratio.”](#)
2. The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in [Section 20.3, “e500 Core PLL Ratio.”](#)
3. The PCI PLL generates the clocking for the PCI bus.
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT} , AV_{DD_CORE} , AV_{DD_PCI} , AV_{DD_LBIU} , and AV_{DD_SRDS} , respectively). The AV_{DD}

23.2 Part Marking

Parts are marked as the example shown in [Figure 64](#).



Notes:

TWLYWW is final test traceability code.

MMMMM is 5 digit mask number.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

YWWLAZ is assembly traceability code.

Figure 64. Part Marking for CBGA and PBGA Device

24 Document Revision History

The following table provides a revision history for this hardware specification.

Table 88. Document Revision History

Rev. Number	Date	Substantive Change(s)
9	02/2012	<ul style="list-style-type: none"> Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. Removed Note from Section 5.1, "Power-On Ramp Rate". Changed the Table 10 title to "Power Supply Ramp Rate". Removed table 11. Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)"¹ from 4 and 25 to 2 and 10 respectively .
8	04/2011	<ul style="list-style-type: none"> Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET* assertion. Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information.
7	09/2010	<ul style="list-style-type: none"> In Table 37, "MII Management AC Timing Specifications, modified the fifth row from "MDC to MDIO delay tMDKHDX (16 × tptb_clk × 8) – 3 — (16 × tptb_clk × 8) + 3" to "MDC to MDIO delay tMDKHDX (16 × tCCB × 8) – 3 — (16 × tCCB × 8) + 3." Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes.
6	12/2009	<ul style="list-style-type: none"> In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. In Table 13 deleted ramp rate requirement for XVDD/SVDD. In Table 13 footnote 1 changed voltage range of concern from 0–400 mV to 20–500mV. In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins.
5	10/2009	<ul style="list-style-type: none"> In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX_CLK duty cycle. Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." Added a reference to Revision 2.1.2. Updated Table 55, "MII Management AC Timing Specifications." Added Section 5.1, "Power-On Ramp Rate."

Table 88. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
2	04/2008	<ul style="list-style-type: none"> Removed 1:1 support on Table 82, "e500 Core to CCB Clock Ratio." Removed MDM from Table 18, "DDR SDRAM Input AC Timing Specifications." MDM is an Output. Figure 57, "PLL Power Supply Filter Circuit with PLAT Pins" (AVDD_PLAT). Figure 58, "PLL Power Supply Filter Circuit with CORE Pins" (AVDD_CORE). Split Figure 59, "PLL Power Supply Filter Circuit with PCI/LBIU Pins," (formerly called just "PLL Power Supply Filter Circuit") into three figures: the original (now specific for AVDD_PCI/AVDD_LBIU) and two new ones.
1	10/2007	<ul style="list-style-type: none"> Adjusted maximum SYSCLK frequency down in Table 5, "SYSCLK AC Timing Specifications" per device erratum GEN-13. Clarified notes to Table 6, "EC_GTX_CLK125 AC Timing Specifications." Added Section 4.4, "PCI/PCI-X Reference Clock Timing." Clarified descriptions and added PCI/PCI-X to Table 9, "PLL Lock Times." Removed support for 266 and 200 Mbps data rates per device erratum GEN-13 in Section 6, "DDR and DDR2 SDRAM." Clarified Note 4 of Table 19, "DDR SDRAM Output AC Timing Specifications." Clarified the reference clock used in Section 7.2, "DUART AC Electrical Specifications." Corrected $V_{IH}(\text{min})$ in Table 22, "GMII, MII, RMII, and TBI DC Electrical Characteristics." Corrected $V_{IL}(\text{max})$ in Table 23, "GMII, MII, RMII, TBI, RGMII, RTBI, and FIFO DC Electrical Characteristics." Removed DC parameters from Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 32, Table 34, and Table 35. Corrected $V_{IH}(\text{min})$ in Table 36, "MII Management DC Electrical Characteristics." Corrected $t_{MDC}(\text{min})$ in Table 37, "MII Management AC Timing Specifications." Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKH2}$, $t_{LBIXKH1}$, and $t_{LBIXKH2}$ in Table 40, "Local Bus Timing Parameters ($BV_{DD} = 3.3 \text{ V}$)—PLL Enabled" and Table 40, "Local Bus Timing Parameters ($BV_{DD} = 2.5 \text{ V}$)—PLL Enabled." Updated parameter descriptions for $t_{LBIVKH1}$, $t_{LBIVKL2}$, $t_{LBIXKH1}$, and $t_{LBIXKL2}$ in Table 42, "Local Bus Timing Parameters—PLL Bypassed." Note that $t_{LBIVKL2}$ and $t_{LBIXKL2}$ were previously labeled $t_{LBIVKH2}$ and $t_{LBIXKH2}$. Added LUPWAIT signal to Figure 23, "Local Bus Signals (PLL Enabled)" and Figure 24, "Local Bus Signals (PLL Bypass Mode)." Added LGTA signal to Figure 25, Figure 26, Figure 27 and Figure 28. Corrected LUPWAIT assertion in Figure 26 and Figure 28. Clarified the PCI reference clock in Section 15.2, "PCI/PCI-X AC Electrical Specifications" Added Section 17.1, "Package Parameters." Added PBGA thermal information in Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid." Updated." Updated Table 87, "Part Numbering Nomenclature."
0	07/2007	<ul style="list-style-type: none"> Initial Release