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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8548pxaujb">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8548pxaujb</a>

- Up to 32 simultaneous open pages for DDR2
- Contiguous or discontiguous memory mapping
- Read-modify-write support for RapidIO atomic increment, decrement, set, and clear transactions
- Sleep mode support for self-refresh SDRAM
- On-die termination support when using DDR2
- Supports auto refreshing
- On-the-fly power management using CKE signal
- Registered DIMM support
- Fast memory access via JTAG port
- 2.5-V SSTL\_2 compatible I/O (1.8-V SSTL\_1.8 for DDR2)
- Support for battery-backed main memory
- Programmable interrupt controller (PIC)
  - Programming model is compliant with the OpenPIC architecture.
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts
  - Supports 4 message interrupts with 32-bit messages
  - Supports connection of an external interrupt controller such as the 8259 programmable interrupt controller
  - Four global high-resolution timers/counters that can generate interrupts
  - Supports a variety of other internal interrupt sources
  - Supports fully nested interrupt delivery
  - Interrupts can be routed to external pin for external processing.
  - Interrupts can be routed to the e500 core's standard or critical interrupt inputs.
  - Interrupt summary registers allow fast identification of interrupt source.
- Integrated security engine (SEC) optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
  - Four crypto-channels, each supporting multi-command descriptor chains
    - Dynamic assignment of crypto-execution units via an integrated controller
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
  - PKEU—public key execution unit
    - RSA and Diffie-Hellman; programmable field size up to 2048 bits
    - Elliptic curve cryptography with  $F_2^m$  and  $F(p)$  modes and programmable field size up to 511 bits
  - DEU—Data Encryption Standard execution unit
    - DES, 3DES
    - Two key (K1, K2) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES

- Dedicated single data rate SDRAM controller
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Four enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Four controllers designed to comply with IEEE Std. 802.3<sup>®</sup>, 802.3u, 802.3x, 802.3z, 802.3ac, and 802.3ab
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
    - 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - Flexible configuration for multiple PHY interface configurations. See [Section 8.1, “Enhanced Three-Speed Ethernet Controller \(eTSEC\) \(10/100/1Gb Mbps\)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics,”](#) for more information.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2<sup>™</sup>, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1<sup>™</sup> virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses

## 4 Input Clocks

This section discusses the timing for the input clocks.

### 4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

**Table 5. SYSCLK AC Timing Specifications**

At recommended operating conditions (see Table 2) with  $OV_{DD} = 3.3\text{ V} \pm 165\text{ mV}$ .

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	$f_{\text{SYSCLK}}$	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	$t_{\text{SYSCLK}}$	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	$t_{\text{KH}}, t_{\text{KL}}$	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	$t_{\text{KHK}}/t_{\text{SYSCLK}}$	40	—	60	%	3
SYSCLK jitter	—	—	—	$\pm 150$	ps	4, 5

**Notes:**

- Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, “CCB/SYSCLK PLL Ratio,” and Section 20.3, “e500 Core PLL Ratio,” for ratio settings.
- Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The SYSCLK driver’s closed loop jitter bandwidth must be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
- For spread spectrum clocking. Guidelines are +0% to –1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

### 4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is  $2 \times t_{\text{CCB}}$ , and minimum clock low time is  $2 \times t_{\text{CCB}}$ . There is no minimum RTC frequency; RTC may be grounded if not needed.

## 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the device. Note that  $GV_{DD}(\text{typ}) = 2.5 \text{ V}$  for DDR SDRAM, and  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$  for DDR2 SDRAM.

### 6.1 DDR SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM controller of the device when  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$ .

**Table 11. DDR2 SDRAM DC Electrical Characteristics for  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	$GV_{DD}$	1.71	1.89	V	1
I/O reference voltage	$MV_{REF}$	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2
I/O termination voltage	$V_{TT}$	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	$V_{IH}$	$MV_{REF} + 0.125$	$GV_{DD} + 0.3$	V	—
Input low voltage	$V_{IL}$	-0.3	$MV_{REF} - 0.125$	V	—
Output leakage current	$I_{OZ}$	-50	50	$\mu\text{A}$	4
Output high current ( $V_{OUT} = 1.420 \text{ V}$ )	$I_{OH}$	-13.4	—	mA	—
Output low current ( $V_{OUT} = 0.280 \text{ V}$ )	$I_{OL}$	13.4	—	mA	—

**Notes:**

- $GV_{DD}$  is expected to be within 50 mV of the DRAM  $V_{DD}$  at all times.
- $MV_{REF}$  is expected to be equal to  $0.5 \times GV_{DD}$ , and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $MV_{REF}$  may not exceed  $\pm 2\%$  of the DC value.
- $V_{TT}$  is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to  $MV_{REF}$ . This rail must track variations in the DC level of  $MV_{REF}$ .
- Output leakage is measured with all outputs disabled,  $0 \text{ V} \leq V_{OUT} \leq GV_{DD}$ .

This table provides the DDR2 I/O capacitance when  $GV_{DD}(\text{typ}) = 1.8 \text{ V}$ .

**Table 12. DDR2 SDRAM Capacitance for  $GV_{DD}(\text{typ})=1.8 \text{ V}$**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	$C_{IO}$	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{\text{DQS}}$	$C_{DIO}$	—	0.5	pF	1

**Note:**

- This parameter is sampled.  $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$ ,  $f = 1 \text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{OUT} = GV_{DD}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2 V.

## 6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface. The DDR controller supports both DDR1 and DDR2 memories. DDR1 is supported with the following AC timings at data rates of 333 MHz. DDR2 is supported with the following AC timings at data rates down to 333 MHz.

### 6.2.1 DDR SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR SDRAM when  $GV_{DD}(typ) = 1.8 V$ .

**Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface**

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit
AC input low voltage	$V_{IL}$	—	$MV_{REF} - 0.25$	V
AC input high voltage	$V_{IH}$	$MV_{REF} + 0.25$	—	V

Table 17 provides the input AC timing specifications for the DDR SDRAM when  $GV_{DD}(typ) = 2.5 V$ .

**Table 17. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface**

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	$V_{IL}$	—	$MV_{REF} - 0.31$	V
AC input high voltage	$V_{IH}$	$MV_{REF} + 0.31$	—	V

This table provides the input AC timing specifications for the DDR SDRAM interface.

**Table 18. DDR SDRAM Input AC Timing Specifications**

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	$t_{CISKEW}$			ps	1, 2
533 MHz		-300	300		
400 MHz		-365	365		
333 MHz		-390	390		

**Notes:**

- $t_{CISKEW}$  represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called  $t_{DISKEW}$ . This can be determined by the following equation:  $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$  where T is the clock period and  $abs(t_{CISKEW})$  is the absolute value of  $t_{CISKEW}$ .

## 14 GP<sub>OUT</sub>/GP<sub>IN</sub>

This section describes the DC and AC electrical specifications for the GP<sub>OUT</sub>/GP<sub>IN</sub> bus of the device.

### 14.1 GP<sub>OUT</sub>/GP<sub>IN</sub> Electrical Characteristics

Table 47 and Table 48 provide the DC electrical characteristics for the GP<sub>OUT</sub> interface.

**Table 47. GP<sub>OUT</sub> DC Electrical Characteristics (3.3 V DC)**

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	BV <sub>DD</sub>	3.13	3.47	V
High-level output voltage (BV <sub>DD</sub> = min, I <sub>OH</sub> = -2 mA)	V <sub>OH</sub>	BV <sub>DD</sub> - 0.2	—	V
Low-level output voltage (BV <sub>DD</sub> = min, I <sub>OL</sub> = 2 mA)	V <sub>OL</sub>	—	0.2	V

**Table 48. GP<sub>OUT</sub> DC Electrical Characteristics (2.5 V DC)**

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5 V	BV <sub>DD</sub>	2.37	2.63	V
High-level output voltage (BV <sub>DD</sub> = min, I <sub>OH</sub> = -1 mA)	V <sub>OH</sub>	2.0	BV <sub>DD</sub> + 0.3	V
Low-level output voltage (BV <sub>DD</sub> min, I <sub>OL</sub> = 1 mA)	V <sub>OL</sub>	GND - 0.3	0.4	V

Table 49 and Table 50 provide the DC electrical characteristics for the GP<sub>IN</sub> interface.

**Table 49. GP<sub>IN</sub> DC Electrical Characteristics (3.3 V DC)**

Parameter	Symbol	Min	Max	Unit
Supply voltage 3.3 V	BV <sub>DD</sub>	3.13	3.47	V
High-level input voltage	V <sub>IH</sub>	2	BV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
Input current (BV <sub>IN</sub> <sup>1</sup> = 0 V or BV <sub>IN</sub> = BV <sub>DD</sub> )	I <sub>IN</sub>	—	±5	μA

**Note:**

1. The symbol BV<sub>IN</sub>, in this case, represents the BV<sub>IN</sub> symbol referenced in Table 1.

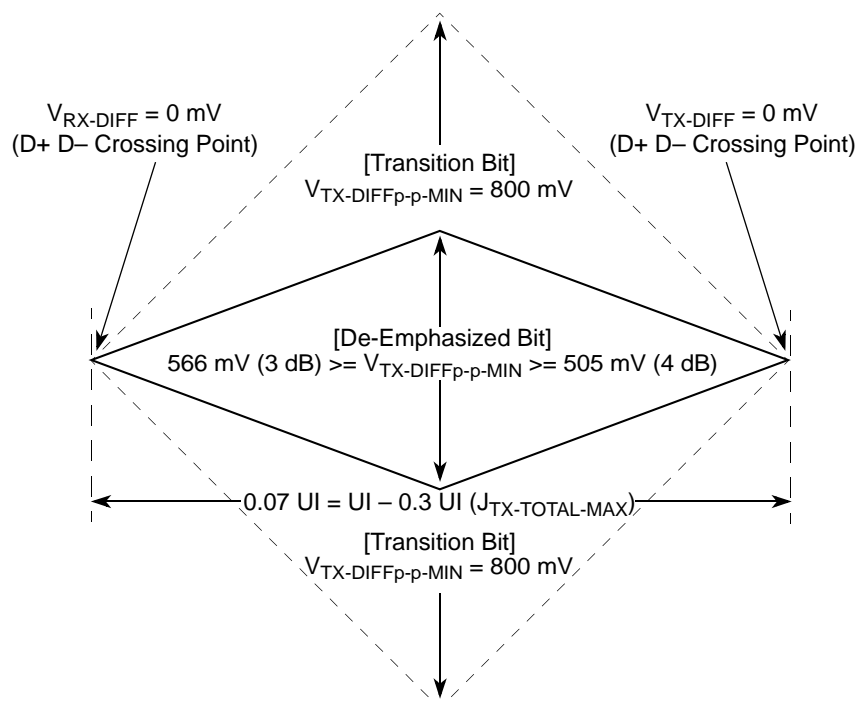


Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

### 17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 57. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps $\pm$ 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2 \times  V_{RX-D+} - V_{RX-D-} $ . See Note 2.
$T_{RX-EYE}$	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ( $V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.



Table 57. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

**Notes:**

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in [Figure 50](#) must be used as the RX device when taking measurements (also see the receiver compliance eye diagram shown in [Figure 49](#)). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A  $T_{RX-EYE} = 0.40$  UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The  $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$  specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. Note that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50  $\Omega$  to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- $\Omega$  probes—see [Figure 50](#)). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode Impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in [Figure 49](#) is specified using the passive compliance/test measurement load (see [Figure 50](#)) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see [Figure 50](#)) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer must provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in [Figure 49](#)) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.



Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV <sub>DD</sub>	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV <sub>DD</sub>	—
TV <sub>DD</sub>	W9, Y6	Power for TSEC3 and TSEC4 (2.5 V, 3.3 V)	TV <sub>DD</sub>	—
GV <sub>DD</sub>	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5)	GV <sub>DD</sub>	—
BV <sub>DD</sub>	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV <sub>DD</sub>	—
V <sub>DD</sub>	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V <sub>DD</sub>	—
SV <sub>DD</sub>	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core Power for SerDes transceivers (1.1 V)	SV <sub>DD</sub>	—
XV <sub>DD</sub>	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV <sub>DD</sub>	—
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	—	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	—	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	—	26
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	—	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	O	V <sub>DD</sub>	13

Table 72 provides the pin-out listing for the MPC8547E 783 FC-PBGA package.

### NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

**Table 72. MPC8547E Pinout Listing**

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PCI1 (One 64-Bit or One 32-Bit)</b>				
PCI1_AD[63:32]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV <sub>DD</sub>	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV <sub>DD</sub>	17
PCI1_C_BE[7:4]	AF15, AD14, AE15, AD15	I/O	OV <sub>DD</sub>	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV <sub>DD</sub>	17
PCI1_PAR64	W15	I/O	OV <sub>DD</sub>	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV <sub>DD</sub>	5, 9, 35
PCI1_GNT0	AG5	I/O	OV <sub>DD</sub>	—
PCI1_IRDY	AF11	I/O	OV <sub>DD</sub>	2
PCI1_PAR	AD12	I/O	OV <sub>DD</sub>	—
PCI1_PERR	AC12	I/O	OV <sub>DD</sub>	2
PCI1_SERR	V13	I/O	OV <sub>DD</sub>	2, 4
PCI1_STOP	W12	I/O	OV <sub>DD</sub>	2
PCI1_TRDY	AG11	I/O	OV <sub>DD</sub>	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV <sub>DD</sub>	—
PCI1_REQ0	AH3	I/O	OV <sub>DD</sub>	—
PCI1_CLK	AH26	I	OV <sub>DD</sub>	39
PCI1_DEVSEL	AH11	I/O	OV <sub>DD</sub>	2
PCI1_FRAME	AE11	I/O	OV <sub>DD</sub>	2
PCI1_IDSEL	AG9	I	OV <sub>DD</sub>	—
PCI1_REQ64	AF14	I/O	OV <sub>DD</sub>	2, 5, 10
PCI1_ACK64	V15	I/O	OV <sub>DD</sub>	2
Reserved	AE28	—	—	2
Reserved	AD26	—	—	2
Reserved	AD25	—	—	2

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	O	—	24

**Note:** All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

### NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73. MPC8545E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PCI1 and PCI2 (One 64-Bit or Two 32-Bit)</b>				
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV <sub>DD</sub>	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV <sub>DD</sub>	17
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV <sub>DD</sub>	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV <sub>DD</sub>	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV <sub>DD</sub>	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV <sub>DD</sub>	5, 9, 35
PCI1_GNT0	AG5	I/O	OV <sub>DD</sub>	—
PCI1_IRDY	AF11	I/O	OV <sub>DD</sub>	2
PCI1_PAR	AD12	I/O	OV <sub>DD</sub>	—
PCI1_PERR	AC12	I/O	OV <sub>DD</sub>	2
PCI1_SERR	V13	I/O	OV <sub>DD</sub>	2, 4
PCI1_STOP	W12	I/O	OV <sub>DD</sub>	2
PCI1_TRDY	AG11	I/O	OV <sub>DD</sub>	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV <sub>DD</sub>	—
PCI1_REQ0	AH3	I/O	OV <sub>DD</sub>	—
PCI1_CLK	AH26	I	OV <sub>DD</sub>	39
PCI1_DEVSEL	AH11	I/O	OV <sub>DD</sub>	2

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_IMP_CAL_RX	L28	I	200 $\Omega$ to GND	—
SD_IMP_CAL_TX	AB26	I	100 $\Omega$ to GND	—
SD_PLL_TPA	U26	O	—	24

**Note:** All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74 provides the pin-out listing for the MPC8543E 783 FC-PBGA package.

### NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 74. MPC8543E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PCI1 (One 32-Bit)</b>				
Reserved	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18,	—	—	110
GPOUT[8:15]	AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22	O	OV <sub>DD</sub>	—
GPIN[8:15]	AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I	OV <sub>DD</sub>	111
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV <sub>DD</sub>	17
Reserved	AF15, AD14, AE15, AD15	—	—	110
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV <sub>DD</sub>	17
Reserved	W15	—	—	110
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	O	OV <sub>DD</sub>	5, 9, 35
PCI1_GNT0	AG5	I/O	OV <sub>DD</sub>	—
PCI1_IRDY	AF11	I/O	OV <sub>DD</sub>	2
PCI1_PAR	AD12	I/O	OV <sub>DD</sub>	—
PCI1_PERR	AC12	I/O	OV <sub>DD</sub>	2
PCI1_SERR	V13	I/O	OV <sub>DD</sub>	2, 4
PCI1_STOP	W12	I/O	OV <sub>DD</sub>	2

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>JTAG</b>				
TCK	AG28	I	OV <sub>DD</sub>	—
TDI	AH28	I	OV <sub>DD</sub>	12
TDO	AF28	O	OV <sub>DD</sub>	—
TMS	AH27	I	OV <sub>DD</sub>	12
$\overline{\text{TRST}}$	AH23	I	OV <sub>DD</sub>	12
<b>DFT</b>				
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25
$\overline{\text{LSSD\_MODE}}$	AH20	I	OV <sub>DD</sub>	25
TEST_SEL	AH14	I	OV <sub>DD</sub>	109
<b>Thermal Management</b>				
THERM0	AG1	—	—	14
THERM1	AH1	—	—	14
<b>Power Management</b>				
ASLEEP	AH18	O	OV <sub>DD</sub>	9, 19, 29
<b>Power and Ground Signals</b>				
GND	A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17, F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27, L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13, U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27, K28, L24, L26, N24, N27, P25, R28, T24, T26, U24, V25, W28, Y24, Y26, AA24, AA27, AB25, AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27	—	—	—
OV <sub>DD</sub>	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV <sub>DD</sub>	—
LV <sub>DD</sub>	N8, R7, T9, U6	Power for TSEC1 and TSEC2 (2.5 V, 3.3 V)	LV <sub>DD</sub>	—

## 20 Clocking

This section describes the PLL configuration of the device. Note that the platform clock is identical to the core complex bus (CCB) clock.

### 20.1 Clock Ranges

Table 75 through Table 77 provide the clocking specifications for the processor cores and Table 78, through Table 80 provide the clocking specifications for the memory bus.

**Table 75. Processor Core Clocking Specifications (MPC8548E and MPC8547E)**

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	1000 MHz		1200 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	1000	800	1200	800	1333	MHz	1, 2

**Notes:**

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

**Table 76. Processor Core Clocking Specifications (MPC8545E)**

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1200 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	800	1200	MHz	1, 2

**Notes:**

- Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.



## 20.3 e500 Core PLL Ratio

This table describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in this table.

**Table 82. e500 Core to CCB Clock Ratio**

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

## 20.4 Frequency Options

**Table 83** This table shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

**Table 83. Frequency Options of SYSCLK with Respect to Memory Bus Speeds**

CCB to SYSCLK Ratio	SYSCLK (MHz)								
	16.66	25	33.33	41.66	66.66	83	100	111	133.33
	Platform/CCB Frequency (MHz)								
2									
3								333	400
4						333	400	445	533
5					333	415	500		
6					400	500			
8				333	533				
9				375					
10			333	417					
12			400	500					
16		400	533						
20	333	500							

**Note:** Due to errata Gen 13 the max sys clk frequency must not exceed 100 MHz if the core clk frequency is below 1200 MHz.

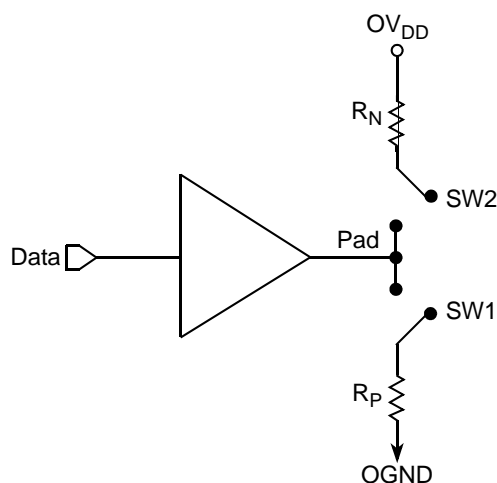


Figure 61. Driver Impedance Measurement

This table summarizes the signal impedance targets. The driver impedances are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ ,  $105^{\circ}\text{C}$ .

Table 86. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
$R_N$	43 Target	25 Target	20 Target	$Z_0$	W
$R_P$	43 Target	25 Target	20 Target	$Z_0$	W

Note: Nominal supply voltages. See Table 1,  $T_j = 105^{\circ}\text{C}$ .

## 22.8 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of  $4.7\text{ k}\Omega$  on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While  $\overline{\text{HRESET}}$  is asserted however, these pins are treated as inputs. The value presented on these pins while  $\overline{\text{HRESET}}$  is asserted, is latched when  $\overline{\text{HRESET}}$  deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately  $20\text{ k}\Omega$ . This value must permit the  $4.7\text{-k}\Omega$  resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during  $\overline{\text{HRESET}}$  (and for platform/system clocks after  $\overline{\text{HRESET}}$  deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor minimizes the disruption of signal quality or speed for output pins thus configured.

as shown in Figure 63. If this is not possible, the isolation resistor allows future access to  $\overline{\text{TRST}}$  in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

COP_TDO	1	2	NC
COP_TDI	3	4	$\overline{\text{COP\_TRST}}$
COP_RUN/STOP	5	6	COP_VDD_SENSE
COP_TCK	7	8	$\overline{\text{COP\_CHKSTP\_IN}}$
COP_TMS	9	10	NC
$\overline{\text{COP\_SRESET}}$	11	12	NC
$\overline{\text{COP\_HRESET}}$	13	KEY No pin	
$\overline{\text{COP\_CHKSTP\_OUT}}$	15	16	GND

**Figure 62. COP Connector Physical Pinout**

## 23.2 Part Marking

Parts are marked as the example shown in [Figure 64](#).



**Notes:**

TWLYYWW is final test traceability code.

MMMMM is 5 digit mask number.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

YWWLAZ is assembly traceability code.

**Figure 64. Part Marking for CBGA and PBGA Device**

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