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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548vjavhd

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Overview

- AESU-Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I^2C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I^2C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)

4 Input Clocks

This section discusses the timing for the input clocks.

4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	t _{SYSCLK}	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t _{KHK} /t _{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth must be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
- 7. For spread spectrum clocking. Guidelines are + 0% to -1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- 8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 19. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[<i>n</i>]/MCK[<i>n</i>] crossing	t _{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK 533 MHz 400 MHz 333 MHz	t _{DDKHAS}	1.48 1.95 2.40		ns	3
ADDR/CMD output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t ddkhax	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output setup with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCS	1.48 1.95 2.40		ns	3
MCS[<i>n</i>] output hold with respect to MCK 533 MHz 400 MHz 333 MHz	^t DDKHCX	1.48 1.95 2.40		ns	3
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 533 MHz 400 MHz 333 MHz	^t DDKHDS, ^t DDKLDS	538 700 900	 	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 533 MHz 400 MHz 333 MHz	^t ddkhdx, ^t ddkldx	538 700 900		ps	5
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5 imes t_{MCK}$ + 0.6	ns	6

8 Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller. The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII, MII, and TBI interfaces can be operated at 3.3 or 2.5 V. The GMII, MII, or TBI interface timing is compliant with the IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."

8.1.1 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 22 and Table 23. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.13	3.47	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = min$, $I_{OH} = -4.0 mA$)	V _{OH}	2.40	$LV_{DD}/TV_{DD} + 0.3$	V	_
Output low voltage ($LV_{DD}/TV_{DD} = min, I_{OL} = 4.0 mA$)	V _{OL}	GND	0.50	V	_
Input high voltage	V _{IH}	2.0	$LV_{DD}/TV_{DD} + 0.3$	V	_
Input low voltage	V _{IL}	-0.3	0.90	V	_
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I _{IH}	—	40	μΑ	1, 2, 3
Input low current (V _{IN} = GND)	IIL	-600	_	μA	

Table 22.	GMII. MI	I. RMII. a	and TBI DC	Electrical	Characteristics
	O min, mi	.,		Licothour	onaraotoristios

Notes:

1. LV_{DD} supports eTSECs 1 and 2.

2. TV_DD supports eTSECs 3 and 4.

3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

A timing diagram for TBI receive appears in Figure 16.



Figure 16. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
Data to clock output skew (at transmitter)	t _{SKRGT} 5	-500 ⁶	0	500 ⁶	ps
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0	_	2.8	ns
Clock period ³	t _{RGT} 5	7.2	8.0	8.8	ns
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 4}	t _{RGTH} /t _{RGT} 5	45	50	55	%
Rise time (20%–80%)	t _{RGTR} 5	_	_	0.75	ns
Fall time (20%–80%)	t _{RGTF} 5		—	0.75	ns

Table 33. RGMII and RTBI AC Timing Specifications

Notes:

 In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

5. Guaranteed by characterization.

6. In rev 1.0 silicon, due to errata, t_{SKRGT} is -650 ps (min) and 650 ps (max). See "eTSEC 10" in the device errata document.

Table 34. RMII Transmit A	C Timing	Specifications	(continued)
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Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TSEC <i>n_</i> TX_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0		10.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 18 shows the RMII transmit AC timing diagram.



Figure 18. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 35. RMII Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TSEC <i>n</i> _TX_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns
TSEC <i>n</i> _TX_CLK duty cycle	t _{RMRH}	35	50	65	%
TSEC <i>n</i> _TX_CLK peak-to-peak jitter	t _{RMRJ}	—	_	250	ps
Rise time TSEC <i>n</i> _TX_CLK(20%–80%)	t _{RMRR}	1.0	_	2.0	ns
Fall time TSEC <i>n</i> _TX_CLK (80%–20%)	t _{RMRF}	1.0	_	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDX}	2.0	_	—	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Parameter		Symbol ²	Min	Мах	Unit	Notes
Valid times:	Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	4 2	20 10	ns	5
Output hold times:	Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	30 30		ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO		t _{jtkldz} t _{jtkloz}	3 3	19 9	ns	5, 6

 Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design.

Figure 29 provides the AC test load for TDO and the boundary-scan outputs.



Figure 29. AC Test Load for the JTAG Interface

Figure 30 provides the JTAG clock input timing diagram.



Figure 30. JTAG Clock Input Timing Diagram



Figure 34 shows the AC timing diagram for the I^2C bus.



Figure 34. I²C Bus AC Timing Diagram

16 High-Speed Serial Interfaces (HSSI)

The device features one Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express and/or serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 38 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for the description. The figure shows a waveform for either a transmitter output (SD_TX and \overline{SD}_TX) or a receiver input (SD_RX and \overline{SD}_RX). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify the illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

• Single-ended swing

The transmitter output signals and the receiver input signals SD_TX, \overline{SD}_TX , \overline{SD}_RX and \overline{SD}_RX each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

- Differential output voltage, V_{OD} (or differential output swing): The differential output voltage (or swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SD_TX} - V_{\overline{SD_TX}}$. The V_{OD} value can be either positive or negative.
- Differential input voltage, V_{ID} (or differential input swing): The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: V_{SD_RX} – V_{SD_RX}. The V_{ID} value can be either positive or negative.
- Differential peak voltage, V_{DIFFp} The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.
- Differential peak-to-peak, $V_{DIFFp-p}$ Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
- Common mode voltage, V_{cm} The common mode voltage is equal to one half of the sum of the voltages between each conductor

High-Speed Serial Interfaces (HSSI)

- The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.
- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 40 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 41 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended mode
 - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-to-peak (from V_{min} to V_{max}) with SD_REF_CLK either left unconnected or tied to ground.
 - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 42 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DCor AC-coupled into the unused phase (SD_REF_CLK) through the same source impedance as the clock input (SD_REF_CLK) in use.



Figure 40. Differential Reference Clock Input DC Requirements (External DC-Coupled)

High-Speed Serial Interfaces (HSSI)

Figure 43 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with SerDes reference clock input's DC requirement.





Figure 44 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the SerDes reference clock input's allowed range (100–400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50- Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 45 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with the SerDes reference clock input's DC requirement, AC-coupling must be used. Figure 45 assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 <u>DC Requirements</u> for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and SD_	REF_CLK AC Requirements
------------------------------	-------------------------

Symbol	Parameter Description	Min	Тур	Max	Unit	Notes
t _{REF}	REFCLK cycle time	_	10	_	ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	_	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	-50		50	ps	_

Note:

1. Typical based on PCI Express Specification 2.0.

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a \pm 300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

PCI Express



Figure 48. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 57 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
V _{RX-DIFFp-p}	Differential peak-to-peak input voltage	0.175	_	1.200	V	$V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $. See Note 2.
T _{RX-EYE}	Minimum receiver eye width	0.4	_	_	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
T _{RX-EYE-MEDIAN-to-} MAX-JITTER	Maximum time between the jitter median and maximum deviation from the median	_	_	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.

Table 57. Differential Receiver (RX) Input Specifications

Package Description

Table 72	. MPC8547E	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	_		2
cfg_pci1_clk	AG24	I	OV _{DD}	5
Reserved	AF25	_		101
Reserved	AE25	_	_	2
Reserved	AG25	_		2
Reserved	AD24	_	_	2
Reserved	AF24	_		2
Reserved	AD27	_		2
Reserved	AD28, AE27, W17, AF26	_		2
Reserved	AH25	_		2
	DDR SDRAM Memory Interface			
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV _{DD}	_
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV _{DD}	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	0	GV _{DD}	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV _{DD}	—
MDQS[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV _{DD}	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	0	GV _{DD}	_
MBA[0:2]	F7, J7, M11	0	GV _{DD}	—
MWE	E7	0	GV _{DD}	—
MCAS	H7	0	GV _{DD}	—
MRAS	L8	0	GV _{DD}	—
MCKE[0:3]	F10, C10, J11, H11	0	GV _{DD}	11
MCS[0:3]	K8, J8, G8, F8	0	GV _{DD}	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV _{DD}	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV _{DD}	_
MODT[0:3]	E6, K6, L7, M7	0	GV _{DD}	—
MDIC[0:1]	A19, B19	I/O	GV _{DD}	36

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
Reserved	U20, V22, W20, Y22	_	—	15		
Reserved	U21, V23, W21, Y23	—	—	15		
SD_PLL_TPD	U28	0	XV _{DD}	24		
SD_REF_CLK	T28	I	XV _{DD}	—		
SD_REF_CLK	T27	I	XV _{DD}	—		
Reserved	AC1, AC3	—	—	2		
Reserved	M26, V28	—	—	32		
Reserved	M25, V27	—	—	34		
Reserved	M20, M21, T22, T23	—	—	38		
	General-Purpose Output					
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV _{DD}	—		
	System Control					
HRESET	AG17	I	OV _{DD}	—		
HRESET_REQ	AG16	0	OV _{DD}	29		
SRESET	AG20	I	OV _{DD}	—		
CKSTP_IN	AA9	I	OV _{DD}	—		
CKSTP_OUT	AA8	0	OV _{DD}	2, 4		
	Debug					
TRIG_IN	AB2	I	OV _{DD}	—		
TRIG_OUT/READY/QUIESCE	AB1	0	OV _{DD}	6, 9, 19, 29		
MSRCID[0:1]	AE4, AG2	0	OV _{DD}	5, 6, 9		
MSRCID[2:4]	AF3, AF1, AF2	0	OV _{DD}	6, 19, 29		
MDVAL	AE5	0	OV _{DD}	6		
CLK_OUT	AE21	0	OV _{DD}	11		
	Clock					
RTC	AF16	I	OV _{DD}	—		
SYSCLK	AH17	I	OV _{DD}	—		
JTAG						
тск	AG28	I	OV _{DD}	—		
TDI	AH28	Ι	OV _{DD}	12		
TDO	AF28	0	OV _{DD}	_		
TMS	AH27	I	OV _{DD}	12		
TRST	AH23	Ι	OV _{DD}	12		

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	_		
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	—		
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV _{DD}	—		
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad Power for SerDes transceivers (1.1 V)	XV _{DD}	_		
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	_	26		
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26		
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	_	26		
AVDD_CORE	AH15	Power for e500 PLL (1.1 V)	_	26		
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)	—	26		
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)		26		
SENSEVDD	M14	0	V_{DD}	13		
SENSEVSS	M16	—	—	13		
Analog Signals						
MVREF	A18	l Reference voltage signal for DDR	MVREF	_		
SD_IMP_CAL_RX	L28	I	200 Ω to GND	—		
SD_IMP_CAL_TX	AB26	I	100 Ω to GND	_		

Table 72. MPC8547E Pinout Listing (continued)

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	0		24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)			1
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2

Table 73. MPC8545E Pinout Listing

21 Thermal

This section describes the thermal specifications of the device.

21.1 Thermal for Version 2.0 Silicon HiCTE FC-CBGA with Full Lid

This section describes the thermal specifications for the HiCTE FC-CBGA package for revision 2.0 silicon.

This table shows the package thermal characteristics.

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	17	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	12	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	11	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	8	°C/W	1, 2
Die junction-to-board	N/A	R_{\thetaJB}	3	°C/W	3
Die junction-to-case	N/A	$R_{ extsf{ heta}JC}$	0.8	°C/W	4

Table 84. Package Thermal Characteristics for HiCTE FC-CBGA

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- 3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature, measured value includes the thermal resistance of the interface layer.

21.2 Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid

This section describes the thermal specifications for the FC-PBGA package for revision 2.1.1, 2.1.2, and 3.0 silicon.

This table shows the package thermal characteristics.

Table 85. Package	Thermal	Characteristics	for FC-PBGA
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Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Die junction-to-ambient (natural convection)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	18	°C/W	1, 2
Die junction-to-ambient (natural convection)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Single-layer board (1s)	$R_{ extsf{ heta}JA}$	13	°C/W	1, 2
Die junction-to-ambient (200 ft/min)	Four-layer board (2s2p)	$R_{ extsf{ heta}JA}$	9	°C/W	1, 2

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level must always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 57, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It must be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be routed directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 57 through Figure 59 shows the PLL power supply filter circuits.



Figure 57. PLL Power Supply Filter Circuit with PLAT Pins



Figure 58. PLL Power Supply Filter Circuit with CORE Pins



Figure 59. PLL Power Supply Filter Circuit with PCI/LBIU Pins

The AV_{DD}_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS ball to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD}_SRDS ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS to

System Design Information

22.10 Guidelines for High-Speed Interface Termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused and when it is partly unused.

22.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin must be terminated as described in this section.

The following pins must be left unconnected (float):

- SD_TX[7:0]
- $\overline{\text{SD}}_{\text{TX}}[7:0]$
- Reserved pins T22, T23, M20, M21

The following pins must be connected to GND:

- SD_RX[7:0]
- <u>SD_RX</u>[7:0]
- SD_REF_CLK
- SD_REF_CLK

NOTE

It is recommended to power down the unused lane through SRDSCR1[0:7] register (offset = $0xE_0F08$) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

Pins V28 and M26 must be tied to XV_{DD} . Pins V27 and M25 must be tied to GND through a 300- Ω resistor.

In Rev 2.0 silicon, POR configuration pin cfg_srds_en on TSEC4_TXD[2]/TSEC3_TXD[6] can be used to power down SerDes block.

22.10.2 SerDes Interface Partly Unused

If only part of the high-speed SerDes interface pins are used, the remaining high-speed serial I/O pins must be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[7:0]
- <u>SD_TX</u>[7:0]
- Reserved pins: T22, T23, M20, M21

The following pins must be connected to GND if not used:

- SD_RX[7:0]
- $\overline{\text{SD}_{RX}}[7:0]$
- SD_REF_CLK