E·XFL



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548vtatgd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Overview

- AESU-Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU—Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I^2C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I^2C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I²C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)

- VRRP and HSRP support for seamless router fail-over
- Up to 16 exact-match MAC addresses supported
- Broadcast address (accept/reject)
- Hash table match on up to 512 multicast addresses
- Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache
- OCeaN switch fabric
 - Full crossbar packet switch
 - Reorders packets from a source based on priorities
 - Reorders packets to bypass blocked packets
 - Implements starvation avoidance algorithms
 - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
 - Four-channel controller
 - All channels accessible by both the local and remote masters
 - Extended DMA functions (advanced chaining and striding capability)
 - Support for scatter and gather transfers
 - Misaligned transfer capability
 - Interrupt on completed segment, link, list, and error
 - Supports transfers to or from any local memory or I/O port
 - Selectable hardware-enforced coherency (snoop/no snoop)
 - Ability to start and flow control each DMA channel from external 3-pin interface
 - Ability to launch DMA from single write transaction
- Two PCI/PCI-X controllers
 - PCI 2.2 and PCI-X 1.0 compatible
 - One 32-/64-bit PCI/PCI-X port with support for speeds of up to 133 MHz (maximum PCI-X frequency in synchronous mode is 110 MHz)
 - One 32-bit PCI port with support for speeds from 16 to 66 MHz (available when the other port is in 32-bit mode)
 - Host and agent mode support
 - 64-bit dual address cycle (DAC) support
 - PCI-X supports multiple split transactions
 - Supports PCI-to-memory and memory-to-PCI streaming

Overview

- Memory prefetching of PCI read accesses
- Supports posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible
- Selectable hardware-enforced coherency
- Serial RapidIO[™] interface unit
 - Supports RapidIO[™] Interconnect Specification, Revision 1.2
 - Both $1 \times$ and $4 \times$ LP-serial link interfaces
 - Long- and short-haul electricals with selectable pre-compensation
 - Transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
 - Auto detection of 1- and 4-mode operation during port initialization
 - Link initialization and synchronization
 - Large and small size transport information field support selectable at initialization time
 - 34-bit addressing
 - Up to 256 bytes data payload
 - All transaction flows and priorities
 - Atomic set/clr/inc/dec for read-modify-write operations
 - Generation of IO_READ_HOME and FLUSH with data for accessing cache-coherent data at a remote memory system
 - Receiver-controlled flow control
 - Error detection, recovery, and time-out for packets and control symbols as required by the RapidIO specification
 - Register and register bit extensions as described in part VIII (Error Management) of the RapidIO specification
 - Hardware recovery only
 - Register support is not required for software-mediated error recovery.
 - Accept-all mode of operation for fail-over support
 - Support for RapidIO error injection
 - Internal LP-serial and application interface-level loopback modes
 - Memory and PHY BIST for at-speed production test
- RapidIO-compatible message unit
 - 4 Kbytes of payload per message
 - Up to sixteen 256-byte segments per message
 - Two inbound data message structures within the inbox
 - Capable of receiving three letters at any mailbox
 - Two outbound data message structures within the outbox
 - Capable of sending three letters simultaneously
 - Single segment multicast to up to 32 devIDs
 - Chaining and direct modes in the outbox

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Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T _{STG}	-55 to 150	°C	

Table 1. Absolute Maximum Ratings ¹ (continued)

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- 2. The -0.3 to 2.75 V range is for DDR and -0.3 to 1.98 V range is for DDR2.
- 3. The 3.63 V maximum is only supported when the port is configured in GMII, MII, RMII, or TBI modes; otherwise the 2.75 V maximum applies. See Section 8.2, "FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications," for details on the recommended operating conditions per protocol.
- 4. (M,L,O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

2.1.2 Recommended Operating Conditions

The following table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

	Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltag	e	V _{DD}	1.1 V ± 55 mV	V	
PLL supply voltage		AV _{DD}	1.1 V ± 55 mV	V	1
Core power supply	for SerDes transceivers	SV _{DD}	1.1 V ± 55 mV	V	
Pad power supply	for SerDes transceivers	XV _{DD}	1.1 V ± 55 mV	V	
DDR and DDR2 DI	RAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ether	net I/O voltage	LV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	_	4
PCI/PCI-X, DUART Ethernet MII mana	F, system control and power management, I ² C, gement, and JTAG I/O voltage	OV _{DD}	3.3 V ± 165 mV	V	3
Local bus I/O volta	ge	BV _{DD} 3.3 V ± 165 mV V 2.5 V ± 125 mV			—
Input voltage	DDR and DDR2 DRAM signals	MV _{IN}	GND to GV _{DD}	V	2
	DDR and DDR2 DRAM reference	MV _{REF}	GND to GV _{DD} /2	V	2
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	GND to LV _{DD} GND to TV _{DD}	V	4
	Local bus signals	BV _{IN}	GND to BV _{DD}	V	
	PCI, DUART, SYSCLK, system control and power management, I ² C, Ethernet MII management, and JTAG signals	OV _{IN}	GND to OV _{DD}	V	3

Table 2. Recommended Operating Conditions

4 Input Clocks

This section discusses the timing for the input clocks.

4.1 System Clock Timing

The following table provides the system clock (SYSCLK) AC timing specifications for the device.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	16	—	133	MHz	1, 6, 7, 8
SYSCLK cycle time	t _{SYSCLK}	7.5	—	60	ns	6, 7, 8
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t _{KHK} /t _{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	_	—	±150	ps	4, 5

Notes:

- Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.
- 2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The SYSCLK driver's closed loop jitter bandwidth must be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.
- 6. This parameter has been adjusted slower according to the workaround for device erratum GEN 13.
- 7. For spread spectrum clocking. Guidelines are + 0% to -1% down spread at modulation rate between 20 and 60 kHz on SYSCLK.
- 8. System with operating core frequency less than 1200 MHz must limit SYSCLK frequency to 100 MHz maximum.

4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal must be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

A summary of the FIFO AC specifications appears in Table 24 and Table 25.

Parameter/Condition	Symbol	Min	Тур	Max	Unit
TX_CLK, GTX_CLK clock period	t _{FIT}	5.3	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t _{FITH} /t _{FIT}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t _{FITJ}	—	_	250	ps
Rise time TX_CLK (20%–80%)	t _{FITR}	—	_	0.75	ns
Fall time TX_CLK (80%–20%)	t _{FITF}	—	_	0.75	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t _{FITDV}	2.0	_	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	_	3.0	ns

Table 24. FIFO Mode Transmit AC Timing Specification

Table 25. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t _{FIR}	5.3	8.0	100	ns
RX_CLK duty cycle	t _{FIRH} /t _{FIR}	45	50	55	%
RX_CLK peak-to-peak jitter	t _{FIRJ}	—		250	ps
Rise time RX_CLK (20%-80%)	t _{FIRR}	—	_	0.75	ns
Fall time RX_CLK (80%–20%)	t _{FIRF}	—	_	0.75	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{FIRDX}	0.5			ns

Note:

1. The minimum cycle period of the TX_CLK and RX_CLK is dependent on the maximum platform frequency of the speed bins the part belongs to as well as the FIFO mode under operation. See Section 4.5, "Platform to FIFO Restrictions."

Timing diagrams for FIFO appear in Figure 6 and Figure 7.



Figure 6. FIFO Transmit AC Timing Diagram

JTAG

Figure 31 provides the $\overline{\text{TRST}}$ timing diagram.







Figure 32. Boundary-Scan Timing Diagram

Table 56. Differential Transmitter	· (TX) Output	Specifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Unit	Comments
V _{TX-DC-CM}	The TX DC common mode voltage	0	_	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
I _{TX-SHORT}	TX short circuit current limit	_	_	90	mA	The total current the transmitter can provide when shorted to its ground
T _{TX-IDLE-MIN}	Minimum time spent in electrical idle	50	_		UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
T _{TX-IDLE-TO-DIFF-DATA}	Maximum time to transition to valid TX specifications after leaving an electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
RL _{TX-DIFF}	Differential return loss	12	_	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL _{TX-CM}	Common mode return loss	6		—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
Z _{TX-DIFF-DC}	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
Z _{TX-DC}	Transmitter DC impedance	40	_	_	Ω	Required TX D+ as well as D– DC impedance during all states
L _{TX-SKEW}	Lane-to-lane output skew	_	_	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single Link
C _{TX}	AC coupling capacitor	75	_	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.

PCI Express

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.



Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.



Figure 50. Compliance Test/Measurement Load

18.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long- and short-run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to Serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for Serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

18.6 Transmitter Specifications

LP-serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than:

- -10 dB for (baud frequency)/10 < Freq(f) < 625 MHz, and
- $-10 \text{ dB} + 10\log(f/625 \text{ MHz}) \text{ dB}$ for $625 \text{ MHz} \le \text{Freq}(f) \le \text{baud}$ frequency

The reference impedance for the differential return loss measurements is $100-\Omega$ resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%–80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Characteristic	Symbol	Rai	nge	Unit	Notos
Characteristic	Symbol	Min	Max	Onic	NOIES
Output voltage	Vo	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential output voltage	V _{DIFFPP}	500	1000	mV p-p	_
Deterministic jitter	J _D	_	0.17	UI p-p	_
Total jitter	J _T	_	0.35	UI p-p	_
Multiple output skew	S _{MO}	_	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 59. Short Run	Transmitter A	AC Timina	Specifications-	-1.25 GBaud
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Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LSYNC_IN	F27	I	BV _{DD}	_
LSYNC_OUT	F28	0	BV _{DD}	_
	DMA			
DMA_DACK[0:1]	AD3, AE1	0	OV _{DD}	5, 9, 102
DMA_DREQ[0:1]	AD4, AE2	I	OV _{DD}	_
DMA_DDONE[0:1]	AD2, AD1	0	OV _{DD}	_
	Programmable Interrupt Controller			
UDE	AH16	I	OV _{DD}	—
MCP	AG19	I	OV _{DD}	_
IRQ[0:7]	AG23, AF18, AE18, AF20, AG18, AF17, AH24, AE20	I	OV _{DD}	—
IRQ[8]	AF19	I	OV _{DD}	—
IRQ[9]/DMA_DREQ3	AF21	I	OV _{DD}	1
IRQ[10]/DMA_DACK3	AE19	I/O	OV _{DD}	1
IRQ[11]/DMA_DDONE3	AD20	I/O	OV _{DD}	1
IRQ_OUT	AD18	0	OV _{DD}	2, 4
	Ethernet Management Interface			
EC_MDC	AB9	0	OV _{DD}	5, 9
EC_MDIO	AC8	I/O	OV _{DD}	—
	Gigabit Reference Clock			
EC_GTX_CLK125	V11	I	LV _{DD}	_
Th	ree-Speed Ethernet Controller (Gigabit Ethern	et 1)		
TSEC1_RXD[7:0]	R5, U1, R3, U2, V3, V1, T3, T2	I	LV _{DD}	—
TSEC1_TXD[7:0]	T10, V7, U10, U5, U4, V6, T5, T8	0	LV _{DD}	5, 9
TSEC1_COL	R4	I	LV _{DD}	—
TSEC1_CRS	V5	I/O	LV _{DD}	20
TSEC1_GTX_CLK	U7	0	LV _{DD}	—
TSEC1_RX_CLK	U3	I	LV _{DD}	—
TSEC1_RX_DV	V2	I	LV _{DD}	—
TSEC1_RX_ER	T1	I	LV _{DD}	—
TSEC1_TX_CLK	T6	I	LV _{DD}	—
TSEC1_TX_EN	U9	0	LV _{DD}	30
TSEC1_TX_ER	Τ7	0	LV _{DD}	—

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Thre	e-Speed Ethernet Controller (Gigabit Ethe	rnet 2)		
TSEC2 RXDI7:01	P2, R2, N1, N2, P3, M2, M1, N3		LVpp	_
TSEC2 TXDI7:01	N9. N10. P8. N7. R9. N5. R8. N6	0	LVpp	5. 9. 33
TSEC2 COL	P1		LVpp	
TSEC2 CRS	R6	I/O	LVpp	20
TSEC2 GTX CLK	P6	0	LVDD	_
TSEC2 RX CLK	N4		LVpp	
TSEC2 RX DV	P5		LVpp	_
TSEC2 RX ER	R1		LVpp	_
TSEC2 TX CLK	P10		LVpp	
TSEC2 TX EN	P7	0	LVpp	30
TSEC2 TX ER	R10	0	LVpp	5. 9. 33
Thre	e-Speed Ethernet Controller (Gigabit Ethe	rnet 3)	DD	-, -,
TSEC3 TXD[3:0]	V8, W10, Y10, W7	,	TVpp	5,9,29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	
TSEC3_GTX_CLK	W8	0	TV _{DD}	
TSEC3_RX_CLK	W2	I	TV _{DD}	
TSEC3_RX_DV	W1	I	TV _{DD}	
TSEC3_RX_ER	Y2	I	TV _{DD}	
TSEC3_TX_CLK	V10		TV _{DD}	_
TSEC3_TX_EN	V9	0	TV _{DD}	30
Thre	e-Speed Ethernet Controller (Gigabit Ethe	rnet 4)		
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	1, 5, 9, 29
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	1
TSEC4_GTX_CLK	AA5	0	TV _{DD}	—
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV _{DD}	1
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV _{DD}	1, 31
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV _{DD}	1, 30
i	DUART		•	
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	_

Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
	Analog Signals			
MVREF	A18	I Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200Ω to GND	_
SD_IMP_CAL_TX	AB26	I	100Ω to GND	
SD_PLL_TPA	U26	0	—	24

Table 71. MPC8548E Pinout Listing (continued)

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, LCS5/DMA_REQ2 is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as DMA_REQ2.

- 2. Recommend a weak pull-up resistor (2-10 kΩ) be placed on this pin to OV_{DD}.
- 3. A valid clock must be provided at POR if TSEC4_TXD[2] is set = 1.
- 4. This pin is an open drain signal.
- 5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
- 6. Treat these pins as no connects (NC) unless using debug address functionality.
- The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 20.2, "CCB/SYSCLK PLL Ratio."
- 8. The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 20.3, "e500 Core PLL Ratio."
- 9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin therefore is described as an I/O for boundary scan.
- 10. This pin functionally requires a pull-up resistor, but during reset it is a configuration input that controls 32- vs. 64-bit PCI operation. Therefore, it must be actively driven low during reset by reset logic if the device is to be configured to be a 64-bit PCI device. See the *PCI Specification*.
- 11. This output is actively driven during reset rather than being three-stated during reset.
- 12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 14.Internal thermally sensitive resistor.
- 15.No connections must be made to these pins if they are not used.
- 16. These pins are not connected for any use.
- 17.PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI1_C_BE[7:4]).
- 19.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 20. This pin is only an output in FIFO mode when used as Rx flow control.

24.Do not connect.

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
TSEC2_TX_ER	R10	0	LV _{DD}	5, 9, 33	
Three	e-Speed Ethernet Controller (Gigabit Eth	ernet 3)			
TSEC3_TXD[3:0]	V8, W10, Y10, W7	0	TV _{DD}	5, 9, 29	
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV _{DD}	_	
TSEC3_GTX_CLK	W8	0	TV _{DD}	_	
TSEC3_RX_CLK	W2	I	TV _{DD}	_	
TSEC3_RX_DV	W1	I	TV _{DD}	_	
TSEC3_RX_ER	Y2	I	TV _{DD}	_	
TSEC3_TX_CLK	V10	I	TV _{DD}	_	
TSEC3_TX_EN	V9	0	TV _{DD}	30	
Three	e-Speed Ethernet Controller (Gigabit Eth	ernet 4)			
TSEC4_TXD[3:0]/TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	0	TV _{DD}	1, 5, 9, 29	
TSEC4_RXD[3:0]/TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV _{DD}	1	
TSEC4_GTX_CLK	AA5	0	TV _{DD}		
TSEC4_RX_CLK/TSEC3_COL	Y5	I	TV _{DD}	1	
TSEC4_RX_DV/TSEC3_CRS	AA3	I/O	TV _{DD}	1, 31	
TSEC4_TX_EN/TSEC3_TX_ER	AB6	0	TV _{DD}	1, 30	
· · ·	DUART			•	
UART_CTS[0:1]	AB3, AC5	I	OV _{DD}	—	
UART_RTS[0:1]	AC6, AD7	0	OV _{DD}	—	
UART_SIN[0:1]	AB5, AC7	I	OV _{DD}	—	
UART_SOUT[0:1]	AB7, AD8	0	OV _{DD}	_	
· · ·	I ² C Interface			•	
IIC1_SCL	AG22	I/O	OV _{DD}	4, 27	
IIC1_SDA	AG21	I/O	OV _{DD}	4, 27	
IIC2_SCL	AG15	I/O	OV _{DD}	4, 27	
IIC2_SDA	AG14	I/O	OV _{DD}	4, 27	
· · ·	SerDes				
SD_RX[0:3]	M28, N26, P28, R26	I	XV _{DD}	—	
SD_RX[0:3]	M27, N25, P27, R25	I	XV _{DD}	—	
SD_TX[0:3]	M22, N20, P22, R20	0	XV _{DD}	—	
SD_TX[0:3]	M23, N21, P23, R21	0	XV _{DD}	—	
Reserved	W26, Y28, AA26, AB28	—	—	40	
Reserved	W25, Y27, AA25, AB27	—	_	40	

Table 72. MPC8547E Pinout Listing (continued)

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SD_PLL_TPA	U26	0		24

Note: All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 73 provides the pin-out listing for the MPC8545E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)			1
PCI1_AD[63:32]/PCI2_AD[31:0]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV _{DD}	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV _{DD}	17
PCI1_C_BE[7:4]/PCI2_C_BE[3:0]	AF15, AD14, AE15, AD15	I/O	OV _{DD}	17
PCI1_C_BE[3:0]	AF9, AD11, Y12, Y13	I/O	OV _{DD}	17
PCI1_PAR64/PCI2_PAR	W15	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AG6, AE6, AF5, AH5	0	OV _{DD}	5, 9, 35
PCI1_GNT0	AG5	I/O	OV _{DD}	—
PCI1_IRDY	AF11	I/O	OV _{DD}	2
PCI1_PAR	AD12	I/O	OV _{DD}	—
PCI1_PERR	AC12	I/O	OV _{DD}	2
PCI1_SERR	V13	I/O	OV _{DD}	2, 4
PCI1_STOP	W12	I/O	OV _{DD}	2
PCI1_TRDY	AG11	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AH2, AG4, AG3, AH4	I	OV _{DD}	—
PCI1_REQ0	AH3	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	39
PCI1_DEVSEL	AH11	I/O	OV _{DD}	2

Table 73. MPC8545E Pinout Listing

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TV _{DD}	W9, Y6	Power for TSEC3 and TSEC4 (2,5 V, 3.3 V)	TV _{DD}	_
GV _{DD}	B3, B11, C7, C9, C14, C17, D4, D6, D10, D15, E2, E8, E11, E18, F5, F12, F16, G3, G7, G9, G11, H5, H12, H15, H17, J10, K3, K12, K16, K18, L6, M4, M8, M13	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V,2.5 V)	GV _{DD}	_
BV _{DD}	C21, C24, C27, E20, E25, G19, G23, H26, J20	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV _{DD}	—
V _{DD}	M19, N12, N14, N16, N18, P11, P13, P15, P17, P19, R12, R14, R16, R18, T11, T13, T15, T17, T19, U12, U14, U16, U18, V17, V19	Power for core (1.1 V)	V _{DD}	_
SV _{DD}	L25, L27, M24, N28, P24, P26, R24, R27, T25, V24, V26, W24, W27, Y25, AA28, AC27	Core power for SerDes transceivers (1.1 V)	SV _{DD}	_
XV _{DD}	L20, L22, N23, P21, R22, T20, U23, V21, W22, Y20	Pad power for SerDes transceivers (1.1 V)	XV _{DD}	_
AVDD_LBIU	J28	Power for local bus PLL (1.1 V)	_	26
AVDD_PCI1	AH21	Power for PCI1 PLL (1.1 V)	_	26
AVDD_PCI2	AH22	Power for PCI2 PLL (1.1 V)	_	26
AVDD_CORE	AH15		_	26
AVDD_PLAT	AH19	Power for CCB PLL (1.1 V)		26
AVDD_SRDS	U25	Power for SRDSPLL (1.1 V)	—	26
SENSEVDD	M14	0	V _{DD}	13

Table 74. MPC8543E Pinout Listing (continued)

Clocking

Characteristic	Maxim 800	num Process MHz	or Core Freq 1000	uency MHz	Unit	Notes
	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	MHz	1, 2

Table 77. Processor Core Clocking Specifications (MPC8543E)

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 78. Memory Bus Clocking Specifications (MPC8548E and MPC8547E)

	Maximum Process			
Characteristic	1000, 1200	1000, 1200, 1333 MHz		
	Min	Max		
Memory bus clock speed	166 266		MHz	1, 2

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

Table 79. Memory Bus Clocking Specifications (MPC8545E)

	Maximum Process	or Core Frequency	Unit	Notes
Characteristic	800, 1000,	1200 MHz		
	Min	Мах		
Memory bus clock speed	166	200	MHz	1, 2

Notes:

 Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

System Design Information

level must always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 57, one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It must be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit must be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It must be routed directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 57 through Figure 59 shows the PLL power supply filter circuits.



Figure 57. PLL Power Supply Filter Circuit with PLAT Pins



Figure 58. PLL Power Supply Filter Circuit with CORE Pins



Figure 59. PLL Power Supply Filter Circuit with PCI/LBIU Pins

The AV_{DD}_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDS ball to ensure it filters out as much noise as possible. The ground connection must be near the AV_{DD}_SRDS ball. The 0.003- μ F capacitor is closest to the ball, followed by the two 2.2 μ F capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS to

- First, the board must have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors must be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors must be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there must be a $1-\mu F$ ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device. This must be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there must be a 10- μ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100- μ F, low ESR SMT tantalum chip capacitor. This must be done for all SerDes supplies.

22.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs must be tied to V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} , as required. All unused active high inputs must be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND pins of the device.

22.6 Pull-Up and Pull-Down Resistor Requirements

The device requires weak pull-up resistors (2–10 k Ω is recommended) on open drain type pins including I²C pins and PIC (interrupt) pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 63. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

The following pins must not be pulled down during power-on reset: TSEC3_TXD[3], HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP. The DMA_DACK[0:1], and TEST_SEL/TEST_SEL pins must be set to a proper state during POR configuration. See the pinlist table of the individual device for more details

See the PCI 2.2 specification for all pull ups required for PCI.

22.7 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 61). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

Ordering Information

MPC	nnnnn	t	рр	ff	C	r
Product Code	Part Identifier	Temperature	Package ^{1, 2, 3}	Processor Frequency ⁴	Core Frequency	Silicon Version
MPC	8545E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

Table 87. Part Numbering Nomenclature (continued)

Notes:

1. See Section 19, "Package Description," for more information on available package types.

2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.

3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.

- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.