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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	·
Ethernet	10/100/1000Mbps (4)
SATA	·
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	·
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548vuaqg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 4.5 Platform to FIFO Restrictions

Note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency  $\leq$  platform clock frequency/4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency  $\leq$  platform clock frequency/4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency must be no more than 167 MHz.

## 4.6 Platform Frequency Requirements for PCI-Express and Serial RapidIO

The CCB clock frequency must be considered for proper operation of the high-speed PCI-Express and Serial RapidIO interfaces as described below.

For proper PCI Express operation, the CCB clock frequency must be greater than:

See *MPC8548ERM*, *Rev.* 2, *PowerQUICC III Integrated Processor Family Reference Manual*, Section 18.1.3.2, "Link Width," for PCI Express interface width details.

For proper serial RapidIO operation, the CCB clock frequency must be greater than:

 $2 \times (0.80) \times (Serial RapidIO interface frequency) \times (Serial RapidIO link width)$ 

64

See *MPC8548ERM*, *Rev.* 2, *PowerQUICC III Integrated Processor Family Reference Manual*, Section 17.4, "1x/4x LP-Serial Signal Descriptions," for serial RapidIO interface width and frequency details.

## 4.7 Other Input Clocks

For information on the input clocks of other functional blocks of the platform see the specific section of this document.

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

## 8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

able 31. TE	I Receive	<b>AC</b> Timing	Specifications
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Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TSEC <i>n</i> _RX_CLK[0:1] clock period	t <sub>TRX</sub>	—	16.0	—	ns
TSEC <i>n</i> _RX_CLK[0:1] skew	t <sub>SKTRX</sub>	7.5	—	8.5	ns
TSECn_RX_CLK[0:1] duty cycle	t <sub>TRXH</sub> /t <sub>TRX</sub>	40	—	60	%
RCG[9:0] setup time to rising TSEC <i>n</i> _RX_CLK	t <sub>TRDVKH</sub>	2.5	—	—	ns
RCG[9:0] hold time to rising TSEC <i>n</i> _RX_CLK	t <sub>TRDXKH</sub>	1.5	—	—	ns
TSEC <i>n</i> _RX_CLK[0:1] clock rise time (20%–80%)	t <sub>TRXR</sub> <sup>2</sup>	0.7	—	2.4	ns
TSEC <i>n</i> _RX_CLK[0:1] clock fall time (80%–20%)	t <sub>TRXF</sub> <sup>2</sup>	0.7	—	2.4	ns

Notes:

1. The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TRDVKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>TRDXKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>TRX</sub> represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).</sub>

2. Guaranteed by design.

#### Enhanced Three-Speed Ethernet (eTSEC)

Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram

## 8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC $n_RX_CLK$  pin (no receive clock is used on TSEC $n_TX_CLK$  in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC\_GTX\_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 32.

Parameter/Condition	Symbol	Min	Тур	Мах	Unit
RX_CLK clock period	t <sub>TRRX</sub>	7.5	8.0	8.5	ns
RX_CLK duty cycle	t <sub>TRRH/TRRX</sub>	40	50	60	%
RX_CLK peak-to-peak jitter	t <sub>TRRJ</sub>	_	_	250	ps
Rise time RX_CLK (20%–80%)	t <sub>TRRR</sub>	_	_	1.0	ns
Fall time RX_CLK (80%–20%)	t <sub>TRRF</sub>	_	_	1.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t <sub>TRRDVKH</sub>	2.0	_	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t <sub>TRRDXKH</sub>	1.0	_	_	ns

#### **Ethernet Management Interface Electrical Characteristics**

## Table 37. MII Management AC Timing Specifications (continued)

At recommended operating conditions with  $\text{OV}_{\text{DD}}$  is 3.3 V ± 5%.

Parameter	Symbol <sup>1</sup>	Min	Тур	Мах	Unit	Notes
MDC fall time	t <sub>MDHF</sub>	_		10	ns	4

### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>MDKHDX</sub> symbolizes management data timing (MD) for the time t<sub>MDC</sub> from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t<sub>MDDVKH</sub> symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>MDC</sub> clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
  </sub>
- 2. This parameter is dependent on the eTSEC system clock speed, which is half of the Platform Frequency (f<sub>CCB</sub>). The actual ECn\_MDC output clock frequency for a specific eTSEC port can be programmed by configuring the MgmtClk bit field of device's MIIMCFG register, based on the platform (CCB) clock running for the device. The formula is: Platform Frequency (CCB) ÷ (2 × Frequency Divider determined by MIICFG[MgmtClk] encoding selection). For example, if MIICFG[MgmtClk] = 000 and the platform (CCB) is currently running at 533 MHz, f<sub>MDC</sub> = 533) ÷ (2 × 4 × 8) = 533) ÷ 64 = 8.3 MHz. That is, for a system running at a particular platform frequency (f<sub>CCB</sub>), the ECn\_MDC output clock frequency can be programmed between maximum f<sub>MDC</sub> = f<sub>CCB</sub> ÷ 64 and minimum f<sub>MDC</sub> = f<sub>CCB</sub> ÷ 448. See 14.5.3.6.6, "MII Management Configuration Register (MIIMCFG)," in the MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual for more detail.
- 3. The maximum ECn\_MDC output clock frequency is defined based on the maximum platform frequency for device (533 MHz) divided by 64, while the minimum ECn\_MDC output clock frequency is defined based on the minimum platform frequency for device (333 MHz) divided by 448, following the formula described in Note 2 above.
- 4. Guaranteed by design.
- 5. t<sub>CCB</sub> is the platform (CCB) clock period.

Figure 21 shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram

## **10.2 Local Bus AC Electrical Specifications**

This table describes the timing parameters of the local bus interface at  $BV_{DD} = 3.3$  V. For information about the frequency range of local bus, see Section 20.1, "Clock Ranges."

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	t <sub>LBK</sub>	7.5	12	ns	2
Local bus duty cycle	t <sub>LBKH/</sub> t <sub>LBK</sub>	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t <sub>LBKSKEW</sub>	—	150	ps	7, 8
Input setup to local bus clock (except LGTA/LUPWAIT)	t <sub>LBIVKH1</sub>	1.8	—	ns	3, 4
LGTA/LUPWAIT input setup to local bus clock	t <sub>LBIVKH2</sub>	1.7	—	ns	3, 4
Input hold from local bus clock (except LGTA/LUPWAIT)	t <sub>LBIXKH1</sub>	1.0	—	ns	3, 4
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKH2</sub>	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t <sub>LBOTOT</sub>	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKHOV1</sub>	—	2.0	ns	—
Local bus clock to data valid for LAD/LDP	t <sub>LBKHOV2</sub>	—	2.2	ns	3
Local bus clock to address valid for LAD	t <sub>LBKHOV3</sub>	—	2.3	ns	3
Local bus clock to LALE assertion	t <sub>LBKHOV4</sub>	—	2.3	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKHOX1</sub>	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t <sub>LBKHOX2</sub>	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKHOZ1</sub>	_	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKHOZ2</sub>		2.5	ns	5

## Table 40. Local Bus Timing Parameters (BV<sub>DD</sub> = 3.3 V)—PLL Enabled

### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one (1). Also, t<sub>LBKH0X</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
- 2. All timings are in reference to LSYNC\_IN for PLL enabled and internal local bus clock for PLL bypass mode.
- 3. All signals are measured from  $BV_{DD}/2$  of the rising edge of LSYNC\_IN for PLL enabled or internal local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 6. t<sub>LBOTOT</sub> is a measurement of the minimum time between the negation of LALE and any change in LAD. t<sub>LBOTOT</sub> is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.
- 8. Guaranteed by design.

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
LGTA/LUPWAIT input hold from local bus clock	t <sub>LBIXKL2</sub>	-1.3		ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t <sub>LBOTOT</sub>	1.5		ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t <sub>LBKLOV1</sub>	_	-0.3	ns	
Local bus clock to data valid for LAD/LDP	t <sub>LBKLOV2</sub>	_	-0.1	ns	4
Local bus clock to address valid for LAD	t <sub>LBKLOV3</sub>	_	0	ns	4
Local bus clock to LALE assertion	t <sub>LBKLOV4</sub>	_	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t <sub>LBKLOX1</sub>	-3.7	_	ns	4
Output hold from local bus clock for LAD/LDP	t <sub>LBKLOX2</sub>	-3.7	_	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t <sub>LBKLOZ1</sub>	_	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	t <sub>LBKLOZ2</sub>		0.2	ns	7

### Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

#### Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>LBIXKH1</sub> symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t<sub>LBK</sub> clock reference (K) goes high (H), in this case for clock one (1). Also, t<sub>LBKH0X</sub> symbolizes local bus timing (LB) for the t<sub>LBK</sub> clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

 All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t<sub>LBKHKT</sub>.

3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV<sub>DD</sub>/2.

4. All signals are measured from  $BV_{DD}/2$  of the rising edge of local bus clock for PLL bypass mode to  $0.4 \times BV_{DD}$  of the signal in question for 3.3-V signaling levels.

5. Input timings are measured at the pin.

6. The value of t<sub>LBOTOT</sub> is the measurement of the minimum time between the negation of LALE and any change in LAD.

7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 8. Guaranteed by characterization.
- 9. Guaranteed by design.

#### Local Bus



Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

## 16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected must provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver must be 50  $\Omega$  to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes reference clocks are defined by each interface protocol based on application usage. See the following sections for detailed information:

- Section 17.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 18.2, "AC Requirements for Serial RapidIO SD\_REF\_CLK and SD\_REF\_CLK"

## 16.2.4.1 Spread Spectrum Clock

SD\_REF\_CLK/SD\_REF\_CLK are designed to work with a spread spectrum clock (+0% to -0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation must be used.

## 16.3 SerDes Transmitter and Receiver Reference Circuits

Figure 47 shows the reference circuits for SerDes data lane's transmitter and receiver.



Figure 47. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO, or SGMII) in this document based on the application usage:

- Section 17, "PCI Express"
- Section 18, "Serial RapidIO"

Note that external an AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in the specification of each protocol section.

Characteristic	Symbol	Range		Unit	Notos
Characteristic	Symbol	Min	Max	Onic	NULES
Differential input voltage	V <sub>IN</sub>	200	1600	mVp-p	Measured at receiver
Deterministic jitter tolerance	J <sub>D</sub>	0.37	—	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	J <sub>DR</sub>	0.55	—	UI p-p	Measured at receiver
Total jitter tolerance <sup>1</sup>	J <sub>T</sub>	0.65	_	UI p-p	Measured at receiver
Multiple input skew	S <sub>MI</sub>	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit error rate	BER	—	10 <sup>-12</sup>		—
Unit interval	UI	320	320	ps	±100 ppm

Table 68	. Receiver	AC	Timing	Specifications-	-3.125	GBaud
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## Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 53. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.



Figure 53. Single Frequency Sinusoidal Jitter Limits

**Package Description** 



- 1. All dimensions are in millimeters.
- 2. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Capacitors may not be present on all devices.
- 6. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
- 7. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 8. All dimensions are symmetric across the package center lines unless dimensioned otherwise.

## Figure 56. Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid

Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	I <sup>2</sup> C interface			•
IIC1_SCL	AG22	I/O	OV <sub>DD</sub>	4, 27
IIC1_SDA	AG21	I/O	OV <sub>DD</sub>	4, 27
IIC2_SCL	AG15	I/O	OV <sub>DD</sub>	4, 27
IIC2_SDA	AG14	I/O	OV <sub>DD</sub>	4, 27
	SerDes			•
SD_RX[0:7]	M28, N26, P28, R26, W26, Y28, AA26, AB28	I	XV <sub>DD</sub>	
SD_RX[0:7]	M27, N25, P27, R25, W25, Y27, AA25, AB27	I	XV <sub>DD</sub>	—
SD_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV <sub>DD</sub>	—
SD_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV <sub>DD</sub>	—
SD_PLL_TPD	U28	0	XV <sub>DD</sub>	24
SD_REF_CLK	T28	I	XV <sub>DD</sub>	3
SD_REF_CLK	T27	I	XV <sub>DD</sub>	3
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	_	_	32
Reserved	M25, V27	—	_	34
Reserved	M20, M21, T22, T23	—	—	38
	General-Purpose Output			
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	0	BV <sub>DD</sub>	—
	System Control			
HRESET	AG17	I	OV <sub>DD</sub>	_
HRESET_REQ	AG16	0	OV <sub>DD</sub>	29
SRESET	AG20	I	OV <sub>DD</sub>	
CKSTP_IN	AA9	I	OV <sub>DD</sub>	—
CKSTP_OUT	AA8	0	OV <sub>DD</sub>	2, 4
	Debug			
TRIG_IN	AB2	I	OV <sub>DD</sub>	—
TRIG_OUT/READY/QUIESCE	AB1	0	OV <sub>DD</sub>	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	0	OV <sub>DD</sub>	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	0	OV <sub>DD</sub>	6, 19, 29
MDVAL	AE5	0	OV <sub>DD</sub>	6
CLK_OUT	AE21	0	OV <sub>DD</sub>	11

Table 71	. MPC8548E	<b>Pinout Listing</b>	(continued)
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Signal	Signal Package Pin Number		Power Supply	Notes		
	Clock					
RTC	AF16	I	OV <sub>DD</sub>	—		
SYSCLK	AH17	I	OV <sub>DD</sub>	—		
	JTAG					
ТСК	AG28	I	OV <sub>DD</sub>	—		
TDI	AH28	I	OV <sub>DD</sub>	12		
TDO	AF28	0	OV <sub>DD</sub>	—		
TMS	AH27	ļ	OV <sub>DD</sub>	12		
TRST	AH23	I	OV <sub>DD</sub>	12		
	DFT					
L1_TSTCLK	AC25	I	OV <sub>DD</sub>	25		
L2_TSTCLK	AE22	I	OV <sub>DD</sub>	25		
LSSD_MODE	AH20	I	OV <sub>DD</sub>	25		
TEST_SEL	AH14	I	OV <sub>DD</sub>	25		
Thermal Management						
THERM0	AG1	—	—	14		
THERM1	AH1	—	_	14		
	Power Management					
ASLEEP	AH18	0	OV <sub>DD</sub>	9, 19, 29		
	Power and Ground Signals					
GND	<ul> <li>A11, B7, B24, C1, C3, C5, C12, C15, C26, D8, D11, D16, D20, D22, E1, E5, E9, E12, E15, E17,</li> <li>F4, F26, G12, G15, G18, G21, G24, H2, H6, H8, H28, J4, J12, J15, J17, J27, K7, K9, K11, K27,</li> <li>L3, L5, L12, L16, N11, N13, N15, N17, N19, P4, P9, P12, P14, P16, P18, R11, R13, R15, R17, R19, T4, T12, T14, T16, T18, U8, U11, U13,</li> <li>U15, U17, U19, V4, V12, V18, W6, W19, Y4, Y9, Y11, Y19, AA6, AA14, AA17, AA22, AA23, AB4, AC2, AC11, AC19, AC26, AD5, AD9, AD22, AE3, AE14, AF6, AF10, AF13, AG8, AG27,</li> <li>K28, L24, L26, N24, N27, P25, R28, T24, T26,</li> <li>U24, V25, W28, Y24, Y26, AA24, AA27, AB25,</li> <li>AC28, L21, L23, N22, P20, R23, T21, U22, V20, W23, Y21, U27</li> </ul>	_	_	_		
OV <sub>DD</sub>	V16, W11, W14, Y18, AA13, AA21, AB11, AB17, AB24, AC4, AC9, AC21, AD6, AD13, AD17, AD19, AE10, AE8, AE24, AF4, AF12, AF22, AF27, AG26	Power for PCI and other standards (3.3 V)	OV <sub>DD</sub>	—		

### Package Description

## Table 71. MPC8548E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
25.These are test signals for factory u	ise only and must be pulled up (100 $\Omega$ –1 k $\Omega$ ) to (	DV <sub>DD</sub> for normal	machine opera	ation.			
26.Independent supplies derived from	n board V <sub>DD</sub> .						
27.Recommend a pull-up resistor (~1	$k\Omega$ ) be placed on this pin to OV <sub>DD</sub> .						
29. The following pins must NOT be p HRESET_REQ, TRIG_OUT/READ	oul <u>led down du</u> ring power-on reset: TSEC3_TXD  Y/QUIESCE, MSRCID[2:4], ASLEEP.	3], TSEC4_TXD	3/TSEC3_TXD	07,			
30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.							
31. This pin is only an output in eTSE	C3 FIFO mode when used as Rx flow control.						
32. These pins must be connected to 2	XV <sub>DD</sub> .						
33.TSEC2_TXD1, TSEC2_TX_ER an HRESET assertion.	e multiplexed as cfg_dram_type[0:1]. They must	be valid at powe	r-up, even befo	ore			
34. These pins must be pulled to group	nd through a 300- $\Omega$ (±10%) resistor.						
35.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI <i>n_</i> AD pins as 'no connect' or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the PCI <i>n_</i> AD pins are not connected to any other PCI device. The PCI block drives the PCI <i>n_</i> AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device.							
36.MDIC0 is grounded through an 18. 1% resistor. These pins are used for	2- $\Omega$ precision 1% resistor and MDIC1 is connected or automatic calibration of the DDR IOs.	ed to GV <sub>DD</sub> throu	gh an 18.2-Ω p	recision			
38. These pins must be left floating.							
39. If PCI1 or PCI2 is configured as P Otherwise the processor will not be	CI asynchronous mode, a valid clock must be pro oot up.	ovided on pin PC	I1_CLK or PCI	2_CLK.			
40.These pins must be connected to	GND.						
101.This pin requires an external 4.7-	kΩ resistor to GND.						
102.For Rev. 2.x silicon, DMA_DACK POR configuration are don't care.	[0:1] must be 0b11 during POR configuration; for	rev. 1.x silicon, t	he pin values o	during			
103.If these pins are not used as GPI $2-10 \text{ k}\Omega$ resistors.	Nn (general-purpose input), they must be pulled	low (to GND) or	high (to LV <sub>DD</sub> )	through			
104.These must be pulled low to GNE	D through 2–10 k $\Omega$ resistors if they are not used.						
105.These must be pulled low or high	to $\text{LV}_{\text{DD}}$ through 2–10 k $\Omega$ resistors if they are no	t used.					
106.For rev. 2.x silicon, DMA_DACK[0 configuration are don't care.	):1] must be 0b10 during POR configuration; for re	v. 1.x silicon, the	pin values duri	ng POR			
107.For rev. 2.x silicon, DMA_DACK[C configuration are don't care.	):1] must be 0b01 during POR configuration; for re	v. 1.x silicon, the	pin values duri	ng POR			
108.For rev. 2.x silicon, DMA_DACK[C configuration are don't care.	):1] must be 0b11 during POR configuration; for re	v. 1.x silicon, the	pin values duri	ng POR			
109. This is a test signal for factory us	e only and must be pulled down (100 $\Omega$ – 1 k $\Omega$ ) t	o GND for norma	al machine ope	eration.			
111. If these pins are not used as GPIN <i>n</i> (general-purpose input), they must be pulled low (to GND) or high (to $OV_{DD}$ ) through							
2-10 K22 HESISIUIS.	during DOP configuration						
112. This pin must not be pulled down	$\alpha$ $\alpha$ $\beta$						
	$\int \int \nabla \nabla D = \int \nabla \nabla \nabla \nabla D = \int \nabla \nabla \nabla \nabla \nabla \nabla D = \int \nabla \nabla$						

## Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MWE	E7	0	GV <sub>DD</sub>	_
MCAS	H7	0	GV <sub>DD</sub>	_
MRAS	L8	0	GV <sub>DD</sub>	
MCKE[0:3]	F10, C10, J11, H11	0	GV <sub>DD</sub>	11
MCS[0:3]	K8, J8, G8, F8	0	GV <sub>DD</sub>	
MCK[0:5]	H9, B15, G2, M9, A14, F1	0	GV <sub>DD</sub>	_
MCK[0:5]	J9, A15, G1, L9, B14, F2	0	GV <sub>DD</sub>	
MODT[0:3]	E6, K6, L7, M7	0	GV <sub>DD</sub>	_
MDIC[0:1]	A19, B19	I/O	GV <sub>DD</sub>	36
	Local Bus Controller Interface			
LAD[0:31]	E27, B20, H19, F25, A20, C19, E28, J23, A25, K22, B28, D27, D19, J22, K20, D28, D25, B25, E22, F22, F21, C25, C22, B23, F20, A23, A22, E19, A21, D21, F19, B21	I/O	BV <sub>DD</sub>	
LDP[0:3]	K21, C28, B26, B22	I/O	BV <sub>DD</sub>	
LA[27]	H21	0	BV <sub>DD</sub>	5, 9
LA[28:31]	H20, A27, D26, A28	0	BV <sub>DD</sub>	5, 7, 9
LCS[0:4]	J25, C20, J24, G26, A26	0	BV <sub>DD</sub>	_
LCS5/DMA_DREQ2	D23	I/O	BV <sub>DD</sub>	1
LCS6/DMA_DACK2	G20	0	BV <sub>DD</sub>	1
LCS7/DMA_DDONE2	E21	0	BV <sub>DD</sub>	1
LWE0/LBS0/LSDDQM[0]	G25	0	BV <sub>DD</sub>	5, 9
LWE1/LBS1/LSDDQM[1]	C23	0	BV <sub>DD</sub>	5, 9
LWE2/LBS2/LSDDQM[2]	J21	0	BV <sub>DD</sub>	5, 9
LWE3/LBS3/LSDDQM[3]	A24	0	BV <sub>DD</sub>	5, 9
LALE	H24	0	BV <sub>DD</sub>	5, 8, 9
LBCTL	G27	0	BV <sub>DD</sub>	5, 8, 9
LGPL0/LSDA10	F23	0	BV <sub>DD</sub>	5, 9
LGPL1/LSDWE	G22	0	BV <sub>DD</sub>	5, 9
LGPL2/LOE/LSDRAS	B27	0	BV <sub>DD</sub>	5, 8, 9
LGPL3/LSDCAS	F24	0	BV <sub>DD</sub>	5, 9
LGPL4/LGTA/LUPWAIT/LPBSE	H23	I/O	BV <sub>DD</sub>	
LGPL5	E26	0	BV <sub>DD</sub>	5, 9
LCKE	E24	0	BV <sub>DD</sub>	
LCLK[0:2]	E23, D24, H22	0	BV <sub>DD</sub>	_

### Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
	Analog Signals			
MVREF	A18	l Reference voltage signal for DDR	MVREF	
SD_IMP_CAL_RX	L28	I	200 Ω (±1%) to GND	_
SD_IMP_CAL_TX	AB26	I	100 Ω (±1%) to GND	—
SD_PLL_TPA	U26	0	AVDD_SRDS	24

## Table 74. MPC8543E Pinout Listing (continued)

**Note:** All note references in this table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

#### Clocking

Characteristic	Maximum Processor Core Freque			uency MHz	Unit	Notes
	Min	Max	Min	Max		
e500 core processor frequency	800	800	800	1000	MHz	1, 2

## Table 77. Processor Core Clocking Specifications (MPC8543E)

Notes:

1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

## Table 78. Memory Bus Clocking Specifications (MPC8548E and MPC8547E)

	Maximum Process	Unit	Notes	
Characteristic	1000, 1200			
	Min	Max		
Memory bus clock speed	166	266	MHz	1, 2

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

### Table 79. Memory Bus Clocking Specifications (MPC8545E)

	Maximum Process	Unit	Notes	
Characteristic	800, 1000,			
	Min	Мах		
Memory bus clock speed	166	200	MHz	1, 2

Notes:

 Caution: The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. See Section 20.2, "CCB/SYSCLK PLL Ratio," and Section 20.3, "e500 Core PLL Ratio," for ratio settings.

2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

# 23 Ordering Information

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Ordering information for the parts fully covered by this specification document is provided in Section 23.1, "Part Numbers Fully Addressed by this Document."

## 23.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the device. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part-numbering scheme also includes an application modifier that may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

MPC	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	t	pp	11	C	r
Product Code	Part Identifier	Temperature	Package <sup>1, 2, 3</sup>	Processor Frequency <sup>4</sup>	Core Frequency	Silicon Version
MPC	8548E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AV = 1500 <sup>3</sup> AU = 1333 AT = 1200 AQ = 1000	J = 533 H = 500 <sup>5</sup> G = 400	Blank = Ver. 2.0 (SVR = 0x80390020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390021) D = Ver. 3.1.x (SVR = 0x80390031)
	8548					Blank = Ver. 2.0 (SVR = 0x80310020) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310021) D = Ver. 3.1.x (SVR = 0x80310031)
	8547E			AU = 1333 AT = 1200 AQ = 1000	J = 533 G = 400	Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80390121) D = Ver. 3.1.x (SVR = 0x80390131)
	8547					Blank = Ver. 2.0 (SVR = 0x80390120) A = Ver. 2.1.1 B = Ver. 2.1.2 C = Ver. 2.1.3 (SVR = 0x80310121) D = Ver. 3.1.x (SVR = 0x80310131)

## Table 87. Part Numbering Nomenclature

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#### **Ordering Information**

MPC	nnnnn	t	рр	ff	C	r
Product Code	Part Identifier	Temperature	Package <sup>1, 2, 3</sup>	Processor Frequency <sup>4</sup>	Core Frequency	Silicon Version
MPC	8545E	Blank = 0 to 105°C C = -40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

## Table 87. Part Numbering Nomenclature (continued)

## Notes:

1. See Section 19, "Package Description," for more information on available package types.

2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.

3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.

- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.

## 23.2 Part Marking

Parts are marked as the example shown in Figure 64.



### Notes:

TWLYYWW is final test traceability code. MMMMM is 5 digit mask number. CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States. YWWLAZ is assembly traceability code.

## Figure 64. Part Marking for CBGA and PBGA Device

# 24 Document Revision History

The following table provides a revision history for this hardware specification.

#### Rev. Date Substantive Change(s) Number • Updated Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and 9 02/2012 Version 3.1.x Silicon with Stamped Lid," with version 3.0 silicon information. Added Figure 56, "Mechanical Dimensions and Bottom Surface Nomenclature of the FC-PBGA with Stamped Lid." • Updated Table 87, "Part Numbering Nomenclature," with version 3.0 silicon information. Removed Note from Section 5.1. "Power-On Ramp Rate". • Changed the Table 10 title to "Power Supply Ramp Rate". • Removed table 11. • Updated the title of Section 21.2, "Thermal for Version 2.1.1, 2.1.2, and 2.1.3 Silicon FC-PBGA with Full Lid and Version 3.1.x Silicon with Stamped Lid" to include Thermal Version 2.1.3 and Version 3.1.x Silicon. Corrected the leaded Solder Ball composition in Table 70, "Package Parameters" • Updated Table 87, "Part Numbering Nomenclature," with Version 3.1.x silicon information. • Updated the Min and Max value of TDO in the valid times row of Table 44, "JTAG AC Timing Specifications (Independent of SYSCLK)<sup>1</sup>" from 4 and 25 to 2 and 10 respectively . 8 04/2011 Added Section 14.1, "GPOUT/GPIN Electrical Characteristics." • Updated Table 71, "MPC8548E Pinout Listing," Table 72, "MPC8547E Pinout Listing," Table 73, "MPC8545E Pinout Listing," and Table 74, "MPC8543E Pinout Listing," to reflect that the TDO signal is not driven during HRSET\* assertion. • Updated Table 87, "Part Numbering Nomenclature" with Ver. 2.1.3 silicon information. In Table 37, "MII Management AC Timing Specifications, modified the fifth row from "MDC to MDIO 7 09/2010 delay tMDKHDX (16 x tptb\_clk x 8) - 3 - (16 x tptb\_clk x 8) + 3" to "MDC to MDIO delay tMDKHDX $(16 \times tCCB \times 8) - 3 - (16 \times tCCB \times 8) + 3."$ Updated Figure 55, "Mechanical Dimensions and Bottom Surface Nomenclature of the HiCTE FC-CBGA and FC-PBGA with Full Lid and figure notes. 6 12/2009 • In Section 5.1, "Power-On Ramp Rate" added explanation that Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. In Table 13 changed required ramp rate from 545 V/s for MVREF and VDD/XVDD/SVDD to 3500 V/s for MVREF and 4000 V/s for VDD. • In Table 13 deleted ramp rate requirement for XVDD/SVDD. In Table 13 footnote 1 changed voltage range of concern from 0-400 mV to 20-500mV. In Table 13 added footnote 2 explaining that VDD voltage ramp rate is intended to control ramp rate of AVDD pins. 5 10/2009 • In Table 27, "GMII Receive AC Timing Specifications," changed duty cycle specification from 40/60 to 35/75 for RX CLK duty cycle. Updated tMDKHDX in Table 37, "MII Management AC Timing Specifications." • Added a reference to Revision 2.1.2. • Updated Table 55, "MII Management AC Timing Specifications." Added Section 5.1, "Power-On Ramp Rate."

## Table 88. Document Revision History