Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (4)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8548vuauj

- – Dedicated single data rate SDRAM controller
- — Parity support
- — Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- • Four enhanced three-speed Ethernet controllers (eTSECs)
  - — Three-speed support (10/100/1000 Mbps)
  - — Four controllers designed to comply with IEEE Std. 802.3®, 802.3u, 802.3x, 802.3z, 802.3ac, and 802.3ab
  - — Support for various Ethernet physical interfaces:
    - – 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII
    - – 10/100 Mbps full and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII
  - — Flexible configuration for multiple PHY interface configurations. See Section 8.1, "Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1Gb Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics," for more information.
  - — TCP/IP acceleration and QoS features available
    - – IP v4 and IP v6 header recognition on receive
    - – IP v4 header checksum verification and generation
    - – TCP and UDP checksum verification and generation
    - – Per-packet configurable acceleration
    - – Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std 802.2™, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - – Supported in all FIFO modes
  - — Quality of service support:
    - – Transmission from up to eight physical queues
    - – Reception to up to eight physical queues
  - — Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - – IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - — Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std. 802.1™ virtual local area network (VLAN) tags and priority
  - — VLAN insertion and deletion
    - – Per-frame VLAN control word or default VLAN for each eTSEC
    - – Extracted VLAN control word passed to software separately
  - — Retransmission following a collision
  - — CRC generation and verification of inbound/outbound frames
  - — Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - — MAC address recognition:
    - – Exact match on primary and virtual 48-bit unicast addresses

- — Single inbound doorbell message structure
- — Facility to accept port-write messages
- PCI Express interface
  - — PCI Express 1.0a compatible
  - — Supports x8,x4,x2, and x1 link widths
  - — Auto-detection of number of connected lanes
  - — Selectable operation as root complex or endpoint
  - — Both 32- and 64-bit addressing
  - — 256-byte maximum payload size
  - — Virtual channel 0 only
  - — Traffic class 0 only
  - — Full 64-bit decode with 32-bit wide windows
- Pin multiplexing for the high-speed I/O interfaces supports one of the following configurations:
  - — 8 PCI Express
  - — 4 PCI Express and 4 serial RapidIO
- Power management
  - — Supports power saving modes: doze, nap, and sleep
  - — Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - — Supports eight 32-bit counters that count the occurrence of selected events
  - — Ability to count up to 512 counter-specific events
  - — Supports 64 reference events that can be counted on any of the eight counters
  - — Supports duration and quantity threshold counting
  - — Burstiness feature that permits counting of burst events with a programmable time between bursts
  - — Triggering and chaining capability
  - — Ability to generate an interrupt on overflow
- System access port
  - — Uses JTAG interface and a TAP controller to access entire system memory map
  - — Supports 32-bit accesses to configuration registers
  - — Supports cache-line burst accesses to main memory
  - — Supports large block (4-Kbyte) uploads and downloads
  - — Supports continuous bit streaming of entire block for fast upload and download
- JTAG boundary scan, designed to comply with IEEE Std. 1149.1™

MPC8548E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 9

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the device. The following table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.

The following table provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit
Core and platform PLL lock times	—	100	μs
Local bus PLL lock time	—	50	μs
PCI/PCI-X bus PLL lock time	—	50	μs

5.1 Power-On Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. The following table provides the power supply ramp rate specifications.

Table 10. Power Supply Ramp Rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for MVREF	—	3500	V/s	1
Required ramp rate for VDD	—	4000	V/s	1, 2

Note:

1. Maximum ramp rate from 200 to 500 mV is most critical as this range may falsely trigger the ESD circuitry.

2. VDD itself is not vulnerable to false ESD triggering; however, as per Section 22.2, "PLL Power Supply Filtering," the recommended AVDD_CORE, AVDD_PLAT, AVDD_LBIU, AVDD_PCI1 and AVDD_PCI2 filters are all connected to VDD. Their ramp rates must be equal to or less than the VDD ramp rate.

MPC8548E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 9

Figure 17 shows the RGMII and RTBI AC timing and multiplexing diagrams.
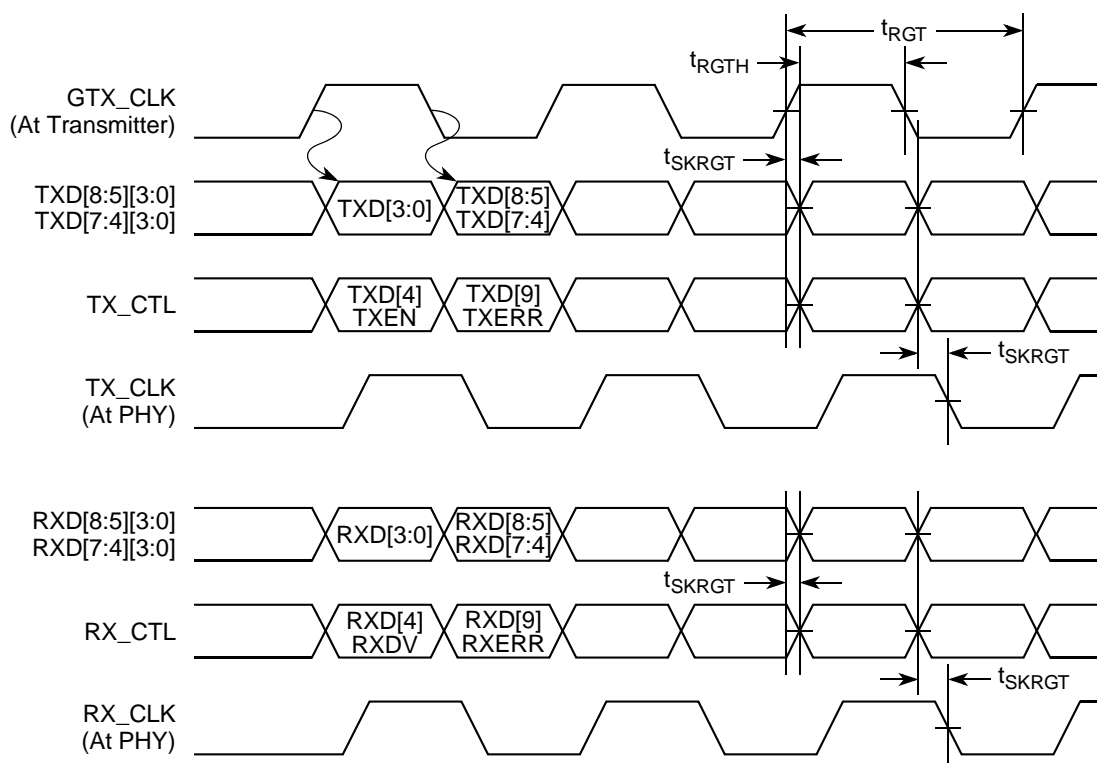

Figure 17. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7   RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1   RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in this table.

Table 34. RMII Transmit AC Timing Specifications

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TSEC*n*_TX_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
TSEC*n*_TX_CLK duty cycle	t_{RMTH}	35	50	65	%
TSEC*n*_TX_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time TSEC*n*_TX_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time TSEC*n*_TX_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

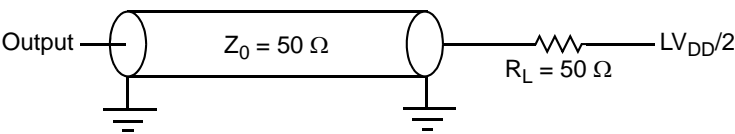Figure 19 provides the AC test load for eTSEC.

Figure 19. eTSEC AC Test Load

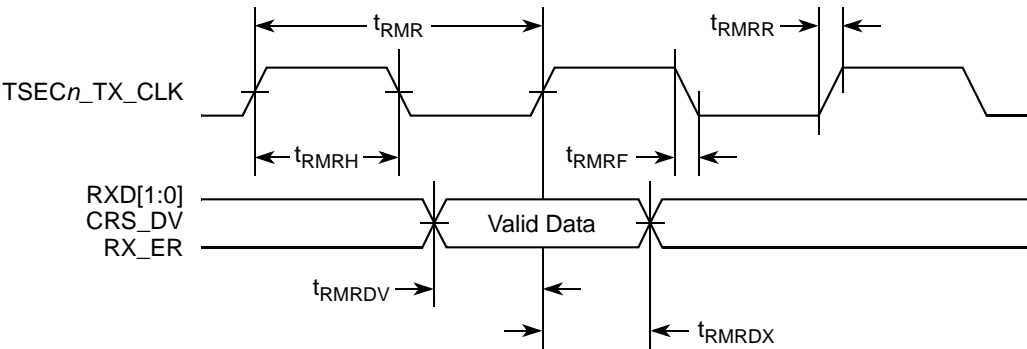Figure 20 shows the RMII receive AC timing diagram.

Figure 20. RMII Receive AC Timing Diagram

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz.
When LBIU operates above 83 MHz, LBIU PLL is recommended to be
enabled.

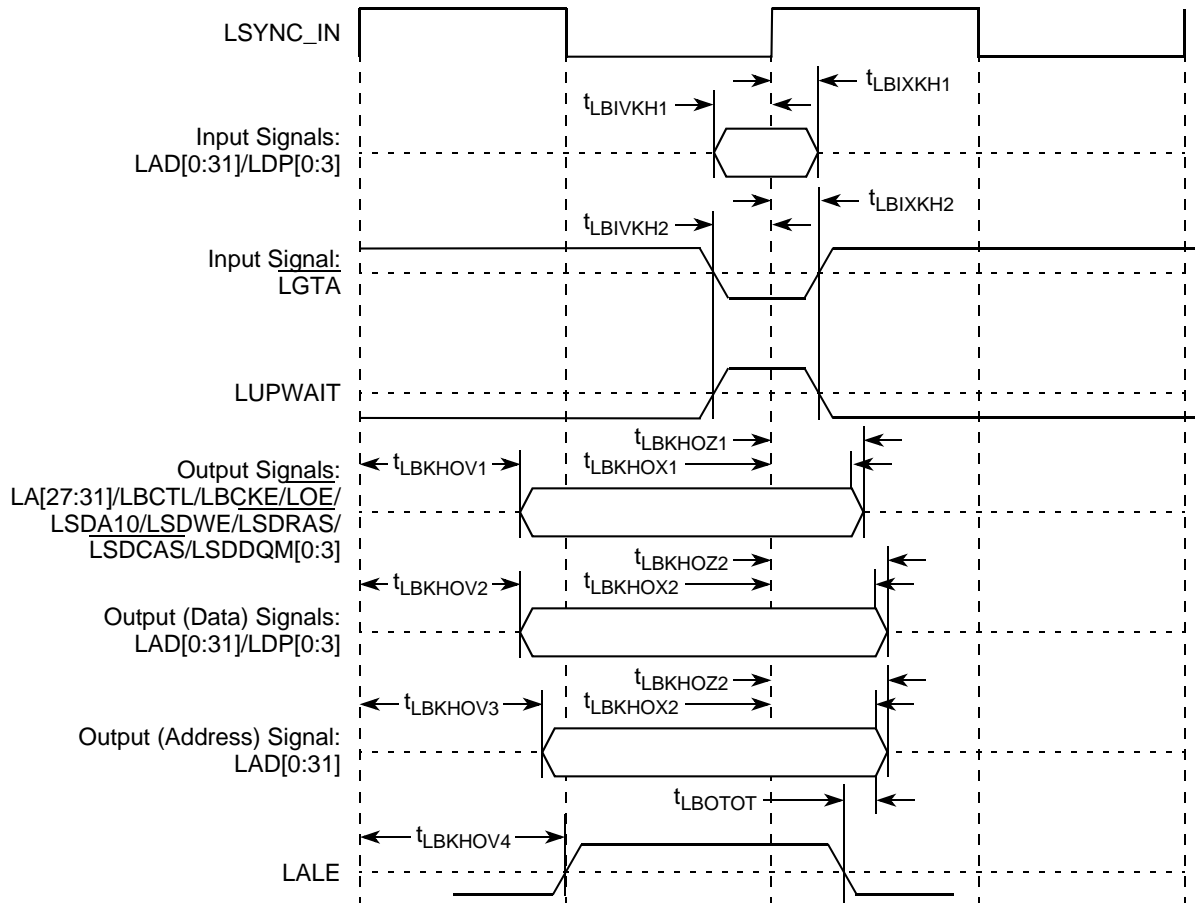Figure 23 through Figure 28 show the local bus signals.

Figure 23. Local Bus Signals (PLL Enabled)

This table describes the timing parameters of the local bus interface at $BV_{DD} = 3.3$ V with PLL disabled.

Table 42. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	4.4	ns	8
Input setup to local bus clock (except $\overline{LGTA}$/LUPWAIT)	$t_{LBIVKH1}$	6.2	—	ns	4, 5
$\overline{LGTA}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.1	—	ns	4, 5
Input hold from local bus clock (except $\overline{LGTA}$/LUPWAIT)	$t_{LBIXKH1}$	−1.8	—	ns	4, 5

Table 42. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	−1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	−0.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	−0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	−3.7	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	−3.7	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.

3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.

4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.

5. Input timings are measured at the pin.

6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.

7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

8. Guaranteed by characterization.
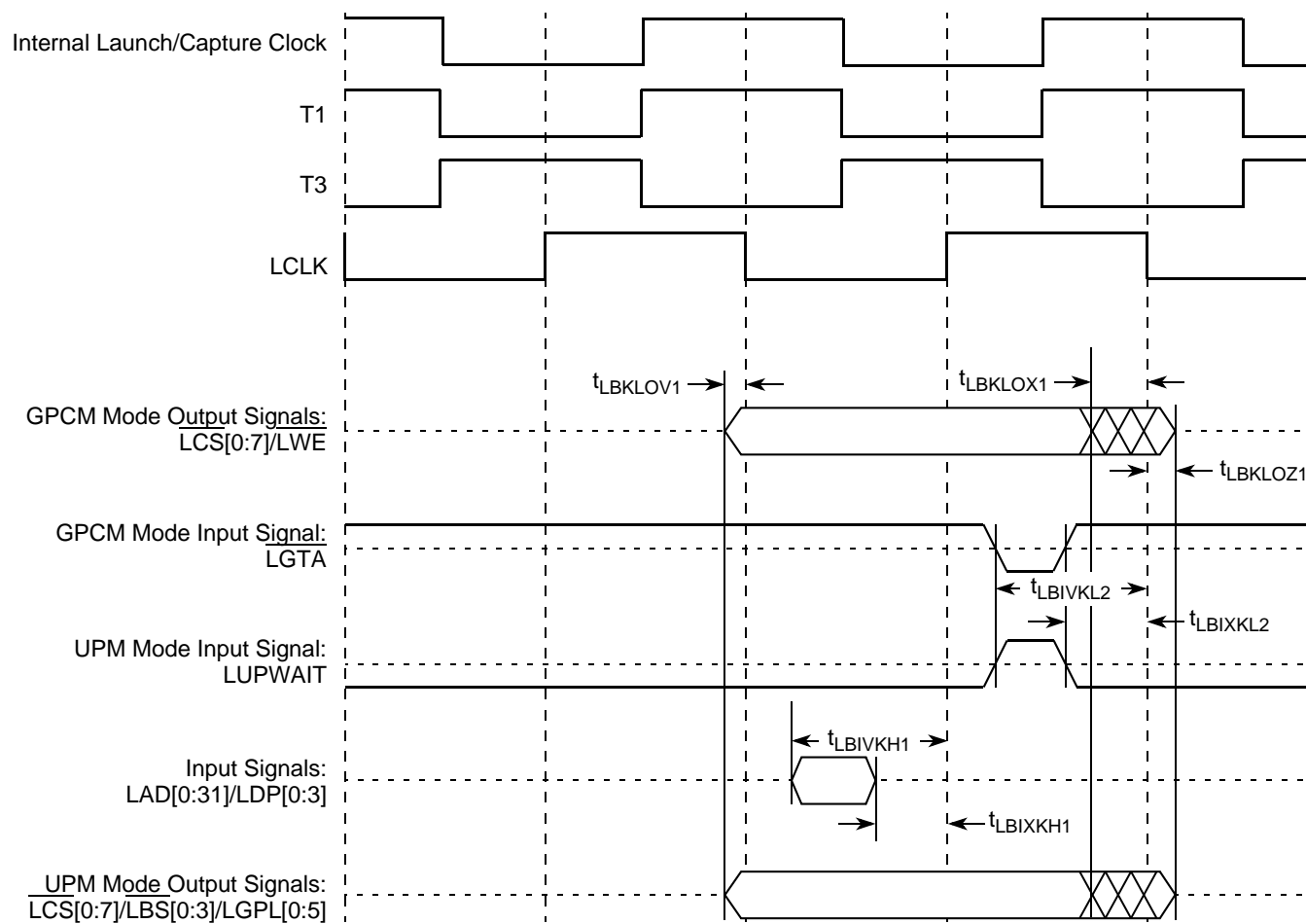
9. Guaranteed by design.

Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

Table 44. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

Parameter	Symbol[2]	Min	Max	Unit	Notes
Valid times: Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	4 2	20 10	ns	5
Output hold times: Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	30 30	— —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	3 3	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 29). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t_{TCLK}.

5. Non-JTAG signal output timing with respect to t_{TCLK}.

6. Guaranteed by design.

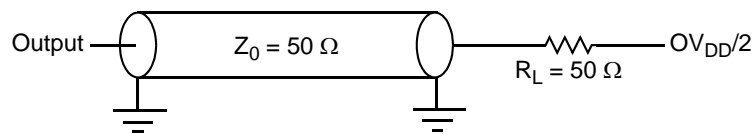Figure 29 provides the AC test load for TDO and the boundary-scan outputs.

Figure 29. AC Test Load for the JTAG Interface

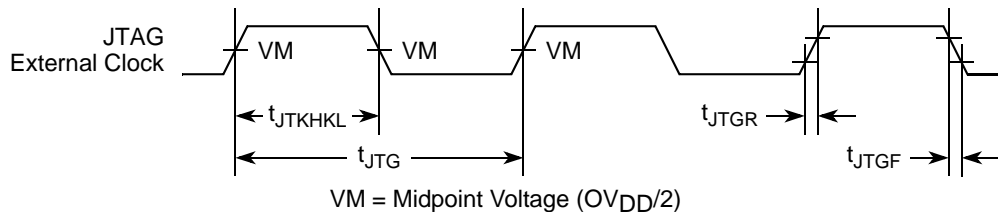Figure 30 provides the JTAG clock input timing diagram.

Figure 30. JTAG Clock Input Timing Diagram

Table 50. GP$_{IN}$ DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
Supply voltage 2.5 V	BV$_{DD}$	2.37	2.63	V
High-level input voltage	V$_{IH}$	1.70	BV$_{DD}$ + 0.3	V
Low-level input voltage	V$_{IL}$	−0.3	0.7	V
Input current (BV$_{IN}$ [1] = 0 V or BV$_{IN}$ = BV$_{DD}$)	I$_{IH}$	—	10	µA

Note:

1. The symbol BV$_{IN}$, in this case, represents the BV$_{IN}$ symbol referenced in Table 1.

15 PCI/PCI-X

This section describes the DC and AC electrical specifications for the PCI/PCI-X bus of the device.

Note that the maximum PCI-X frequency in synchronous mode is 110 MHz.

15.1 PCI/PCI-X DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI/PCI-X interface.

Table 51. PCI/PCI-X DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V$_{IH}$	2	OV$_{DD}$ + 0.3	V	—
Low-level input voltage	V$_{IL}$	−0.3	0.8	V	—
Input current (V$_{IN}$ = 0 V or V$_{IN}$ = V$_{DD}$)	I$_{IN}$	—	±5	µA	2
High-level output voltage (OV$_{DD}$ = min, I$_{OH}$ = −2 mA)	V$_{OH}$	2.4	—	V	—
Low-level output voltage (OV$_{DD}$ = min, I$_{OL}$ = 2 mA)	V$_{OL}$	—	0.4	V	—

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications.*
2. The symbol V$_{IN}$, in this case, represents the OV$_{IN}$ symbol referenced in Table 1 and Table 2.

15.2 PCI/PCI-X AC Electrical Specifications

This section describes the general AC timing parameters of the PCI/PCI-X bus. Note that the clock reference CLK is represented by SYSCLK when the PCI controller is configured for synchronous mode and by PCI*n*_CLK when it is configured for asynchronous mode.

— The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 39. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.

— The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:

— When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (see the following bullet for more detail), since the input is AC-coupled on-chip.

— This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.

— If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.

- The input amplitude requirement:

— This requirement is described in detail in the following sections.
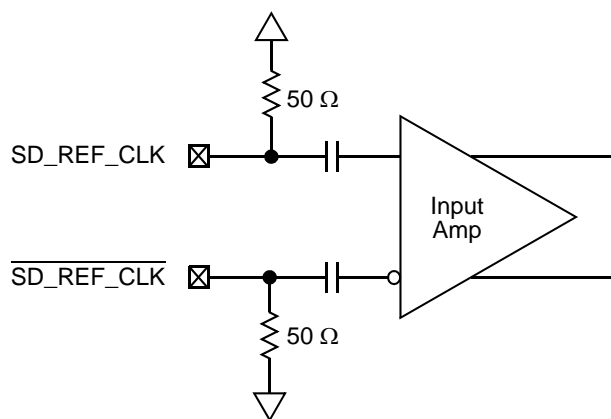

Figure 39. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below:

- Differential mode

17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8548E.

17.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see Section 16.2, "SerDes Reference Clocks."

17.2 AC Requirements for PCI Express SerDes Clocks

Table 55 lists the AC requirements for the PCI Express SerDes clocks.

Table 55. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Unit	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location.	–50	—	50	ps	—

Note:

1. Typical based on *PCI Express Specification 2.0.*

17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer see *PCI Express Base Specification. Rev. 1.0a.*

17.4.1 Differential Transmitter (TX) Output

Table 56 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 50). Note that the series capacitors, CTX, are optional for the return loss measurement.
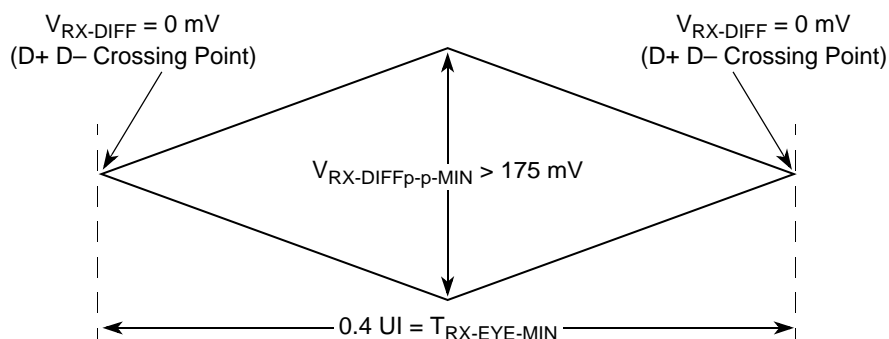
Figure 49. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 50.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

Figure 50. Compliance Test/Measurement Load

Table 72 provides the pin-out listing for the MPC8547E 783 FC-PBGA package.

NOTE

All note references in the following table use the same numbers as those for Table 71. See Table 71 for the meanings of these notes.

Table 72. MPC8547E Pinout Listing

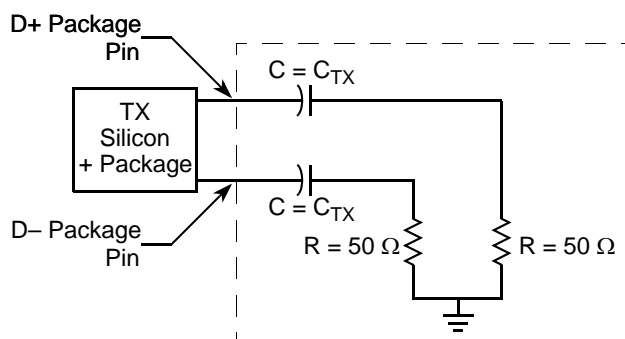| Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 (One 64-Bit or One 32-Bit)				
PCI1_AD[63:32]	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24	I/O	OV$_{DD}$	17
PCI1_AD[31:0]	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9, AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15	I/O	OV$_{DD}$	17
PCI1_C_$\overline{BE}$[7:4]	AF15, AD14, AE15, AD15	I/O	OV$_{DD}$	17
PCI1_C_$\overline{BE}$[3:0]	AF9, AD11, Y12, Y13	I/O	OV$_{DD}$	17
PCI1_PAR64	W15	I/O	OV$_{DD}$	—
$\overline{PCI1\_GNT}$[4:1]	AG6, AE6, AF5, AH5	O	OV$_{DD}$	5, 9, 35
$\overline{PCI1\_GNT0}$	AG5	I/O	OV$_{DD}$	—
$\overline{PCI1\_IRDY}$	AF11	I/O	OV$_{DD}$	2
PCI1_PAR	AD12	I/O	OV$_{DD}$	—
$\overline{PCI1\_PERR}$	AC12	I/O	OV$_{DD}$	2
$\overline{PCI1\_SERR}$	V13	I/O	OV$_{DD}$	2, 4
$\overline{PCI1\_STOP}$	W12	I/O	OV$_{DD}$	2
$\overline{PCI1\_TRDY}$	AG11	I/O	OV$_{DD}$	2
$\overline{PCI1\_REQ}$[4:1]	AH2, AG4, AG3, AH4	I	OV$_{DD}$	—
$\overline{PCI1\_REQ0}$	AH3	I/O	OV$_{DD}$	—
PCI1_CLK	AH26	I	OV$_{DD}$	39
$\overline{PCI1\_DEVSEL}$	AH11	I/O	OV$_{DD}$	2
$\overline{PCI1\_FRAME}$	AE11	I/O	OV$_{DD}$	2
PCI1_IDSEL	AG9	I	OV$_{DD}$	—
$\overline{PCI1\_REQ64}$	AF14	I/O	OV$_{DD}$	2, 5,10
$\overline{PCI1\_ACK64}$	V15	I/O	OV$_{DD}$	2
Reserved	AE28	—	—	2
Reserved	AD26	—	—	2
Reserved	AD25	—	—	2

MPC8548E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 9

Table 72. MPC8547E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Reserved	AE26	—	—	2
cfg_pci1_clk	AG24	I	OV$_{DD}$	5
Reserved	AF25	—	—	101
Reserved	AE25	—	—	2
Reserved	AG25	—	—	2
Reserved	AD24	—	—	2
Reserved	AF24	—	—	2
Reserved	AD27	—	—	2
Reserved	AD28, AE27, W17, AF26	—	—	2
Reserved	AH25	—	—	2
DDR SDRAM Memory Interface				
MDQ[0:63]	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6	I/O	GV$_{DD}$	—
MECC[0:7]	H13, F13, F11, C11, J13, G13, D12, M12	I/O	GV$_{DD}$	—
MDM[0:8]	M17, C16, K17, E16, B6, C4, H4, K1, E13	O	GV$_{DD}$	—
MDQS[0:8]	M15, A16, G17, G14, A5, D3, H1, L2, C13	I/O	GV$_{DD}$	—
$\overline{\text{MDQS}}$[0:8]	L17, B16, J16, H14, C6, C2, H3, L4, D13	I/O	GV$_{DD}$	—
MA[0:15]	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11	O	GV$_{DD}$	—
MBA[0:2]	F7, J7, M11	O	GV$_{DD}$	—
$\overline{\text{MWE}}$	E7	O	GV$_{DD}$	—
$\overline{\text{MCAS}}$	H7	O	GV$_{DD}$	—
$\overline{\text{MRAS}}$	L8	O	GV$_{DD}$	—
MCKE[0:3]	F10, C10, J11, H11	O	GV$_{DD}$	11
$\overline{\text{MCS}}$[0:3]	K8, J8, G8, F8	O	GV$_{DD}$	—
MCK[0:5]	H9, B15, G2, M9, A14, F1	O	GV$_{DD}$	—
$\overline{\text{MCK}}$[0:5]	J9, A15, G1, L9, B14, F2	O	GV$_{DD}$	—
MODT[0:3]	E6, K6, L7, M7	O	GV$_{DD}$	—
MDIC[0:1]	A19, B19	I/O	GV$_{DD}$	36

Table 73. MPC8545E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD\_TX}}$[0:3]	M23, N21, P23, R21	O	XV$_{DD}$	—
Reserved	W26, Y28, AA26, AB28	—	—	40
Reserved	W25, Y27, AA25, AB27	—	—	40
Reserved	U20, V22, W20, Y22	—	—	15
Reserved	U21, V23, W21, Y23	—	—	15
SD_PLL_TPD	U28	O	XV$_{DD}$	24
SD_REF_CLK	T28	I	XV$_{DD}$	—
$\overline{\text{SD\_REF\_CLK}}$	T27	I	XV$_{DD}$	—
Reserved	AC1, AC3	—	—	2
Reserved	M26, V28	—	—	32
Reserved	M25, V27	—	—	34
Reserved	M20, M21, T22, T23	—	—	38
General-Purpose Output				
GPOUT[24:31]	K26, K25, H27, G28, H25, J26, K24, K23	O	BV$_{DD}$	—
System Control				
$\overline{\text{HRESET}}$	AG17	I	OV$_{DD}$	—
$\overline{\text{HRESET\_REQ}}$	AG16	O	OV$_{DD}$	29
$\overline{\text{SRESET}}$	AG20	I	OV$_{DD}$	—
$\overline{\text{CKSTP\_IN}}$	AA9	I	OV$_{DD}$	—
$\overline{\text{CKSTP\_OUT}}$	AA8	O	OV$_{DD}$	2, 4
Debug				
TRIG_IN	AB2	I	OV$_{DD}$	—
TRIG_OUT/READY/$\overline{\text{QUIESCE}}$	AB1	O	OV$_{DD}$	6, 9, 19, 29
MSRCID[0:1]	AE4, AG2	O	OV$_{DD}$	5, 6, 9
MSRCID[2:4]	AF3, AF1, AF2	O	OV$_{DD}$	6, 19, 29
MDVAL	AE5	O	OV$_{DD}$	6
CLK_OUT	AE21	O	OV$_{DD}$	11
Clock				
RTC	AF16	I	OV$_{DD}$	—
SYSCLK	AH17	I	OV$_{DD}$	—
JTAG				
TCK	AG28	I	OV$_{DD}$	—
TDI	AH28	I	OV$_{DD}$	12

Table 74. MPC8543E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:5]	N9, N10, P8, N7, R9, N5	O	LV$_{DD}$	—
cfg_dram_type0/GPOUT6	R8	O	LV$_{DD}$	5, 9
GPOUT7	N6	O	LV$_{DD}$	—
Reserved	P1	—	—	104
Reserved	R6	—	—	104
Reserved	P6	—	—	15
Reserved	N4	—	—	105
FIFO1_RXC2	P5	I	LV$_{DD}$	104
Reserved	R1	—	—	104
Reserved	P10	—	—	105
FIFO1_TXC2	P7	O	LV$_{DD}$	15
cfg_dram_type1	R10	O	LV$_{DD}$	5, 9
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_TXD[3:0]	V8, W10, Y10, W7	O	TV$_{DD}$	5, 9, 29
TSEC3_RXD[3:0]	Y1, W3, W5, W4	I	TV$_{DD}$	—
TSEC3_GTX_CLK	W8	O	TV$_{DD}$	—
TSEC3_RX_CLK	W2	I	TV$_{DD}$	—
TSEC3_RX_DV	W1	I	TV$_{DD}$	—
TSEC3_RX_ER	Y2	I	TV$_{DD}$	—
TSEC3_TX_CLK	V10	I	TV$_{DD}$	—
TSEC3_TX_EN	V9	O	TV$_{DD}$	30
TSEC3_TXD[7:4]	AB8, Y7, AA7, Y8	O	TV$_{DD}$	5, 9, 29
TSEC3_RXD[7:4]	AA1, Y3, AA2, AA4	I	TV$_{DD}$	—
Reserved	AA5	—	—	15
TSEC3_COL	Y5	I	TV$_{DD}$	—
TSEC3_CRS	AA3	I/O	TV$_{DD}$	31
TSEC3_TX_ER	AB6	O	TV$_{DD}$	—
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AB3, AC5	I	OV$_{DD}$	—
$\overline{\text{UART\_RTS}}$[0:1]	AC6, AD7	O	OV$_{DD}$	—
UART_SIN[0:1]	AB5, AC7	I	OV$_{DD}$	—
UART_SOUT[0:1]	AB7, AD8	O	OV$_{DD}$	—
I^{2}C interface				
IIC1_SCL	AG22	I/O	OV$_{DD}$	4, 27

MPC8548E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 9

the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces must be kept short, wide and direct.
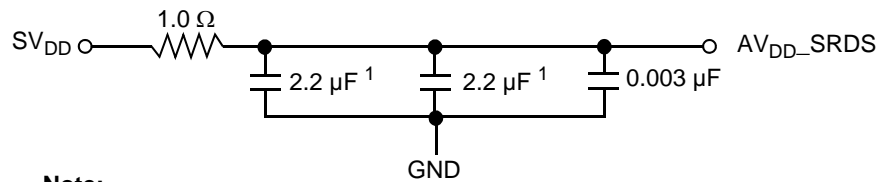
Note:
1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 60. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD}_SRDS must be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors must receive their power from separate V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors must be placed directly under the device using a standard escape pattern as much as possible. If some caps are to be placed surrounding the part it must be routed with large trace to minimize the inductance.

These capacitors must have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors must be used to minimize lead inductance, preferably 0402 or 0603 sizes. Besides, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors must have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They must also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON). However, customers must work directly with their power regulator vendor for best values, types and quantity of bulk capacitors.

22.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors must be used to minimize inductance. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.

MPC8548E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 9

Table 87. Part Numbering Nomenclature (continued)

MPC	nnnnn	t	pp	ff	c	r
Product Code	Part Identifier	Temperature	Package[1, 2, 3]	Processor Frequency[4]	Core Frequency	Silicon Version
MPC	8545E	Blank = 0 to 105°C C = −40° to 105°C	HX = CBGA VU = Pb-free CBGA PX = PBGA VT = Pb-free PBGA	AT = 1200 AQ = 1000 AN = 800	G = 400	Blank = Ver. 2.0 (SVR = 0x80390220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80390231)
	8545					Blank = Ver. 2.0 (SVR = 0x80310220) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80310231)
	8543E			AQ = 1000 AN = 800		Blank = Ver. 2.0 (SVR = 0x803A0020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x803A0031)
	8543					Blank = Ver. 2.0 (SVR = 0x80320020) A = Ver. 2.1.1 B = Ver. 2.1.2 D = Ver. 3.1.x (SVR = 0x80320031)

Notes:

1. See Section 19, "Package Description," for more information on available package types.

2. The HiCTE FC-CBGA package is available on only Version 2.0 of the device.

3. The FC-PBGA package is available on only Version 2.1.1, 2.1.2, and 2.1.3 of the device.

4. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

5. This speed available only for silicon Version 2.1.1, 2.1.2, and 2.1.3.