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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 32x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk24fn1m0vll12

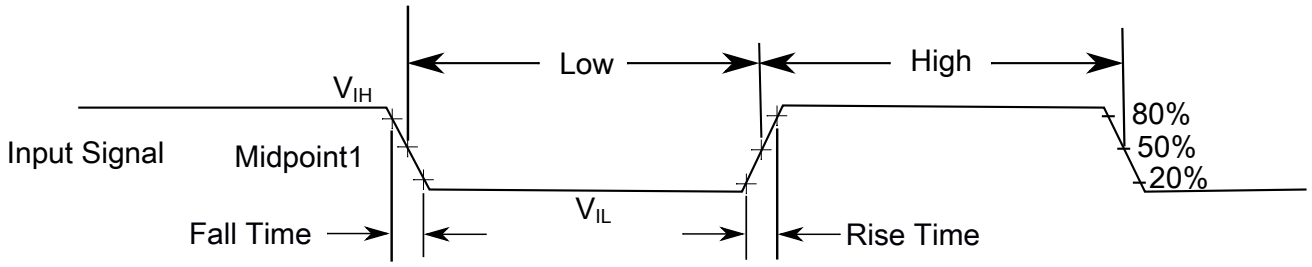
Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	–0.3	5.5	V
V_{DRTC_WAKEUP}	RTC Wakeup input voltage	–0.3	V_{BAT} + 0.3	V
V_{AIO}	Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
V_{REGIN}	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -8mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
$V_{OH\_RTC\_WAKEUP}$	Output high voltage — high drive strength	V_{BAT} – 0.5	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA	V_{BAT} – 0.5	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA				
	Output high voltage — low drive strength	V_{BAT} – 0.5	—	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA	V_{BAT} – 0.5	—	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA				
$I_{OH\_RTC\_WAKEUP}$	Output high current total for RTC_WAKEUP pins	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
$V_{OL\_RTC\_WAKEUP}$	Output low voltage — high drive strength	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA				
	Output low voltage — low drive strength	—	0.5	V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA	—	0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA				
$I_{OL\_RTC\_WAKEUP}$	Output low current total for RTC_WAKEUP pins	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	1
I_{IN}	Input leakage current (per pin) at 25°C	—	0.025	µA	1
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) for full temperature range	—	1	µA	
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) at 25°C	—	0.025	µA	

Table continues on the next page...

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	31.1	36.65	mA	
	• @ 3.0V	—	31	36.75	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	42.7	48.35	mA	
	• @ 3.0V					
	• @ 25°C	—	40	41.60	mA	
	• @ 105°C	—	48.33	51.50	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	17.9	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	6.9	—	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.0	—	mA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.7	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.678	—	mA	8
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.49	1.24	mA	
	• @ 70°C	—	1.18	4.3	mA	
	• @ 105°C	—	3.0	12.5	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	57	139.31	µA	
	• @ 70°C	—	291	679.33	µA	
	• @ 105°C	—	927.3	1869.85	µA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					9

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ –40 to 25°C	—	5.8	10.48	µA	
	• @ 70°C	—	26.7	47.99	µA	
	• @ 105°C	—	114.9	196.49	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25°C	—	4.4	5.54	µA	
	• @ 70°C	—	21	36.46	µA	
	• @ 105°C	—	90.2	150.17	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.1	2.34	µA	
	• @ 70°C	—	6.84	10.36	µA	
	• @ 105°C	—	29.4	46.74	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	0.817	0.86	µA	
	• @ 70°C	—	3.97	5.77	µA	
	• @ 105°C	—	21.3	33.99	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	0.52	0.62	µA	
	• @ 70°C	—	3.67	5.7	µA	
	• @ 105°C	—	21.20	34.9	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	0.339	0.412	µA	
	• @ 70°C	—	3.36	4.2	µA	
	• @ 105°C	—	20.3	29.9	µA	
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled					
	• @ 1.8 V					
	— • @ –40 to 25°C	—	0.16	0.19	µA	
	— • @ 70°C	—	0.55	0.72	µA	
	— • @ 105°C	—	2.5	3.68	µA	
	• @ 3.0 V					
	— • @ –40 to 25°C	—	0.18	0.21	µA	
	— • @ 70°C	—	0.66	0.86	µA	
	— • @ 105°C	—	2.92	4.30	µA	

Table continues on the next page...

Table 10. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{BUS}	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	0.8	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
$f_{FlexCAN\_ERCLK}$	FlexCAN external reference clock	—	8	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, timers, and I^2C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) - 3 V				4
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	8	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	18	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	12	ns	
	Port rise and fall time (high drive strength) - 5 V				4
	• Slew disabled				

Table continues on the next page...

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA}$ x chip power dissipation

2.4.2 Thermal attributes

Table 13. Thermal attributes

Board type	Symbol	Description	144 LQFP	121 XFBGA	100 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	51	33.3	51	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	43	21.1	39	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	26.2	41	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	17.8	32	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	30	16.3	24	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	11	12	11	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	0.2	2	°C/W	4

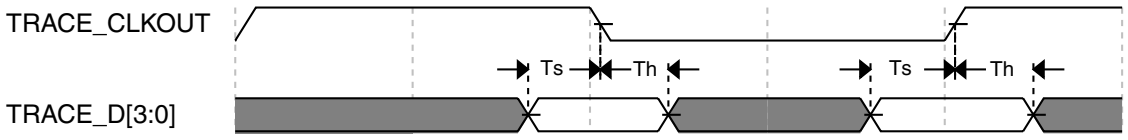


Figure 6. Trace data specifications

3.1.2 JTAG electricals

Table 15. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.6	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 16. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Table continues on the next page...

Table 18. IRC48M specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0 to 85 °C • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.0	$\%f_{irc48m}$	1
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	2
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	3

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma)
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting USB_CLK_RECOVER_IRC_EN[IRC_EN]=1.

3.3.3 Oscillator electrical specifications

3.3.3.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	

Table continues on the next page...

Table 21. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.4.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.4 Memories and memory interfaces

3.4.1 Flash (FTFE) electrical specifications

This section describes the electrical characteristics of the FTFE module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	416	3616	ms	1

3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 30 and Table 31 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.6.1.1 16-bit ADC operating conditions

Table 30. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

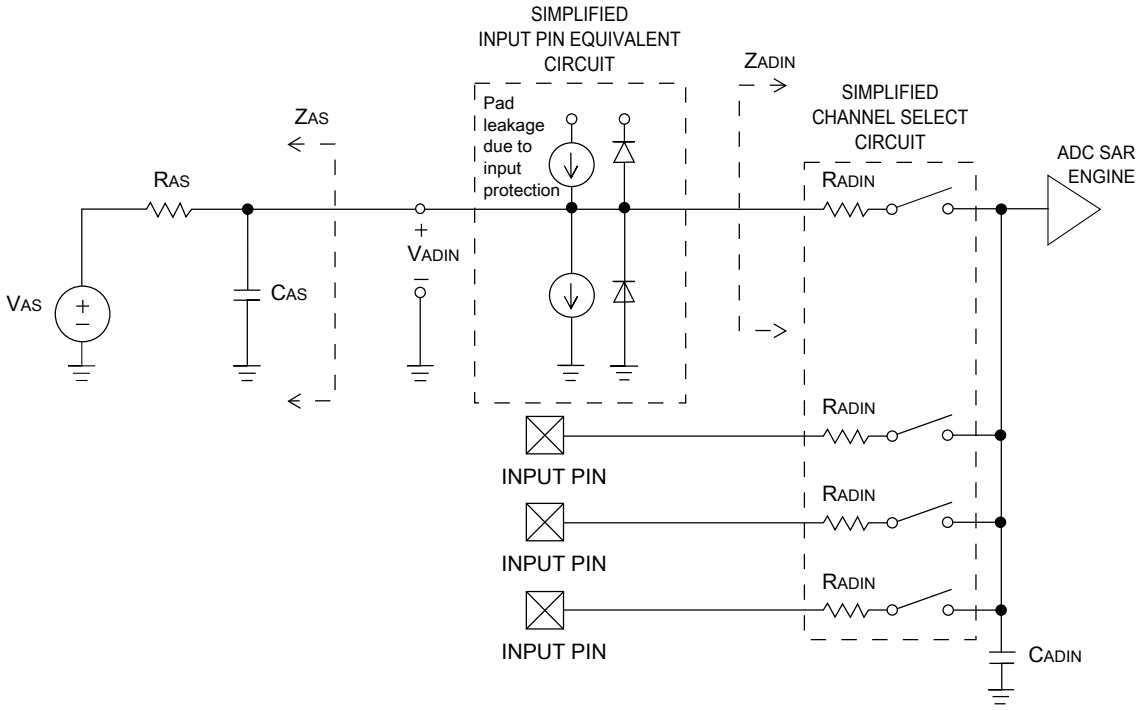


Figure 14. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 31. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					

Table continues on the next page...

Table 31. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — — 	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and

Table continues on the next page...

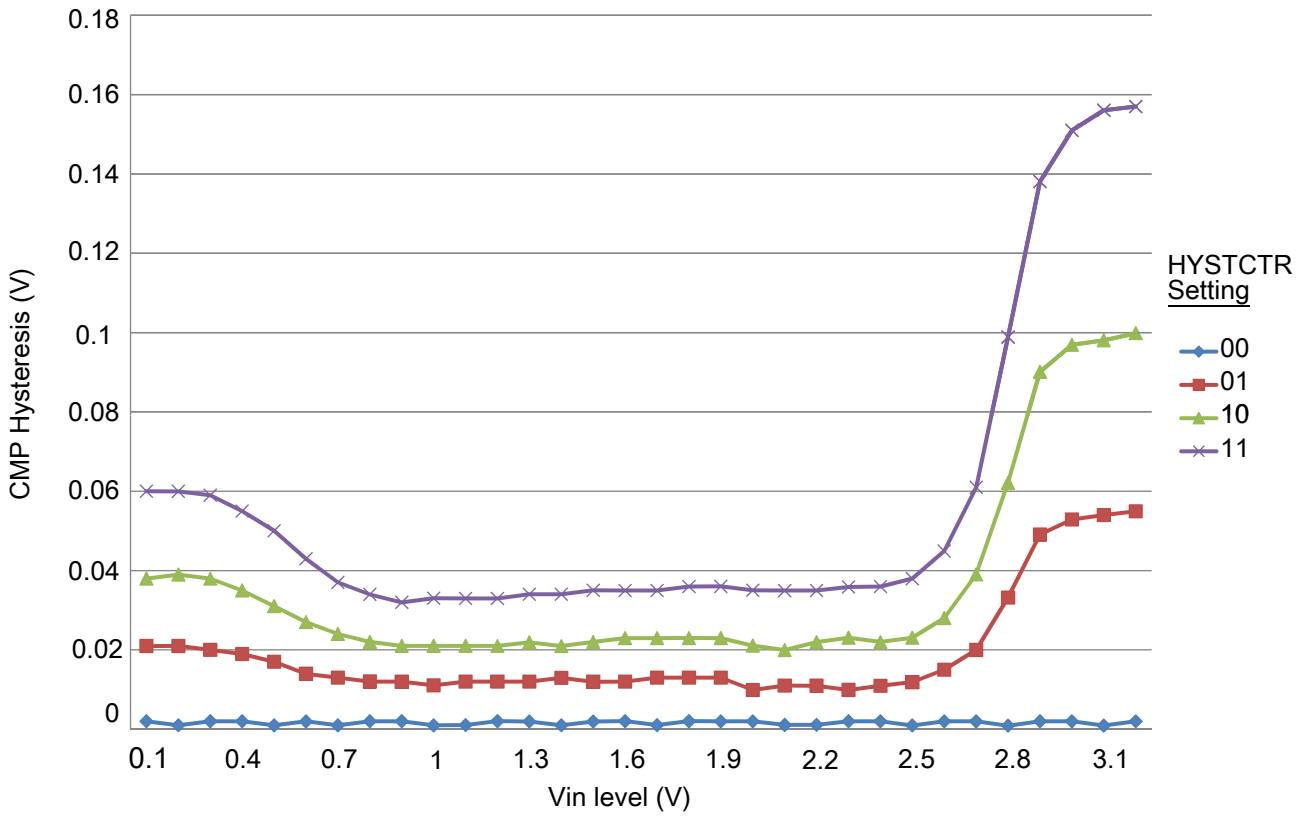


Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

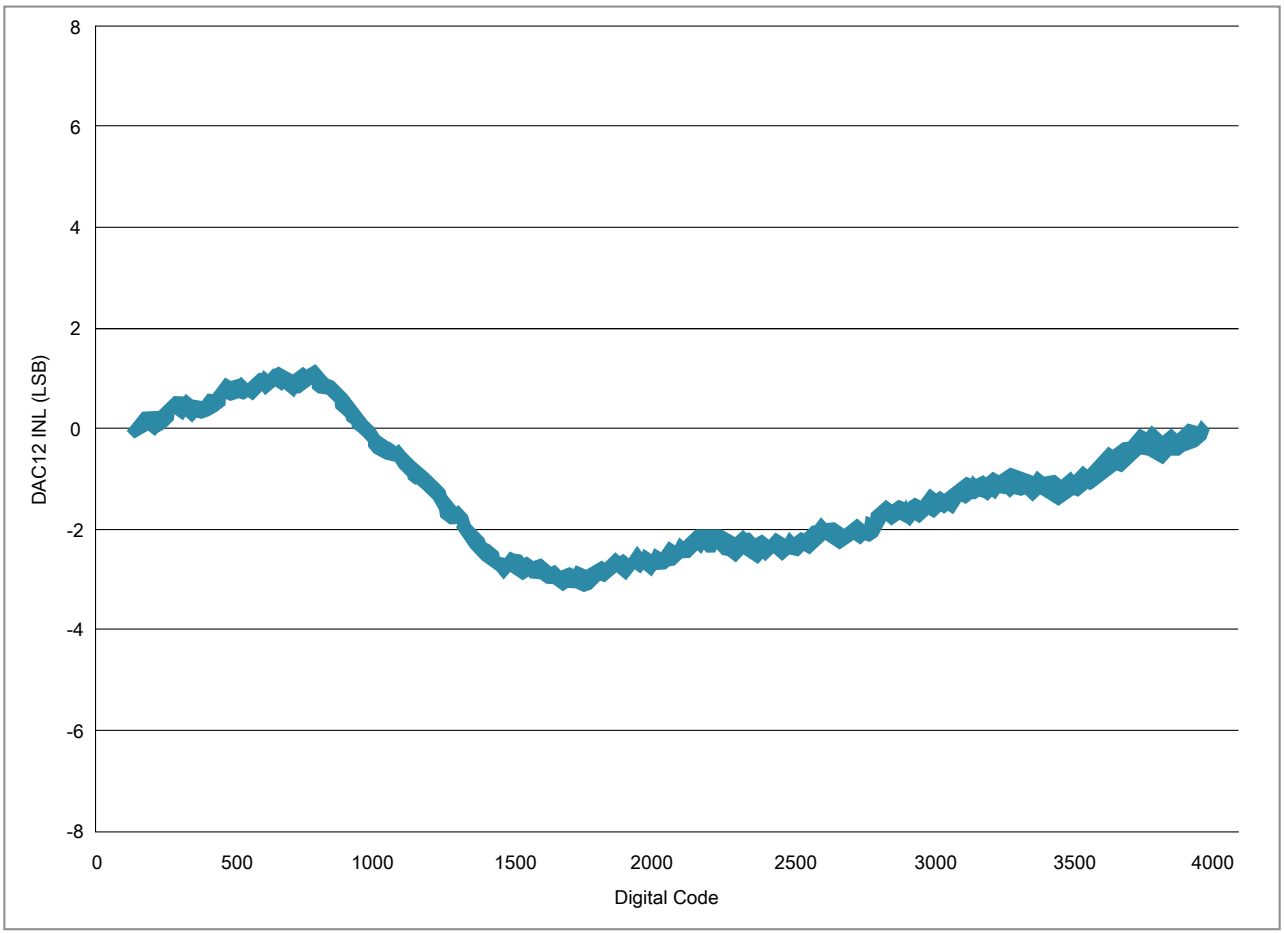


Figure 19. Typical INL error vs. digital code

Table 40. USB VREG electrical specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.8.4 CAN switching specifications

See General switching specifications.

Table 43. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	21	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

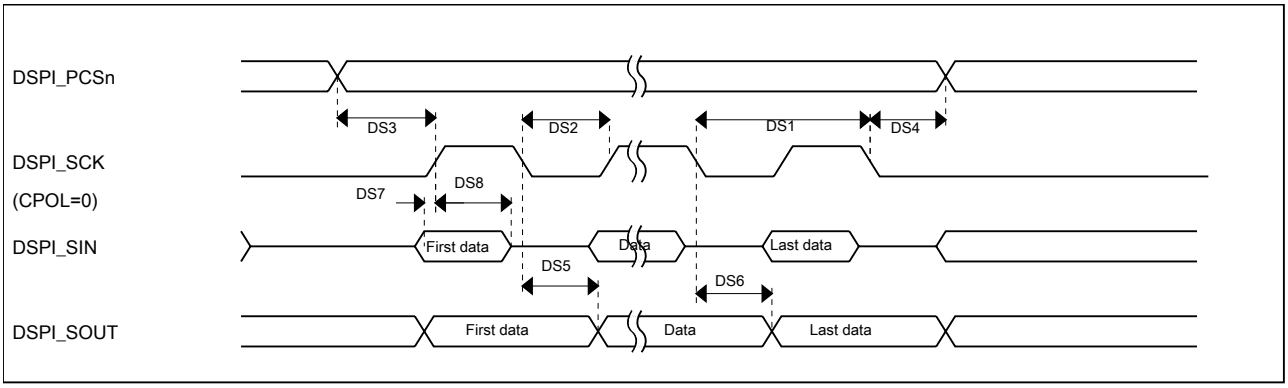


Figure 23. DSPI classic SPI timing — master mode

Table 44. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	4	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	21	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

144 QFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
6	—	VSS	VSS										
7	5	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3	TRACE_D0				LLWU_P2	
8	6	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0				
9	7	DISABLED		PTE6/ x_LLWU_ P16	SPI1_PCS3	UART3_ CTS_b	I2S0_MCLK		FTM3_CH1	USB_SOF_ OUT		x_LLWU_ P16	
10	—	DISABLED		PTE7		UART3_ RTS_b	I2S0_RXD0		FTM3_CH2				
11	—	DISABLED		PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_ FS		FTM3_CH3				
12	—	DISABLED		PTE9/ x_LLWU_ P17	I2S0_TXD1	UART5_RX	I2S0_RX_ BCLK		FTM3_CH4			x_LLWU_ P17	
13	—	DISABLED		PTE10/ x_LLWU_ P18		UART5_ CTS_b	I2S0_TXD0		FTM3_CH5			x_LLWU_ P18	
14	—	DISABLED		PTE11		UART5_ RTS_b	I2S0_TX_ FS		FTM3_CH6				
15	—	DISABLED		PTE12			I2S0_TX_ BCLK		FTM3_CH7				
16	8	VDD	VDD										
17	9	VSS	VSS										
18	—	VSS	VSS										
19	10	USB0_DP	USB0_DP										
20	11	USB0_DM	USB0_DM										
21	12	VOUT33	VOUT33										
22	13	VREGIN	VREGIN										
23	14	ADC0_DP1	ADC0_DP1										
24	15	ADC0_DM1	ADC0_DM1										
25	16	ADC1_DP1	ADC1_DP1										
26	17	ADC1_DM1	ADC1_DM1										
27	18	ADC0_ DP0/ ADC1_DP3	ADC0_ DP0/ ADC1_DP3										
28	19	ADC0_ DM0/ ADC1_DM3	ADC0_ DM0/ ADC1_DM3										
29	20	ADC1_ DP0/ ADC0_DP3	ADC1_ DP0/ ADC0_DP3										
30	21	ADC1_ DM0/ ADC0_DM3	ADC1_ DM0/ ADC0_DM3										
31	22	VDDA	VDDA										

144 QFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
32	23	VREFH	VREFH										
33	24	VREFL	VREFL										
34	25	VSSA	VSSA										
35	—	ADC1_ SE16/ CMP2_IN2/ ADC0_ SE22	ADC1_ SE16/ CMP2_IN2/ ADC0_ SE22										
36	—	ADC0_ SE16/ CMP1_IN2/ ADC0_ SE21	ADC0_ SE16/ CMP1_IN2/ ADC0_ SE21										
37	26	VREF_ OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_ SE18	VREF_ OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_ SE18										
38	27	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23	DAC0_ OUT/ CMP1_IN3/ ADC0_ SE23										
39	—	DAC1_ OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_ SE23	DAC1_ OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_ SE23										
40	28	XTAL32	XTAL32										
41	29	EXTAL32	EXTAL32										
42	30	VBAT	VBAT										
43	—	VDD	VDD										
44	—	VSS	VSS										
45	31	ADC0_ SE17	ADC0_ SE17	PTE24		UART4_TX		I2C0_SCL	EWM_ OUT_b				
46	32	ADC0_ SE18	ADC0_ SE18	PTE25/ x_LLWU_ P21		UART4_RX		I2C0_SDA	EWM_IN			x_LLWU_ P21	
47	33	DISABLED		PTE26	ENET_ 1588_ CLKIN	UART4_ CTS_b			RTC_ CLKOUT	USB_ CLKIN			
48	—	DISABLED		PTE27		UART4_ RTS_b							
49	—	DISABLED		PTE28									

144 QFP	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
68	46	DISABLED		PTA16	SPI0_ SOUT	UART0_ CTS_b/ UART0_ COL_b	RMII0_ TXD0/ MII0_TXD0		I2S0_RX_ FS	I2S0_RXD1			
69	47	ADC1_ SE17	ADC1_ SE17	PTA17	SPI0_SIN	UART0_ RTS_b	RMII0_ TXD1/ MII0_TXD1		I2S0_MCLK				
70	48	VDD	VDD										
71	49	VSS	VSS										
72	50	EXTAL0	EXTAL0	PTA18		FTM0_ FLT2	FTM_ CLKIN0					EXTAL0	
73	51	XTAL0	XTAL0	PTA19		FTM1_ FLT0	FTM_ CLKIN1		LPTMR0_ ALT1			LPTMR0_ ALT1	
74	52	RESET_b	RESET_b									RESET_b	
75	—	DISABLED		PTA24			MII0_TXD2		FB_A29				
76	—	DISABLED		PTA25			MII0_ TXCLK		FB_A28				
77	—	DISABLED		PTA26			MII0_TXD3		FB_A27				
78	—	DISABLED		PTA27			MII0_CRS		FB_A26				
79	—	DISABLED		PTA28			MII0_TXER		FB_A25				
80	—	DISABLED		PTA29			MII0_COL		FB_A24				
81	53	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0	RMII0_ MDIO/ MII0_MDIO		FTM1_QD_ PHA			LLWU_P5	
82	54	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1	RMII0_ MDC/ MII0_MDC		FTM1_QD_ PHB				
83	55	ADC0_ SE12	ADC0_ SE12	PTB2	I2C0_SCL	UART0_ RTS_b	ENET0_ 1588_ TMR0		FTM0_ FLT3				
84	56	ADC0_ SE13	ADC0_ SE13	PTB3	I2C0_SDA	UART0_ CTS_b/ UART0_ COL_b	ENET0_ 1588_ TMR1		FTM0_ FLT0				
85	—	ADC1_ SE10	ADC1_ SE10	PTB4			ENET0_ 1588_ TMR2		FTM1_ FLT0				
86	—	ADC1_ SE11	ADC1_ SE11	PTB5			ENET0_ 1588_ TMR3		FTM2_ FLT0				
87	—	ADC1_ SE12	ADC1_ SE12	PTB6				FB_AD23					
88	—	ADC1_ SE13	ADC1_ SE13	PTB7				FB_AD22					
89	—	DISABLED		PTB8		UART3_ RTS_b		FB_AD21					

9 Revision History

The following table provides a revision history for this document.

Table 55. Revision History

Rev. No.	Date	Substantial Changes
2	01/2014	Initial public release.
3	04/2014	• Format changes
4	09/2014	• Updated Table 6 "Power consumption operating behavior." • Updated Table 17 "IRC48M specifications • Updated Table 35 "VREF full-range operating behavior"
5	12/2014	• Updated Table 6 "Power consumption operating behavior." • Added a note to the section "Power consumption operating behaviors."
6	08/2015	• Added a footnote to the maximum SCL clock frequency value in the table "I^2C timing" • Changed the title of the table "I^2C 1 MHZ timing" to "I^2C 1 Mbps timing" • Added a footnote and updated the table "IRC48M specifications" for open loop total deviation of IRC48M frequency at high voltage and low voltage. • Added a footnote on the ambient temperature entry to the section "Thermal operating requirements." • Added a note to the section "Power consumption operating behaviors" and updated values in the table "Power consumption operating behaviors." • Added a note to the maximum frequency value in the table "Slave mode DSPI timing (limited voltage range)." • Redeveloped the section "Terminology and guidelines."
7	10/2016	• Updated the values of I_{DD_STOP} and I_{DD_VLLS0} in the table "Power consumption operating behaviors"