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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 39x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx256vmb7

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3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

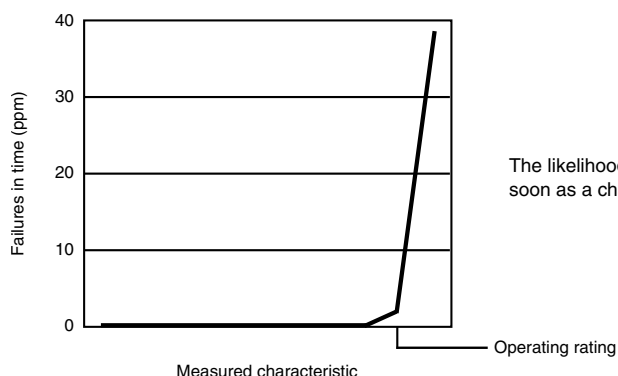
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{mA}$	$V_{DD} - 0.5$	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{mA}$	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	μA	1
I_{IN}	Input leakage current (per pin) at 25°C	—	0.025	μA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R_{PU}	Internal pullup resistors	20	50	k Ω	2
R_{PD}	Internal pulldown resistors	20	50	k Ω	3

1. Measured at $V_{DD}=3.6\text{V}$

2. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

3. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $V_{LLSx} \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 72 MHz
- Bus clock = 36 MHz
- FlexBus clock = 36 MHz
- Flash clock = 24 MHz

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.46	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.61	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ -40 to 25°C	—	0.35	0.567	mA	
	• @ 70°C	—	0.384	0.793	mA	
	• @ 105°C	—	0.628	1.2	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ -40 to 25°C	—	5.9	32.7	μA	
	• @ 70°C	—	26.1	59.8	μA	
	• @ 105°C	—	98.1	188	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ -40 to 25°C	—	2.6	8.6	μA	
	• @ 70°C	—	10.3	29.1	μA	
	• @ 105°C	—	42.5	92.5	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ -40 to 25°C	—	1.9	5.8	μA	
	• @ 70°C	—	6.9	12.1	μA	
	• @ 105°C	—	28.1	41.9	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ -40 to 25°C	—	1.59	5.5	μA	
	• @ 70°C	—	4.3	9.5	μA	
	• @ 105°C	—	17.5	34	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ -40 to 25°C	—	1.47	5.4	μA	
	• @ 70°C	—	2.97	8.1	μA	
	• @ 105°C	—	12.41	32	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ -40 to 25°C	—	0.19	0.22	μA	
	• @ 70°C	—	0.49	0.64	μA	
	• @ 105°C	—	2.2	3.2	μA	

Table continues on the next page...

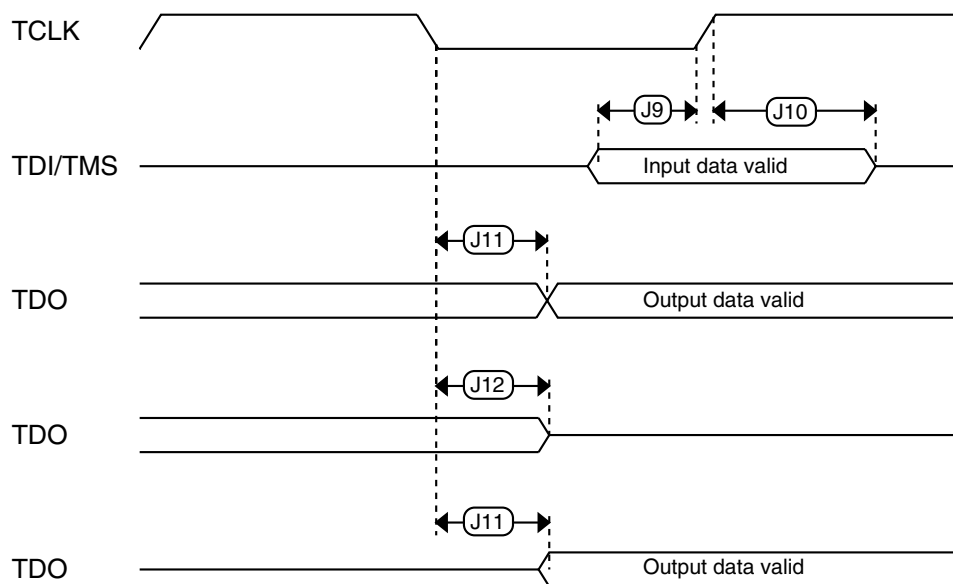


Figure 8. Test Access Port timing

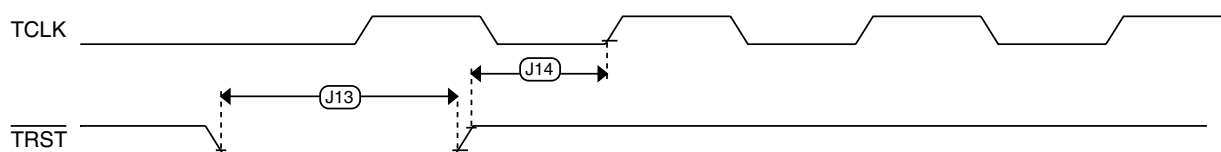


Figure 9. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

Peripheral operating requirements and behaviors

6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 14. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0) • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I _{DDOSC}	Supply current — high gain mode (HGO=1) • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz	—	25	—	μA	1
		—	400	—	μA	
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3

Table continues on the next page...

Table 19. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t _{pgmchk}	Program Check execution time	—	—	45	μs	1
t _{rdsrc}	Read Resource execution time	—	—	30	μs	1
t _{pgm4}	Program Longword execution time	—	65	145	μs	
t _{ersblk32k}	Erase Flash Block execution time 32 KB data flash	—	55	465	ms	2
t _{ersblk256k}	256 KB program flash	—	122	985	ms	
t _{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t _{pgmsec512p}	Program Section execution time 512 B program flash	—	2.4	—	ms	
t _{pgmsec512d}	512 B data flash	—	4.7	—	ms	
t _{pgmsec1kp}	1 KB program flash	—	4.7	—	ms	
t _{pgmsec1kd}	1 KB data flash	—	9.3	—	ms	
t _{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t _{rdonce}	Read Once execution time	—	—	25	μs	1
t _{pgmonce}	Program Once execution time	—	65	—	μs	
t _{ersall}	Erase All Blocks execution time	—	175	1500	ms	2
t _{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
t _{swapx01}	Swap Control execution time control code 0x01	—	200	—	μs	
t _{swapx02}	control code 0x02	—	70	150	μs	
t _{swapx04}	control code 0x04	—	70	150	μs	
t _{swapx08}	control code 0x08	—	—	30	μs	
t _{pgmpart32k}	Program Partition for EEPROM execution time 32 KB FlexNVM	—	70	—	ms	
t _{setramff}	Set FlexRAM Function execution time: Control Code 0xFF	—	50	—	μs	
t _{setram8k}	8 KB EEPROM backup	—	0.3	0.5	ms	
t _{setram32k}	32 KB EEPROM backup	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
t _{eewr8bers}	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3

Table continues on the next page...

Table 21. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Data Flash						
$t_{\text{nvmretd}10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{\text{nvmretd}1k}$	Data retention after up to 1 K cycles	20	100	—	years	
n_{nvmcyd}	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{\text{nvmretee}100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{\text{nvmretee}10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{\text{nvmwree}16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{\text{nvmwree}128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{\text{nvmwree}512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{\text{nvmwree}4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{\text{nvmwree}8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.
3. Write endurance represents the number of writes to each FlexRAM location at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes}_{\text{subsystem}} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write_efficiency} \times n_{\text{nvmcyd}}$$

where

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 23. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSI[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 24. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	13.7	—	ns	2
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWE}n}$, $\overline{\text{FB_CS}n}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSI[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 25](#) and [Table 26](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 27](#) and [Table 28](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 25. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} -V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} -V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	Reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage		V _{REFL}	—	V _{REFH}	V	
C _{ADIN}	Input capacitance	16 bit modes 8/10/12 bit modes	— —	8 4	10 5	pF	
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13/12 bit modes f _{ADCK} < 4MHz	—	—	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13 bit modes	1.0	—	18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	4

Table continues on the next page...

6.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0 • ADLPC=1, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	• 12 bit modes • <12 bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	• 12 bit modes • <12 bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	• 12 bit modes • <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	• 16 bit modes • ≤13 bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16 bit differential mode • Avg=32 • Avg=4 16 bit single-ended mode • Avg=32 • Avg=4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16 bit differential mode • Avg=32 16 bit single-ended mode • Avg=32	— —	-94 -85	— —	dB dB	7

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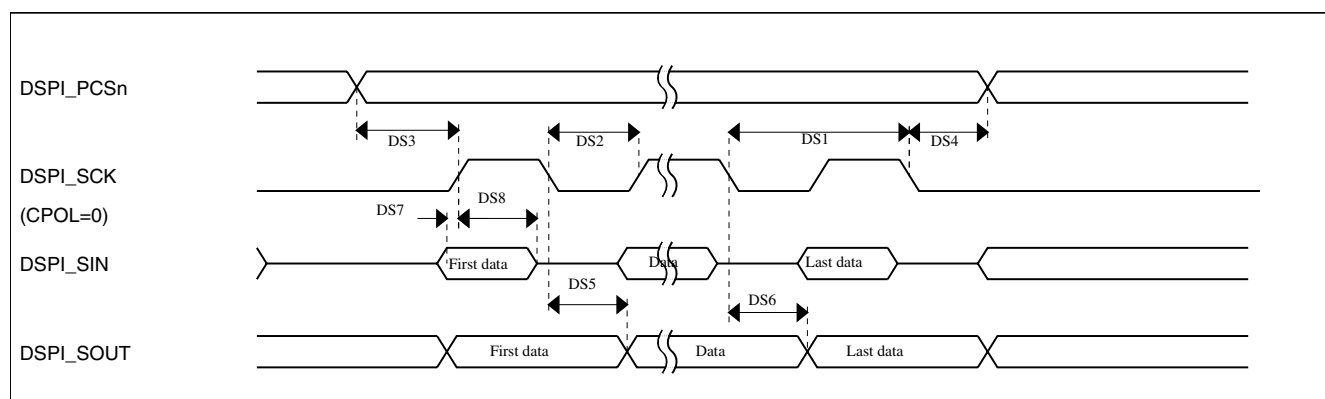


Figure 21. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI_SS}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{DSPI_SS}$ inactive to DSPI_SOUT not driven	—	14	ns

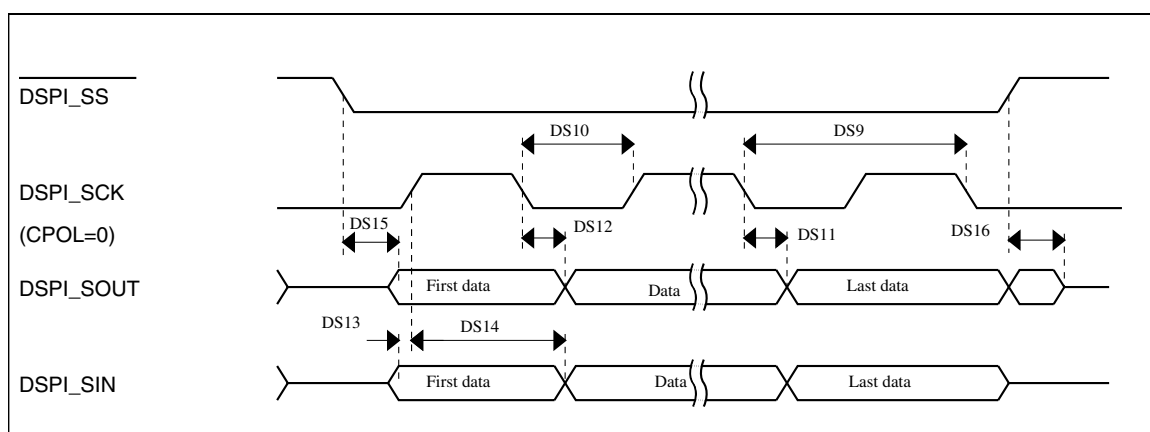


Figure 22. DSPI classic SPI timing — slave mode

6.8.6 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.6.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 41. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

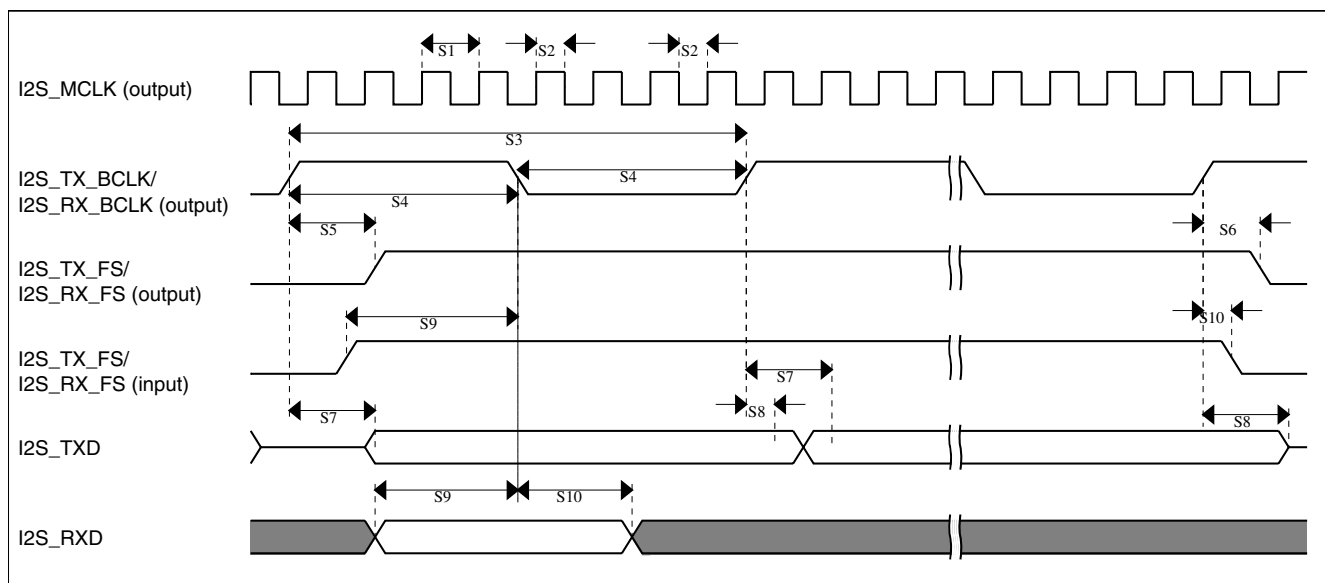


Figure 27. I2S/SAI timing — master modes

Table 44. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7.6	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	67	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	6.5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Table 45. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
T _{Con20}	Response time @ 20 pF	8	15	25	μs	12
I _{TSI_RUN}	Current added in run mode	—	55	—	μA	
I _{TSI_LP}	Low power mode current adder	—	1.3	2.5	μA	13

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. Fixed external capacitance of 20 pF.
3. REFCHRG = 2, EXTCHRG=0.
4. REFCHRG = 0, EXTCHRG = 10.
5. V_{DD} = 3.0 V.
6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; I_{ext} = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; I_{ext} = 16.
10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; I_{ext} = 16.
11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to $(C_{ref} * I_{ext}) / (I_{ref} * PS * NSCN)$. Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: I_{ext} = 6 μA (EXTCHRG = 2), PS = 128, NSCN = 2, I_{ref} = 16 μA (REFCHRG = 7), C_{ref} = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: I_{ext} = 2 μA (EXTCHRG = 0), PS = 128, NSCN = 32, I_{ref} = 32 μA (REFCHRG = 15).
12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to <http://www.freescale.com> and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
80-pin LQFP	98ASS23174W
81-pin MAPBGA	98ASA00344D

8 Pinout

8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	1	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX			I2C1_SDA	RTC_CLKOUT	
E3	2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			I2C1_SCL	SPI1_SIN	
E2	3	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b					
F4	4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b				SPI1_SOUT	
E7	—	VDD	VDD	VDD								
F7	—	VSS	VSS	VSS								
H7	5	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX					
G4	6	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX					
E6	7	VDD	VDD	VDD								
G7	8	VSS	VSS	VSS								
F1	9	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
F2	10	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ ALT3		
G1	11	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_ b	I2C0_SDA				
G2	12	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_ b	I2C0_SCL				
L6	—	VSS	VSS	VSS								
K1	13	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
K2	14	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
L1	15	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
L2	16	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
F5	17	VDDA	VDDA	VDDA								
G5	18	VREFH	VREFH	VREFH								
G6	19	VREFL	VREFL	VREFL								
F6	20	VSSA	VSSA	VSSA								

Pinout

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
L3	21	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
K5	22	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
L7	—	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
L4	23	XTAL32	XTAL32	XTAL32								
L5	24	EXTAL32	EXTAL32	EXTAL32								
K6	25	VBAT	VBAT	VBAT								
J6	26	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSIO_CH1	PTA0	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
H8	27	PTA1	JTAG_TDI/ EZP_DI	TSIO_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
J7	28	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
H9	29	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
J8	30	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
K7	31	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_TX_ BCLK	JTAG_TRST_ b	
E5	—	VDD	VDD	VDD								
G3	—	VSS	VSS	VSS								
K8	32	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
L8	33	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
K9	34	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK	I2S0_TXD1	
L9	35	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
J10	36	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b/ UART0_COL_ b			I2S0_RX_FS	I2S0_RXD1	
H10	37	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_ b			I2S0_MCLK		
L10	38	VDD	VDD	VDD								
K10	39	VSS	VSS	VSS								
L11	40	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
K11	41	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J11	42	RESET_b	RESET_b	RESET_b								
G11	43	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSIO_CH0	ADC0_SE8/ ADC1_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
G10	44	PTB1	ADC0_SE9/ ADC1_SE9/ TSIO_CH6	ADC0_SE9/ ADC1_SE9/ TSIO_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
G9	45	PTB2	ADC0_SE12/ TSIO_CH7	ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	UART0_RTS_ b			FTM0_FLT3		
G8	46	PTB3	ADC0_SE13/ TSIO_CH8	ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_ b			FTM0_FLT0		
D10	47	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
C10	48	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
—	49	VSS	VSS	VSS								
—	50	VDD	VDD	VDD								
B10	51	PTB16	TSIO_CH9	TSIO_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
E9	52	PTB17	TSIO_CH10	TSIO_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_b		
D9	53	PTB18	TSIO_CH11	TSIO_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_QD_ PHA		
C9	54	PTB19	TSIO_CH12	TSIO_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB		
B9	55	PTC0	ADC0_SE14/ TSIO_CH13	ADC0_SE14/ TSIO_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14	I2S0_TXD1		
D8	56	PTC1/ LLWU_P6	ADC0_SE15/ TSIO_CH14	ADC0_SE15/ TSIO_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0	FB_AD13	I2S0_TXD0		
C8	57	PTC2	ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1	FB_AD12	I2S0_TX_FS		
B8	58	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK		
—	59	VSS	VSS	VSS								
—	60	VDD	VDD	VDD								
A8	61	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
D7	62	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT		
C7	63	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_ BCLK	FB_AD9	I2S0_MCLK		
B7	64	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN		I2S0_RX_FS	FB_AD8			
A7	65	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK	FB_AD7			
D6	66	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK	FB_AD6	FTM2_FLT0		
C6	67	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL		I2S0_RX_FS	FB_AD5			

Table 46. Revision History (continued)

Rev. No.	Date	Substantial Changes
2	4/2012	• Replaced TBDs throughout. • Updated "Power consumption operating behaviors" table. • Updated "ADC electrical specifications" section. • Updated "VREF full-range operating behaviors" table. • Updated "I2S/SAI Switching Specifications" section. • Updated "TSI electrical specifications" table.