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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1008 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f396kpmc-g-sne2

3. Differences Among Products and Notes on Product Selection

■ Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “Electrical Characteristics”.

■ Package

For details of information on each package, see “Packages and Corresponding Products” and “Package Dimension”.

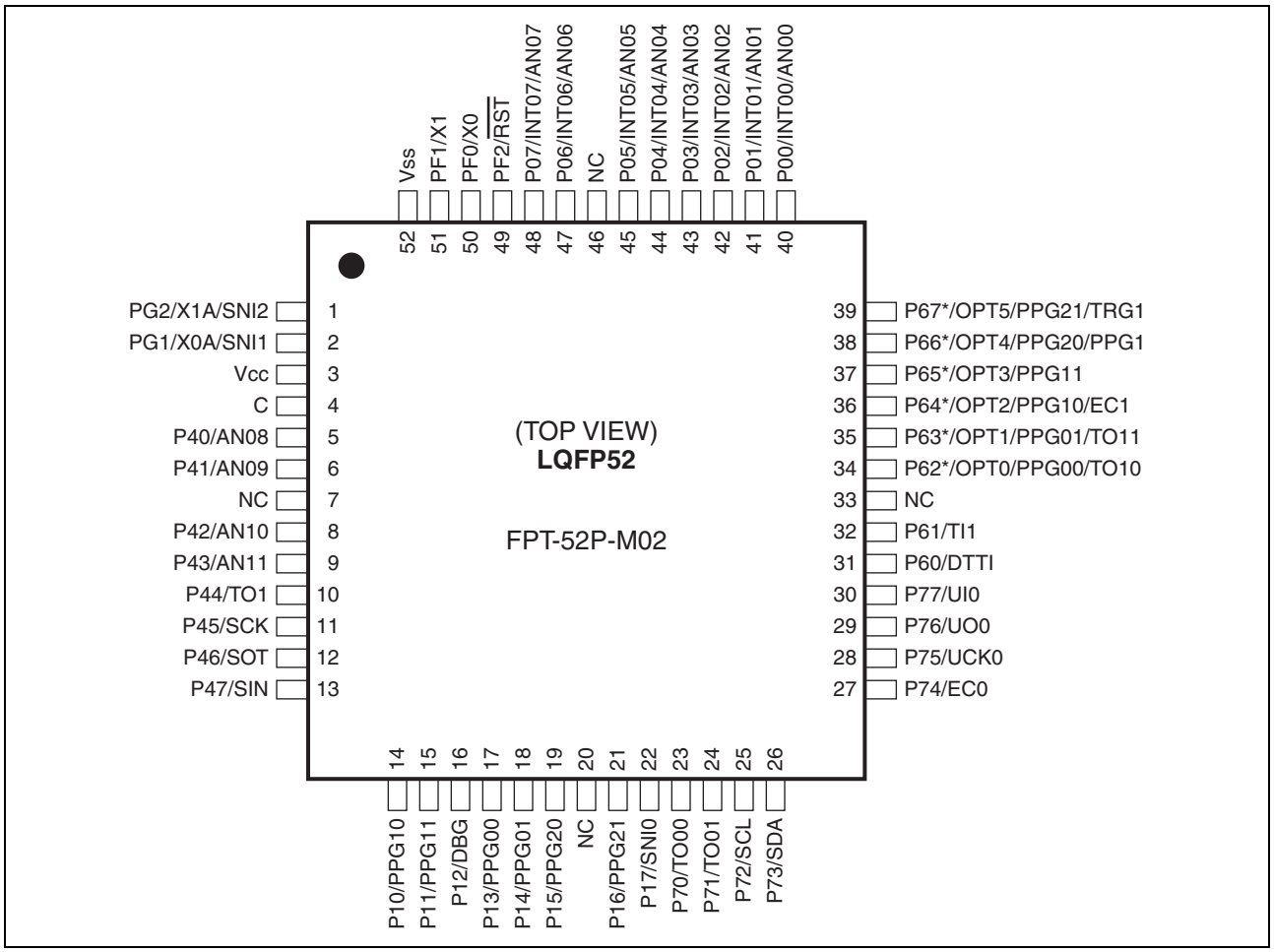
■ Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “Electrical Characteristics”.

■ On-chip debug function

The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 29 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in the hardware manual of the MB95390H Series.



*: High-current pin (8 mA/12 mA)

(Continued)

5. Pin Functions

Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
1	1	1	PG2	C	General-purpose I/O port
			X1A		Subclock I/O oscillation pin
			SNI2		Trigger input pin for the position detection function of the MPG waveform sequencer
2	2	2	PG1	C	General-purpose I/O port
			X0A		Subclock input oscillation pin
			SNI1		Trigger input pin for the position detection function of the MPG waveform sequencer
3	3	3	V_{CC}	—	Power supply pin
4	4	4	C	—	Capacitor connection pin
5	5	5	P40	K	General-purpose I/O port
			AN08		A/D converter analog input pin
6	6	6	P41	K	General-purpose I/O port
			AN09		A/D converter analog input pin
—	—	7	NC	—	It is an internally connected pin. Always leave it unconnected.
7	7	8	P42	K	General-purpose I/O port
			AN10		A/D converter analog input pin
8	8	9	P43	K	General-purpose I/O port
			AN11		A/D converter analog input pin
9	9	10	P44	G	General-purpose I/O port
			TO1		16-bit reload timer ch. 0 output pin
10	10	11	P45	G	General-purpose I/O port
			SCK		LIN-UART clock I/O pin
11	11	12	P46	G	General-purpose I/O port
			SOT		LIN-UART data output pin
12	12	13	P47	J	General-purpose I/O port
			SIN		LIN-UART data input pin
13	13	14	P10	G	General-purpose I/O port
			PPG10		8/16-bit PPG ch. 1 output pin
14	14	15	P11	G	General-purpose I/O port
			PPG11		8/16-bit PPG ch. 1 output pin
15	15	16	P12	H	General-purpose I/O port
			DBG		DBG input pin
16	16	17	P13	G	General-purpose I/O port
			PPG00		8/16-bit PPG ch. 0 output pin

(Continued)

Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
17	17	18	P14	G	General-purpose I/O port
			PPG01		8/16-bit PPG ch. 0 output pin
18	18	19	P15	G	General-purpose I/O port
			PPG20		8/16-bit PPG ch. 2 output pin
—	—	20	NC	—	It is an internally connected pin. Always leave it unconnected.
19	19	21	P16	G	General-purpose I/O port
			PPG21		8/16-bit PPG ch. 2 output pin
20	20	22	P17	G	General-purpose I/O port
			SNI0		Trigger input pin for the position detection function of the MPG waveform sequencer
21	21	23	P70	G	General-purpose I/O port
			TO00		8/16-bit composite timer ch. 0 output pin
22	22	24	P71	G	General-purpose I/O port
			TO01		8/16-bit composite timer ch. 0 output pin
23	23	25	P72	I	General-purpose I/O port
			SCL		I^2C clock I/O pin
24	24	26	P73	I	General-purpose I/O port
			SDA		I^2C data I/O pin
25	25	27	P74	G	General-purpose I/O port
			EC0		8/16-bit composite timer ch. 0 clock input pin
26	26	28	P75	G	General-purpose I/O port
			UCK0		UART/SIO ch. 0 clock I/O pin
27	27	29	P76	G	General-purpose I/O port
			UO0		UART/SIO ch. 0 data output pin
28	28	30	P77	J	General-purpose I/O port
			UI0		UART/SIO ch. 0 data input pin
29	29	31	P60	G	General-purpose I/O port
			DTTI		MPG waveform sequencer input pin
30	30	32	P61	G	General-purpose I/O port
			TI1		16-bit reload timer ch. 0 input pin
—	—	33	NC	—	It is an internally connected pin. Always leave it unconnected.
31	31	34	P62	D	General-purpose I/O port High-current pin
			OPT0		MPG waveform sequencer output pin
			PPG00		8/16-bit PPG ch. 0 output pin
			TO10		8/16-bit composite timer ch. 1 output pin

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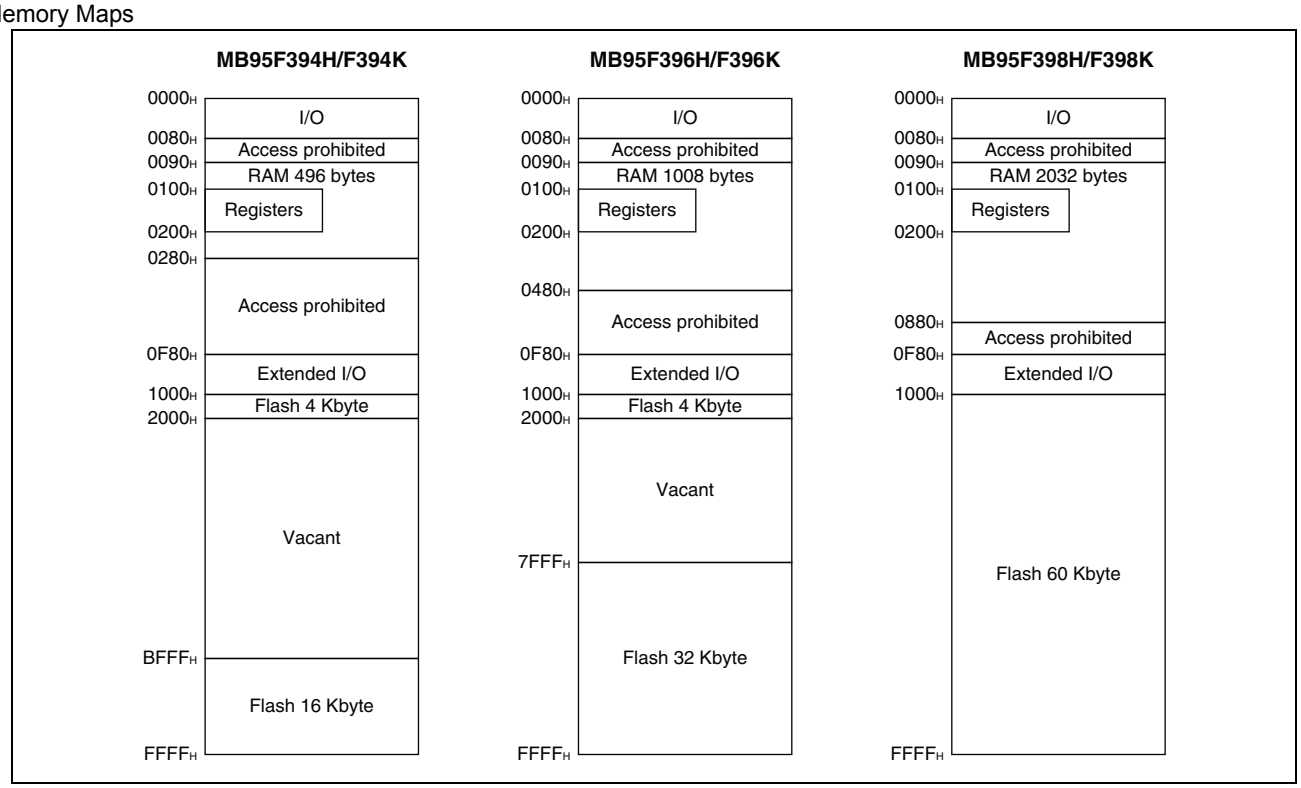
11. CPU Core

■ Memory Space

The memory space of the MB95390H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95390H Series are shown below.

■ Memory Maps



Address	Register abbreviation	Register name	R/W	Initial value
$0FAC_H$ to $0FAF_H$	—	(Disabled)	—	—
$0FB0_H$	PDCRH1	16-bit PPG down counter register (upper)	R	00000000_B
$0FB1_H$	PDCRL1	16-bit PPG down counter register (lower)	R	00000000_B
$0FB2_H$	PCSRH1	16-bit PPG cycle setting buffer register (upper)	R/W	11111111_B
$0FB3_H$	PCSRL1	16-bit PPG cycle setting buffer register (lower)	R/W	11111111_B
$0FB4_H$	PDUTH1	16-bit PPG duty setting buffer register (upper)	R/W	11111111_B
$0FB5_H$	PDUTL1	16-bit PPG duty setting buffer register (lower)	R/W	11111111_B
$0FB6_H$ to $0FBB_H$	—	(Disabled)	—	—
$0FBC_H$	BGR1	LIN-UART baud rate generator register 1	R/W	00000000_B
$0FBD_H$	BGR0	LIN-UART baud rate generator register 0	R/W	00000000_B
$0FBE_H$	PSSR0	UART/SIO prescaler select register	R/W	00000000_B
$0FBF_H$	BRSR0	UART/SIO baud rate setting register	R/W	00000000_B
$0FC0_H$, $0FC1_H$	—	(Disabled)	—	—
$0FC2_H$	AIDRH	A/D input disable register (upper)	R/W	00000000_B
$0FC3_H$	AIDRL	A/D input disable register (lower)	R/W	00000000_B
$0FC4_H$	OPDBRH0	Output data buffer register (upper) ch. 0	R/W	00000000_B
$0FC5_H$	OPDBRL0	Output data buffer register (lower) ch. 0	R/W	00000000_B
$0FC6_H$	OPDBRH1	Output data buffer register (upper) ch. 1	R/W	00000000_B
$0FC7_H$	OPDBRL1	Output data buffer register (lower) ch. 1	R/W	00000000_B
$0FC8_H$	OPDBRH2	Output data buffer register (upper) ch. 2	R/W	00000000_B
$0FC9_H$	OPDBRL2	Output data buffer register (lower) ch. 2	R/W	00000000_B
$0FCA_H$	OPDBRH3	Output data buffer register (upper) ch. 3	R/W	00000000_B
$0FCB_H$	OPDBRL3	Output data buffer register (lower) ch. 3	R/W	00000000_B
$0FCC_H$	OPDBRH4	Output data buffer register (upper) ch. 4	R/W	00000000_B
$0FCD_H$	OPDBRL4	Output data buffer register (lower) ch. 4	R/W	00000000_B
$0FCE_H$	OPDBRH5	Output data buffer register (upper) ch. 5	R/W	00000000_B
$0FCF_H$	OPDBRL5	Output data buffer register (lower) ch. 5	R/W	00000000_B
$0FD0_H$	OPDBRH6	Output data buffer register (upper) ch. 6	R/W	00000000_B
$0FD1_H$	OPDBRL6	Output data buffer register (lower) ch. 6	R/W	00000000_B
$0FD2_H$	OPDBRH7	Output data buffer register (upper) ch. 7	R/W	00000000_B
$0FD3_H$	OPDBRL7	Output data buffer register (lower) ch. 7	R/W	00000000_B
$0FD4_H$	OPDBRH8	Output data buffer register (upper) ch. 8	R/W	00000000_B
$0FD5_H$	OPDBRL8	Output data buffer register (lower) ch. 8	R/W	00000000_B
$0FD6_H$	OPDBRH9	Output data buffer register (upper) ch. 9	R/W	00000000_B
$0FD7_H$	OPDBRL9	Output data buffer register (lower) ch. 9	R/W	00000000_B
$0FD8_H$	OPDBRHA	Output data buffer register (upper) ch. A	R/W	00000000_B
$0FD9_H$	OPDBRLA	Output data buffer register (lower) ch. A	R/W	00000000_B

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14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P62 to P67
	I_{OL2}	—	15		P62 to P67
"L" level average current	I_{OLAV1}	—	4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}	—	12		P62 to P67 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	−15	mA	Other than P12, P62 to P67, P72, P73 and PF2
	I_{OH2}	—	−15		P12, P62 to P67, P72, P73 and PF2
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P12, P62 to P67, P72, P73 and PF2 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}	—	−8		P12, P62 to P67, P72, P73 and PF2 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	Tstg	−55	+150	°C	

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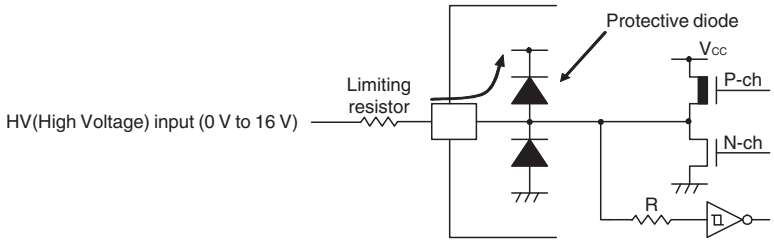
*1: The parameter is based on V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P10, P11, P13 to P17, P40 to P47, P60 to P67, P70, P71, P74 to P77, PF0, PF1, PG1 and PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit

- Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*3	Max		
"H" level input voltage	V_{IHI}	P47, P72, P73, P77	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P10 to P17, P40 to P47, P60 to P67, P70 to P77, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P47, P72, P73, P77	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P10 to P17, P40 to P47, P60 to P67, P70 to P77, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P72, P73, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P62 to P67, P72, P73, PF2	I_{OH} = −4 mA	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P62 to P67	I_{OH} = −8 mA	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P62 to P67	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P62 to P67	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	−5	—	+5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00 to P07, P10, P11, P13 to P17, P40 to P47, P60, P61, P70, P71, P74 to P76, PG1, PG2	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*3	Max		
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	
Power supply current*2	I_{CC}	V_{CC} (External clock operation)	V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	14.8	17	mA	Except during Flash memory writing and erasing
				—	33.5	39.5	mA	During Flash memory writing and erasing
				—	16.6	21	mA	At A/D conversion
	I_{CCS}		V_{CC} = 5.5 V F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	7	9	mA	
	I_{CCL}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25°C	—	60	153	µA	
	I_{CCLS}		V_{CC} = 5.5 V F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	9.4	84	µA	
	I_{CCT}		V_{CC} = 5.5 V F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	4.3	30	µA	
	I_{CCMCR}	V_{CC}	V_{CC} = 5.5 V F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode	—	11.8	13.2	mA	
	I_{CCSCR}		V_{CC} = 5.5 V Sub-CR clock mode (divided by 2) T_A = +25°C	—	113	410	µA	

(Continued)

14.4.2 Source Clock/Machine Clock

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 12.5 MHz Max: F_{CRH} = 1 MHz
			—	61	—	µs	When the sub-oscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: F_{SP} = 12.5 MHz Max: F_{SP} = 1 MHz, divided by 16
			61	—	976.5	µs	When the sub-oscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). This source clock is divided to become a machine clock according to the divide ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

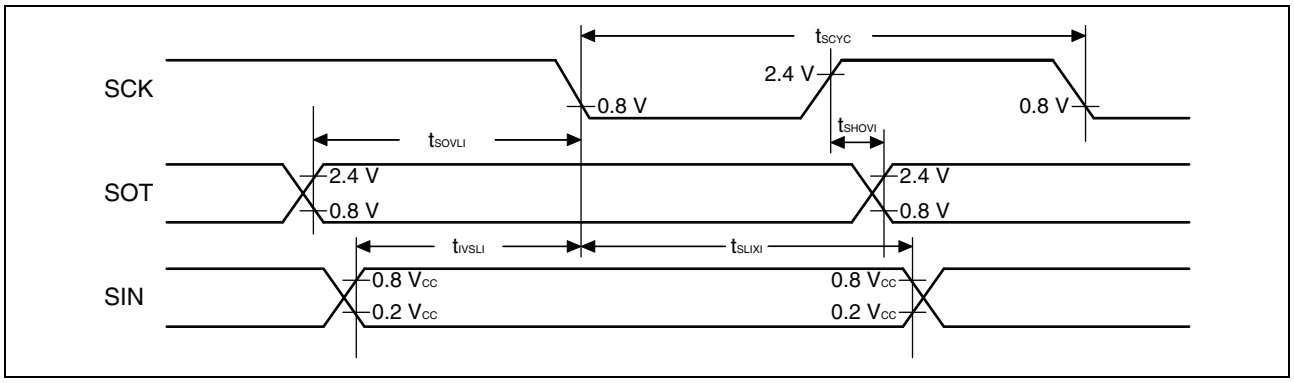
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↓ → valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.



(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		$(2\ nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3\ t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm/2)t_{MCLK} - 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to the interrupt at the 8th SCL↓.

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Sym-bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	4 t_{MCLK} − 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		4 t_{MCLK} − 20	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
STOP condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} − 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} − 3 t_{MCLK} − 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} − 20	—	ns	At reception
SDA↓ → SCL↑ (at wakeup function)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t_{MCLK} − 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2:
- See “Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I^2C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I^2C clock control register (ICCR0).
- The actual timing of I^2C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < $t_{MCLK} \leq$ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < $t_{MCLK} \leq$ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < $t_{MCLK} \leq$ 10 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < $t_{MCLK} \leq$ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < $t_{MCLK} \leq$ 10 MHz

14.5 A/D Converter

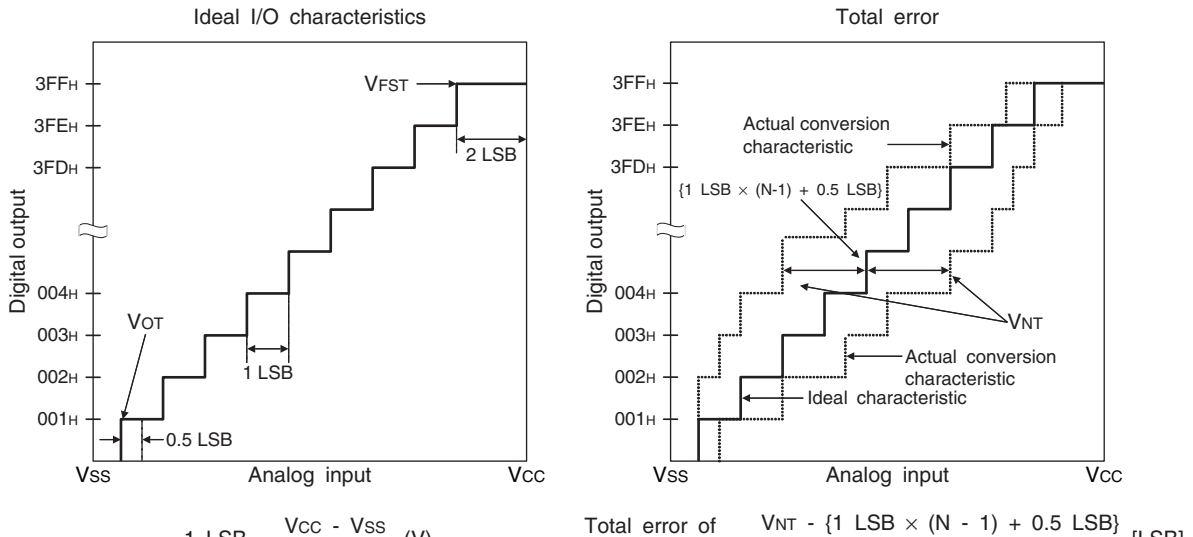
14.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		−3	—	+3	LSB	
Linearity error		−2.5	—	+2.5	LSB	
Differential linear error		−1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} − 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} − 4.5 LSB	V_{CC} − 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	−0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

14.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

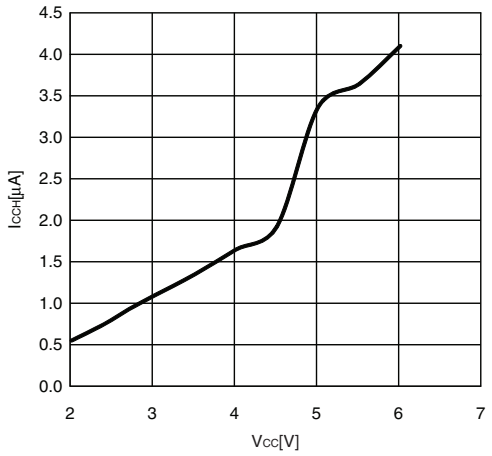
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value

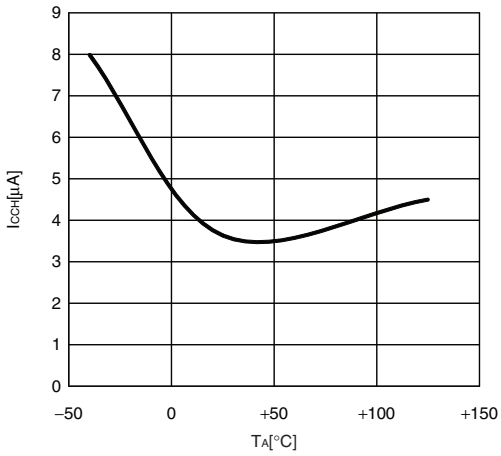
V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

(Continued)

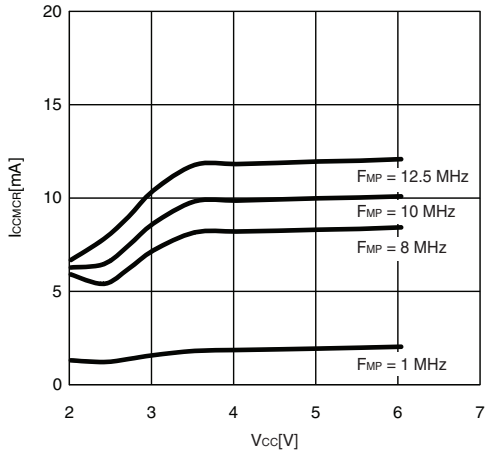
I_{CCH} – V_{CC}
T_A = +25°C, F_{MPL} = (stop)
Substop mode with the external clock stopping



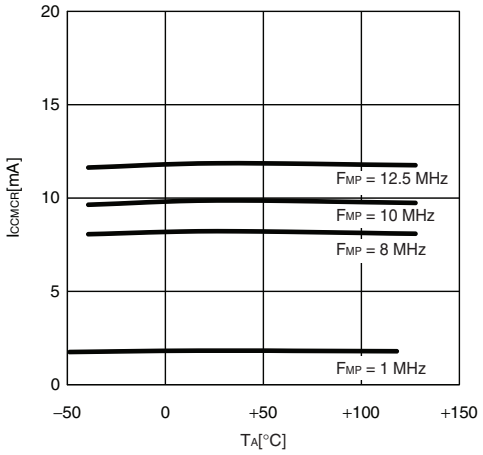
I_{CCH} – T_A
V_{CC} = 5.5 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



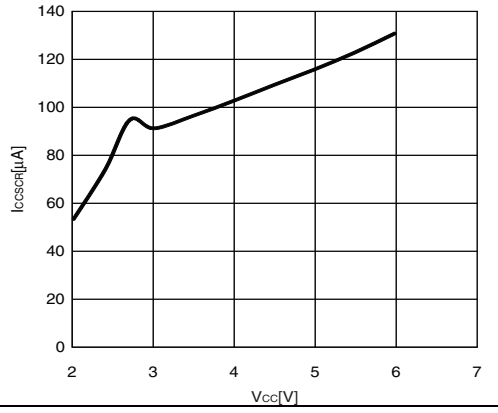
I_{CCMCR} – V_{CC}
T_A = +25°C, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



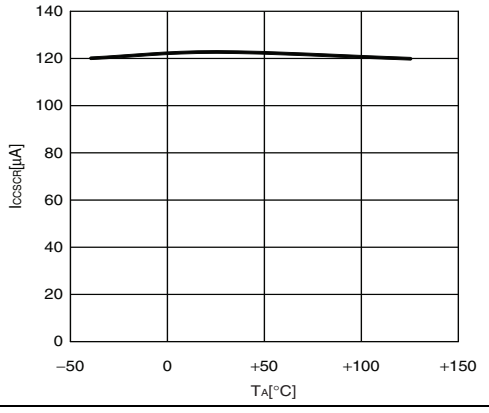
I_{CCMCR} – T_A
V_{CC} = 5.5 V, F_{MP} = 1, 8, 10, 12.5 MHz (no division)
Main clock mode with the main CR clock operating



I_{CCSCR} – V_{CC}
T_A = +25°C, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating



I_{CCSCR} – T_A
V_{CC} = 5.5 V, F_{MPL} = 50 kHz (divided by 2)
Subclock mode with the sub-CR clock operating



16. Mask Options

No.	Part Number	MB95F394H MB95F396H MB95F398H	MB95F394K MB95F396K MB95F398K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

17. Ordering Information

Part Number	Package
MB95F394HPMC-G-SNE2 MB95F394KPMC-G-SNE2 MB95F396HPMC-G-SNE2 MB95F396KPMC-G-SNE2 MB95F398HPMC-G-SNE2 MB95F398KPMC-G-SNE2	48-pin plastic LQFP (FPT-48P-M49)
MB95F394HPMC1-G-SNE2 MB95F394KPMC1-G-SNE2 MB95F396HPMC1-G-SNE2 MB95F396KPMC1-G-SNE2 MB95F398HPMC1-G-SNE2 MB95F398KPMC1-G-SNE2	52-pin plastic LQFP (FPT-52P-M02)
MB95F394HWQN-G-SNE1 MB95F394HWQN-G-SNERE1 MB95F394KWQN-G-SNE1 MB95F394KWQN-G-SNERE1 MB95F396HWQN-G-SNE1 MB95F396HWQN-G-SNERE1 MB95F396KWQN-G-SNE1 MB95F396KWQN-G-SNERE1 MB95F398HWQN-G-SNE1 MB95F398HWQN-G-SNERE1 MB95F398KWQN-G-SNE1 MB95F398KWQN-G-SNERE1	48-pin plastic QFN (LCC-48P-M11)

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