Infineon Technologies - MB95F398KPMC-G-SNE2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.98K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f398kpmc-g-sne2

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Part number / Parameter	MB95F394H	MB95F396H	MB95F398H	MB95F394K	MB95F396K	MB95F398K
UART/SIO	1 channel					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
I^2C	1 channel					
	• Master/slave transmission and receiving • It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.					
8/16-bit PPG	3 channels					
	• Each channel of PPG can be used as two 8-bit PPG channels or a single 16-bit PPG channel. • The counter operating clock can be selected from eight clock sources.					
16-bit PPG	• PWM mode and one-shot mode are available to use. • The counter operating clock can be selected from eight clock sources. • It supports external trigger start. • It can work independently or together with the multi-pulse generator.					
16-bit reload timer	• Two clock modes and two counter operating modes are available to use. • It can output square waveform. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode • It can work independently or together with the multi-pulse generator.					
Multi-pulse generator (for DC motor control)	• 16-bit PPG timer: 1 channel • 16-bit reload timer operations: toggle output, one-shot output • Event counter: 1 channel • Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, and write/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of write/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-48P-M49 FPT-52P-M02 LCC-48P-M11					

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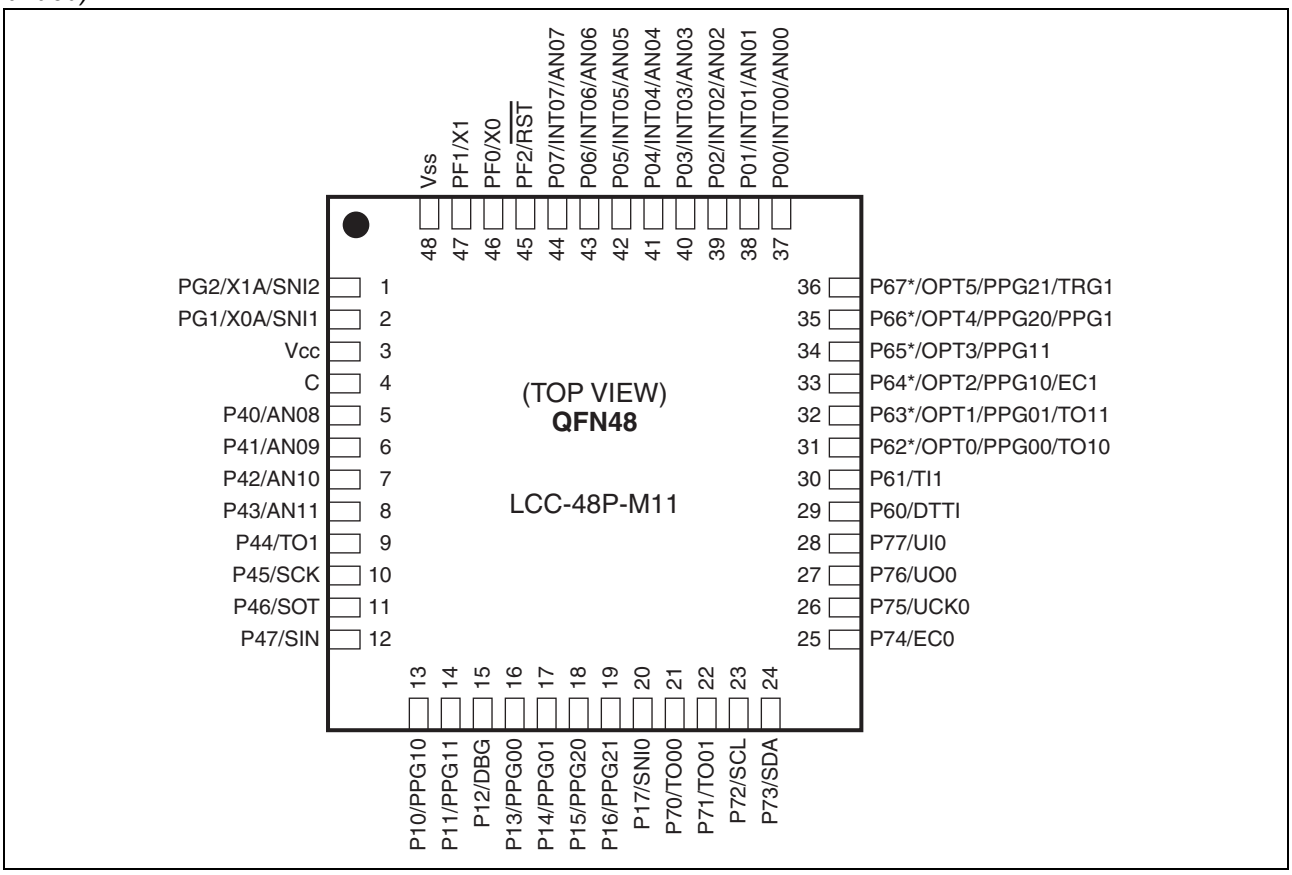

*: High-current pin (8 mA/12 mA)

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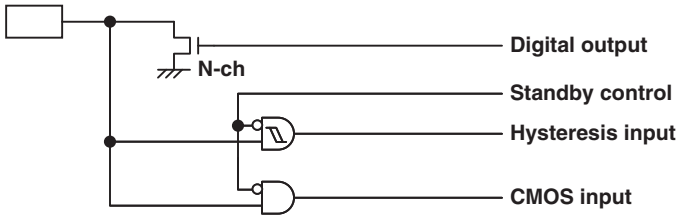
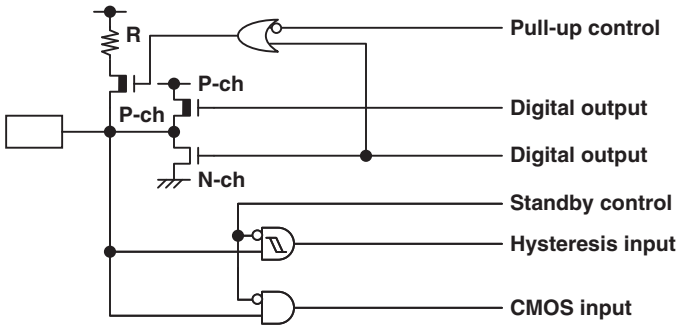
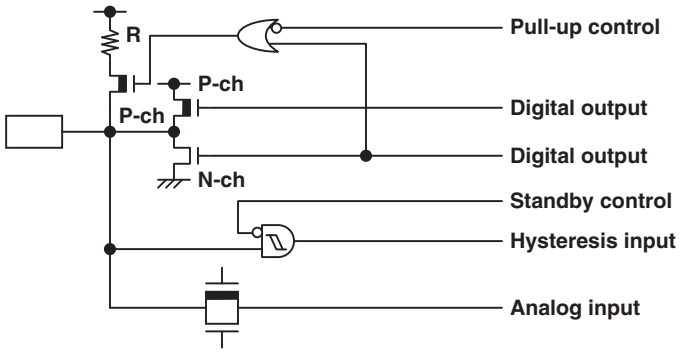
Type	Circuit	Remarks
I		■ N-ch open drain output ■ Hysteresis input ■ CMOS input
J		■ CMOS output ■ Hysteresis input ■ CMOS input ■ Pull-up control available
K		■ Hysteresis input ■ CMOS output ■ Pull-up control available ■ Analog input

7. Notes On Device Handling

■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "14.1 Absolute Maximum Ratings" of “Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

■ Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

8. Pin Connection

■ Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

9. Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

■ DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

■ $\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{\text{RST}}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The $\overline{\text{RST}}$/PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output of the $\overline{\text{RST}}$/PF2 pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

12. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0000_H	PDR0	Port 0 data register	R/W	00000000_B
0001_H	DDR0	Port 0 direction register	R/W	00000000_B
0002_H	PDR1	Port 1 data register	R/W	00000000_B
0003_H	DDR1	Port 1 direction register	R/W	00000000_B
0004_H	—	(Disabled)	—	—
0005_H	WATR	Oscillation stabilization wait time setting register	R/W	11111111_B
0006_H	—	(Disabled)	—	—
0007_H	SYCC	System clock control register	R/W	$0000X011_B$
0008_H	STBC	Standby control register	R/W	$00000XXX_B$
0009_H	RSRR	Reset source register	R/W	$XXXXXXXX_B$
$000A_H$	TBTC	Time-base timer control register	R/W	00000000_B
$000B_H$	WPCR	Watch prescaler control register	R/W	00000000_B
$000C_H$	WDTC	Watchdog timer control register	R/W	$00XX0000_B$
$000D_H$	SYCC2	System clock control register 2	R/W	$XX100011_B$
$000E_H$ to 0011_H	—	(Disabled)	—	—
0012_H	PDR4	Port 4 data register	R/W	00000000_B
0013_H	PDR4	Port 4 direction register	R/W	00000000_B
0014_H, 0015_H	—	(Disabled)	—	—
0016_H	PDR6	Port 6 data register	R/W	00000000_B
0017_H	DDR6	Port 6 direction register	R/W	00000000_B
0018_H	DDR7	Port 7 data register	R/W	00000000_B
0019_H	DDR7	Port 7 direction register	R/W	00000000_B
$001A_H$ to 0027_H	—	(Disabled)	—	—
0028_H	PDRF	Port F data register	R/W	00000000_B
0029_H	DDRF	Port F direction register	R/W	00000000_B
$002A_H$	PDRG	Port G data register	R/W	00000000_B
$002B_H$	DDRG	Port G direction register	R/W	00000000_B
$002C_H$	PUL0	Port 0 pull-up register	R/W	00000000_B
$002D_H$	PUL1	Port 1 pull-up register	R/W	00000000_B
$002E_H$, $002F_H$	—	(Disabled)	—	—
0030_H	PUL4	Port 4 pull-up register	R/W	00000000_B
0031_H	PUL6	Port 6 pull-up register	R/W	00000000_B
0032_H	PUL7	Port 7 pull-up register	R/W	00000000_B
0033_H, 0034_H	—	(Disabled)	—	—
0035_H	PULG	Port G pull-up register	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0036_H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000_B
0037_H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000_B
0038_H	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000_B
0039_H	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000_B
$003A_H$	PC01	8/16-bit PPG timer 01 control register	R/W	00000000_B
$003B_H$	PC00	8/16-bit PPG timer 00 control register	R/W	00000000_B
$003C_H$	PC11	8/16-bit PPG timer 11 control register	R/W	00000000_B
$003D_H$	PC10	8/16-bit PPG timer 10 control register	R/W	00000000_B
$003E_H$	PC21	8/16-bit PPG timer 21 control register	R/W	00000000_B
$003F_H$	PC20	8/16-bit PPG timer 20 control register	R/W	00000000_B
0040_H	TMCSRH1	16-bit reload timer control status register upper	R/W	00000000_B
0041_H	TMCSRL1	16-bit reload timer control status register lower	R/W	00000000_B
0042_H, 0043_H	—	(Disabled)	—	—
0044_H	PCNTH1	16-bit PPG status control register upper	R/W	00000000_B
0045_H	PCNTL1	16-bit PPG status control register lower	R/W	00000000_B
0046_H, 0047_H	—	(Disabled)	—	—
0048_H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000_B
0049_H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000_B
$004A_H$	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000_B
$004B_H$	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000_B
$004C_H$ to $004F_H$	—	(Disabled)	—	—
0050_H	SCR	LIN-UART serial control register	R/W	00000000_B
0051_H	SMR	LIN-UART serial mode register	R/W	00000000_B
0052_H	SSR	LIN-UART serial status register	R/W	00001000_B
0053_H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000_B
0054_H	ESCR	LIN-UART extended status control register	R/W	00000100_B
0055_H	ECCR	LIN-UART extended communication control register	R/W	$000000XX_B$
0056_H	SMC10	UART/SIO serial mode control register 1	R/W	00000000_B
0057_H	SMC20	UART/SIO serial mode control register 2	R/W	00100000_B
0058_H	SSR0	UART/SIO serial status and data register	R/W	00000001_B
0059_H	TDR0	UART/SIO serial output data register	R/W	00000000_B
$005A_H$	RDR0	UART/SIO serial input data register	R	00000000_B
$005B_H$ to $005F_H$	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0060_H	IBCR00	I^2C bus control register 0	R/W	00000000_B
0061_H	IBCR10	I^2C bus control register 1	R/W	00000000_B
0062_H	IBCR0	I^2C bus status register	R/W	00000000_B
0063_H	IDDR0	I^2C data register	R/W	00000000_B
0064_H	IAAR0	I^2C address register	R/W	00000000_B
0065_H	ICCR0	I^2C clock control register	R/W	00000000_B
0066_H	OPCUR	Output control register (upper)	R/W	00000000_B
0067_H	OPCLR	Output control register (lower)	R/W	00000000_B
0068_H	IPCUR	Input control register (upper)	R/W	00000000_B
0069_H	IPCLR	Input control register (lower)	R/W	00000000_B
$006A_H$	NCCR	Noise cancellation control register	R/W	00000000_B
$006B_H$	TCSR	Timer control status register	R/W	00000000_B
$006C_H$	ADC1	8/10-bit A/D converter control register 1	R/W	00000000_B
$006D_H$	ADC2	8/10-bit A/D converter control register 2	R/W	00000000_B
$006E_H$	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000_B
$006F_H$	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000_B
0070_H	—	(Disabled)	—	—
0071_H	FSR2	Flash memory status register 2	R/W	00000000_B
0072_H	FSR	Flash memory status register	R/W	$000X0000_B$
0073_H	SWRE0	Flash memory sector write control register 0	R/W	00000000_B
0074_H	FSR3	Flash memory status register 3	R	00000000_B
0075_H	—	(Disabled)	—	—
0076_H	WREN	Wild register address compare enable register	R/W	00000000_B
0077_H	WROR	Wild register data test setting register	R/W	00000000_B
0078_H	—	Mirror of register bank pointer (RP) and mirror of direct bank pointer (DP)	—	—
0079_H	ILR0	Interrupt level setting register 0	R/W	11111111_B
$007A_H$	ILR1	Interrupt level setting register 1	R/W	11111111_B
$007B_H$	ILR2	Interrupt level setting register 2	R/W	11111111_B
$007C_H$	ILR3	Interrupt level setting register 3	R/W	11111111_B
$007D_H$	ILR4	Interrupt level setting register 4	R/W	11111111_B
$007E_H$	ILR5	Interrupt level setting register 5	R/W	11111111_B
$007F_H$	—	(Disabled)	—	—
$0F80_H$	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000_B
$0F81_H$	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000_B
$0F82_H$	WRDR0	Wild register data setting register ch. 0	R/W	00000000_B

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
$0F83_H$	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000_B
$0F84_H$	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000_B
$0F85_H$	WRDR1	Wild register data setting register ch. 1	R/W	00000000_B
$0F86_H$	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000_B
$0F87_H$	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000_B
$0F88_H$	WRDR2	Wild register data setting register ch. 2	R/W	00000000_B
$0F89_H$ to $0F91_H$	—	(Disabled)	—	—
$0F92_H$	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000_B
$0F93_H$	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000_B
$0F94_H$	T01DR	8/16-bit composite timer 01 data register	R/W	00000000_B
$0F95_H$	T00DR	8/16-bit composite timer 00 data register	R/W	00000000_B
$0F96_H$	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000_B
$0F97_H$	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	00000000_B
$0F98_H$	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	00000000_B
$0F99_H$	T11DR	8/16-bit composite timer 11 data register	R/W	00000000_B
$0F9A_H$	T10DR	8/16-bit composite timer 10 data register	R/W	00000000_B
$0F9B_H$	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	00000000_B
$0F9C_H$	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	11111111_B
$0F9D_H$	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	11111111_B
$0F9E_H$	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	11111111_B
$0F9F_H$	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	11111111_B
$0FA0_H$	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	11111111_B
$0FA1_H$	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	11111111_B
$0FA2_H$	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	11111111_B
$0FA3_H$	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	11111111_B
$0FA4_H$	PPGS	8/16-bit PPG startup register	R/W	00000000_B
$0FA5_H$	REVC	8/16-bit PPG output reverse register	R/W	00000000_B
$0FA6_H$	PPS21	8/16-bit PPG21 cycle setting buffer register	R/W	11111111_B
$0FA7_H$	PPS20	8/16-bit PPG20 cycle setting buffer register	R/W	11111111_B
$0FA8_H$	TMRH1	16-bit reload timer timer register (upper)	R/W	00000000_B
	TMRLRH1	16-bit reload timer reload register (upper)		
$0FA9_H$	TMRL1	16-bit reload timer timer register (lower)	R/W	00000000_B
	TMRLRL1	16-bit reload timer reload register (lower)		
$0FAA_H$	PDS21	8/16-bit PPG21 duty setting buffer register	R/W	11111111_B
$0FAB_H$	PDS20	8/16-bit PPG20 duty setting buffer register	R/W	11111111_B

(Continued)

13. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0, ch. 4	IRQ00	$FFFA_H$	$FFFB_H$	L00 [1:0]	High
External interrupt ch. 1, ch. 5	IRQ01	$FFF8_H$	$FFF9_H$	L01 [1:0]	
External interrupt ch. 2, ch. 6	IRQ02	$FFF6_H$	$FFF7_H$	L02 [1:0]	
External interrupt ch. 3, ch. 7	IRQ03	$FFF4_H$	$FFF5_H$	L03 [1:0]	
UART/SIO ch. 0, MPG (DTTI)	IRQ04	$FFF2_H$	$FFF3_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	$FFF0_H$	$FFF1_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	$FFEE_H$	$FFEF_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	$FFEC_H$	$FFED_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	$FFEA_H$	$FFEB_H$	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	$FFE8_H$	$FFE9_H$	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	$FFE6_H$	$FFE7_H$	L10 [1:0]	
8/16-bit PPG ch. 2 (upper)	IRQ11	$FFE4_H$	$FFE5_H$	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	$FFE2_H$	$FFE3_H$	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	$FFE0_H$	$FFE1_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	$FFDE_H$	$FFDF_H$	L14 [1:0]	
8/16-bit PPG ch. 2 (lower)	IRQ15	$FFDC_H$	$FFDD_H$	L15 [1:0]	
16-bit reload timer ch. 1, MPG (write timing/compare clear), I^2C	IRQ16	$FFDA_H$	$FFDB_H$	L16 [1:0]	
16-bit PPG timer ch. 1, MPG (position detection/compare match)	IRQ17	$FFD8_H$	$FFD9_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	$FFD6_H$	$FFD7_H$	L18 [1:0]	
Time-base timer	IRQ19	$FFD4_H$	$FFD5_H$	L19 [1:0]	
Watch prescaler	IRQ20	$FFD2_H$	$FFD3_H$	L20 [1:0]	
—	IRQ21	$FFD0_H$	$FFD1_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	$FFCE_H$	$FFCF_H$	L22 [1:0]	
Flash memory	IRQ23	$FFCC_H$	$FFCD_H$	L23 [1:0]	Low

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	−2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
"L" level maximum output current	I_{OL1}	—	15	mA	Other than P62 to P67
	I_{OL2}	—	15		P62 to P67
"L" level average current	I_{OLAV1}	—	4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}	—	12		P62 to P67 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	I_{OH1}	—	−15	mA	Other than P12, P62 to P67, P72, P73 and PF2
	I_{OH2}	—	−15		P12, P62 to P67, P72, P73 and PF2
"H" level average current	I_{OHAV1}	—	−4	mA	Other than P12, P62 to P67, P72, P73 and PF2 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}	—	−8		P12, P62 to P67, P72, P73 and PF2 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	ΣI_{OH}	—	−100	mA	
"H" level total average output current	ΣI_{OHAV}	—	−50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	−40	+85	°C	
Storage temperature	Tstg	−55	+150	°C	

(Continued)

14.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*3	Max		
"H" level input voltage	V_{IHI}	P47, P72, P73, P77	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	When CMOS input level (hysteresis input) is selected
	V_{IHS}	P00 to P07, P10 to P17, P40 to P47, P60 to P67, P70 to P77, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P47, P72, P73, P77	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	When CMOS input level (hysteresis input) is selected
	V_{ILS}	P00 to P07, P10 to P17, P40 to P47, P60 to P67, P70 to P77, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P72, P73, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P62 to P67, P72, P73, PF2	I_{OH} = −4 mA	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P62 to P67	I_{OH} = −8 mA	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P62 to P67	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P62 to P67	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	−5	—	+5	µA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00 to P07, P10, P11, P13 to P17, P40 to P47, P60, P61, P70, P71, P74 to P76, PG1, PG2	V_I = 0 V	25	50	100	kΩ	When pull-up resistance is enabled

(Continued)

14.4 AC Characteristics

14.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*1	1	—	32.5	MHz	
	F_{CRH}	—	—	12.25	12.5	12.75	MHz	When the main CR clock is used*2
				9.80	10	10.20	MHz	
				7.84	8	8.16	MHz	
				0.98	1	1.02	MHz	
				12.18	12.5	12.82	MHz	When the main CR clock is used*3
				9.75	10	10.25	MHz	
				7.80	8	8.20	MHz	
				0.97	1	1.03	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	200	kHz	When the sub-CR clock is used
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When the external clock is used
		X0, X1	*1	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1} t_{WL1}	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*1	12.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rise time and fall time	t_{CR} t_{CF}	X0	X1: open	—	—	5	ns	When the external clock is used
		X0, X1	*1	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	80	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	10	µs	When the sub-CR clock is used

*1: The external clock signal is input to X0 and the inverted external clock signal to X1.

*2: These specifications are only applicable to a product in LQFP package (FPT-48P-M49 or FPT-52P-M02).

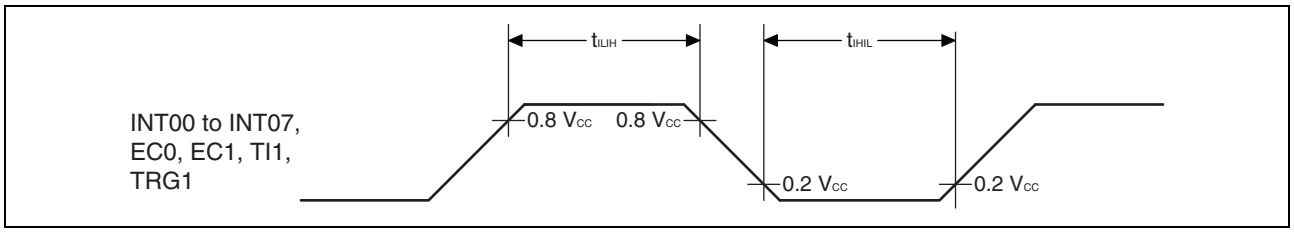
*3: These specifications are only applicable to a product in QFN package (LCC-48P-M11).

14.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1,TI1, TRG1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



14.4.6 LIN-UART Timing

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 − t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 95	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 95	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 95	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.

Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

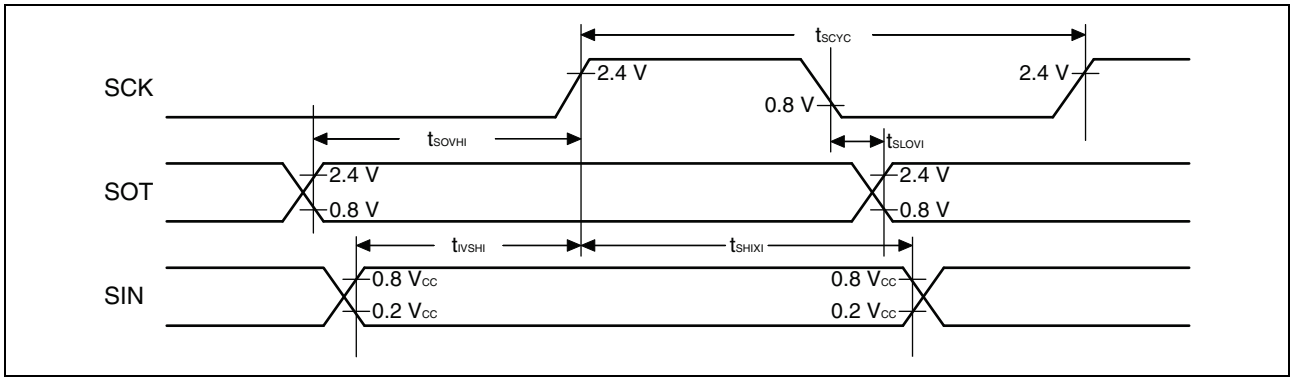
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−95	+95	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 190	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		—	4 t_{MCLK}*3	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.



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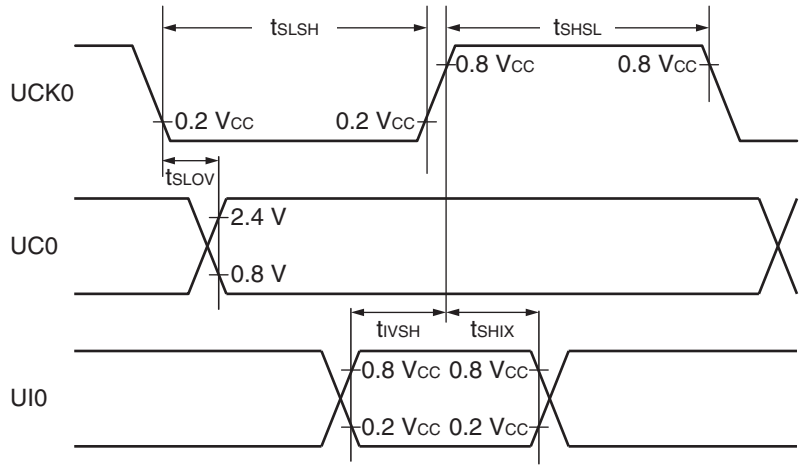
(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Sym-bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	4 t_{MCLK} − 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		4 t_{MCLK} − 20	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
STOP condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} − 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} − 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} − 3 t_{MCLK} − 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} − 20	—	ns	At reception
SDA↓ → SCL↑ (at wakeup function)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t_{MCLK} − 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

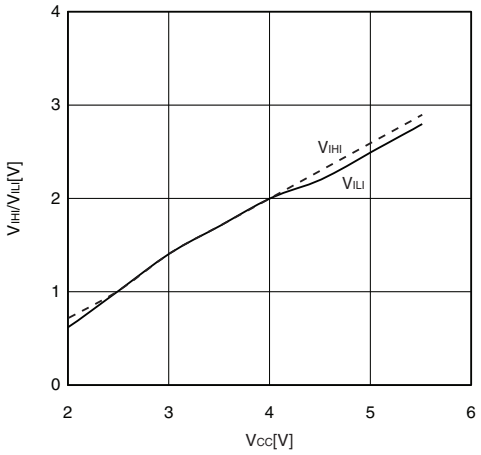
*2:
- See “Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I^2C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I^2C clock control register (ICCR0).
- The actual timing of I^2C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < $t_{MCLK} \leq$ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < $t_{MCLK} \leq$ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 98) : 0.9 MHz < $t_{MCLK} \leq$ 10 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 10 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < $t_{MCLK} \leq$ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < $t_{MCLK} \leq$ 8 MHz
  (m, n) = (6, 4) : 3.3 MHz < $t_{MCLK} \leq$ 10 MHz

- External shift clock mode

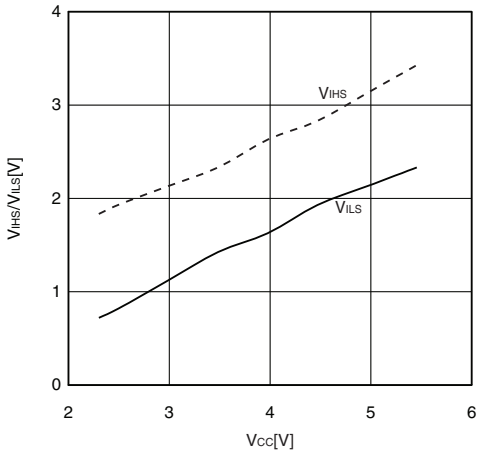


■ Input voltage characteristics

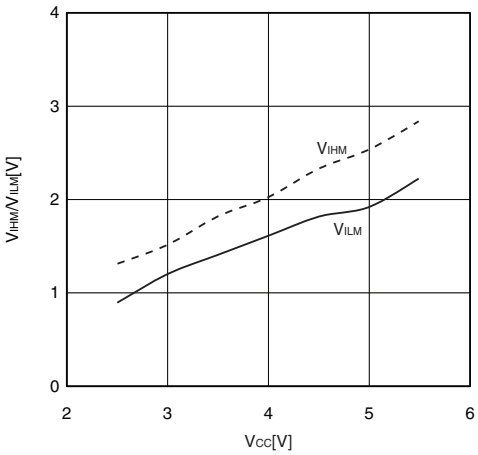
$V_{IHI} - V_{CC}$ and $V_{ILI} - V_{CC}$
$T_A = +25°C$



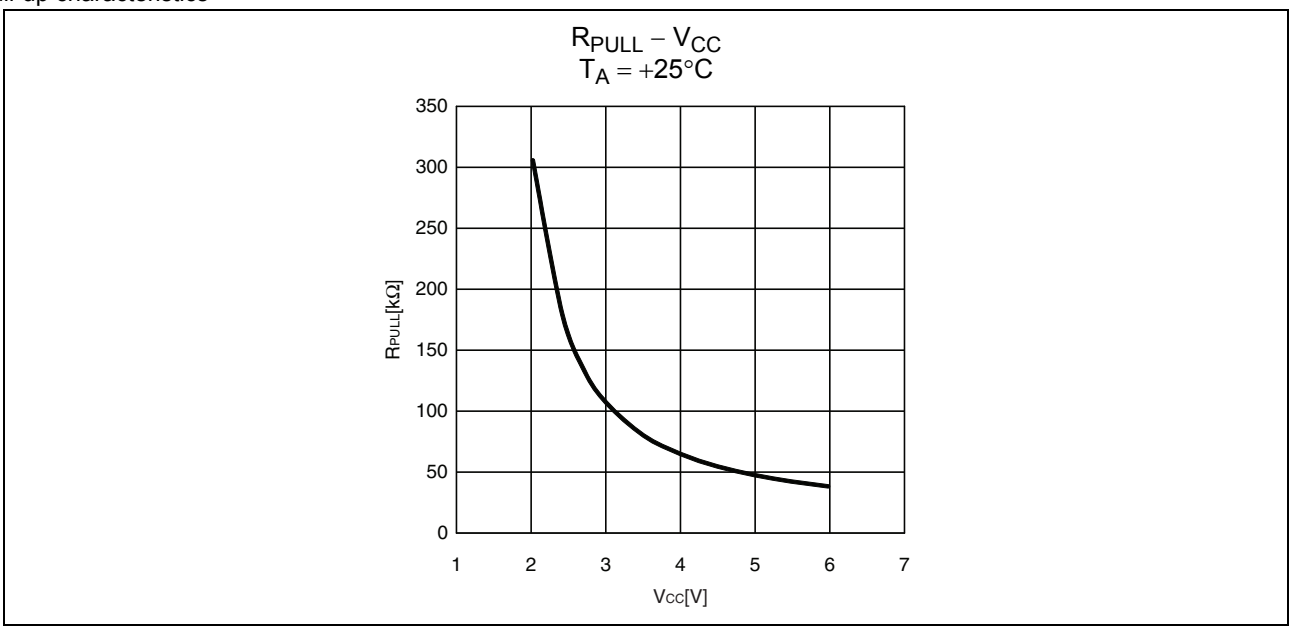
$V_{IHS} - V_{CC}$ and $V_{ILS} - V_{CC}$
$T_A = +25°C$



$V_{IHM} - V_{CC}$ and $V_{ILM} - V_{CC}$
$T_A = +25°C$



■ Pull-up characteristics



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