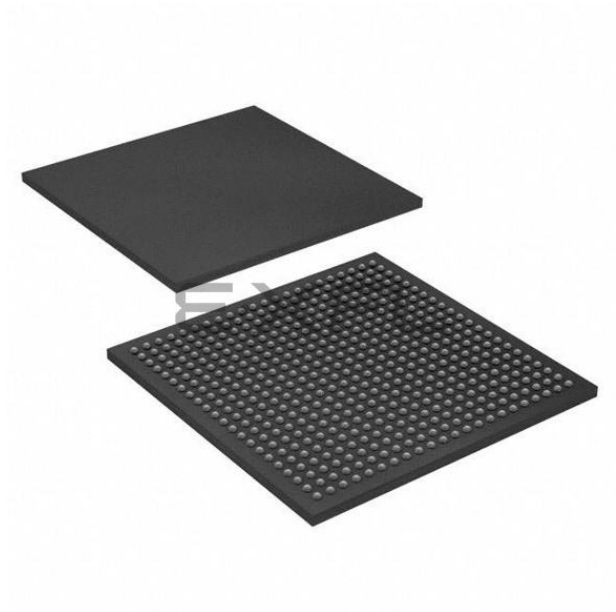

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba5u19c7n

Cyclone V Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Cyclone® V devices.

Cyclone V devices are offered in commercial and industrial grades. Commercial devices are offered in –C6 (fastest), –C7, and –C8 speed grades. Industrial grade devices are offered in the –I7 speed grade. Automotive devices are offered in the –A7 speed grade.

Cyclone V SoC devices are also offered in a low-power variant, as indicated by the L power option in the device part number. These devices have 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE. Note that the L power option devices are only available in –I7 speed grade, and have the equivalent operating conditions and timing specifications as the standard –I7 speed grade devices.

Table 1. Low Power Variants

Density	Ordering Part Number (OPN)	Static Power Reduction
25K LE	5CSEBA2U19I7LN	30%
	5CSEBA2U23I7LN	
	5CSXFC2C6U23I7LN	
40K LE	5CSEBA4U19I7LN	
	5CSEBA4U23I7LN	
	5CSXFC4C6U23I7LN	
85K LE	5CSEBA5U19I7LN	20%
	5CSEBA5U23I7LN	
	5CSXC5C6U23I7LN	

continued...

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 3. Maximum Allowed Overshoot During Transitions for Cyclone V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%

continued...

Symbol	Description	Condition	Minimum(11)	Typical	Maximum(11)	Unit
		1.8 V	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
$V_{CC\_AUX\_SHARED}$(14)	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

Recommended Operating Conditions on page 8
Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based EPE and the Intel® Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Handbook
  Provides more information about power estimation tools.

(11) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(14) $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.

Table 9. OCT Calibration Accuracy Specifications for Cyclone V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–C6	–I7, –C7	–C8, –A7	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 17. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Cyclone V Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[19] (mA)	I_{OH}[19] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4

continued...

(19) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[19] (mA)	I_{OH}[19] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO}+ 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

(19) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Symbol	V_{OD} Setting[48]	V_{OD} Value (mV)	V_{OD} Setting[48]	V_{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Cyclone V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

(48) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		–C8, –A7 speed grades	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	–C6, –C7, –I7 speed grades	—	—	550(54)	MHz
		–C8, –A7 speed grades	—	—	460(54)	MHz
f_{OUT_EXT}	Output frequency for external clock output	–C6, –C7, –I7 speed grades	—	—	667(54)	MHz
		–C8, –A7 speed grades	—	—	533(54)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$t_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High(55)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps

continued...

(53) The VCO frequency reported by the Intel Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(54) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

(55) High bandwidth PLL settings are not supported in external feedback mode.

DSP Block Performance Specifications

Table 32. DSP Block Performance Specifications for Cyclone V Devices

Mode		Performance			Unit
		–C6	–C7, –I7	–C8, –A7	
Modes using One DSP Block	Independent 9 × 9 multiplication	340	300	260	MHz
	Independent 18 × 19 multiplication	287	250	200	MHz
	Independent 18 × 18 multiplication	287	250	200	MHz
	Independent 27 × 27 multiplication	250	200	160	MHz
	Independent 18 × 25 multiplication	310	250	200	MHz
	Independent 20 × 24 multiplication	310	250	200	MHz
	Two 18 × 19 multiplier adder mode	310	250	200	MHz
	18 × 18 multiplier added summed with 36-bit input	310	250	200	MHz
Modes using Two DSP Blocks	Complex 18 × 19 multiplication	310	250	200	MHz

Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 33. Memory Block Performance Specifications for Cyclone V Devices

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–C6	–C7, –I7	–C8, –A7	
MLAB	Single port, all supported widths	0	1	420	350	300	MHz
	Simple dual-port, all supported widths	0	1	420	350	300	MHz
	Simple dual-port with read and write at the same address	0	1	340	290	240	MHz

continued...

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–C6	–C7, –I7	–C8, –A7	
	ROM, all supported width	0	1	420	350	300	MHz
M10K Block	Single-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port with the **read-during-write** option set to **Old Data**, all supported widths	0	1	275	240	180	MHz
	True dual port, all supported widths	0	1	315	275	240	MHz
	ROM, all supported widths	0	1	315	275	240	MHz

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

DLL Frequency Range Specifications

Table 35. DLL Frequency Range Specifications for Cyclone V Devices

Parameter	–C6	–C7, –I7	–C8	Unit
DLL operating frequency range	167 – 400	167 – 400	167 – 333	MHz

DQS Logic Block Specifications

Table 36. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Cyclone V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–C6	–C7, –I7	–C8	Unit
2	40	80	80	ps

Memory Output Clock Jitter Specifications

Table 37. Memory Output Clock Jitter Specifications for Cyclone V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Intel recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Parameter	Clock Network	Symbol	–C6		–C7, –I7		–C8		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	–60	60	–70	70	–70	70	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	—	90	—	100	—	100	ps

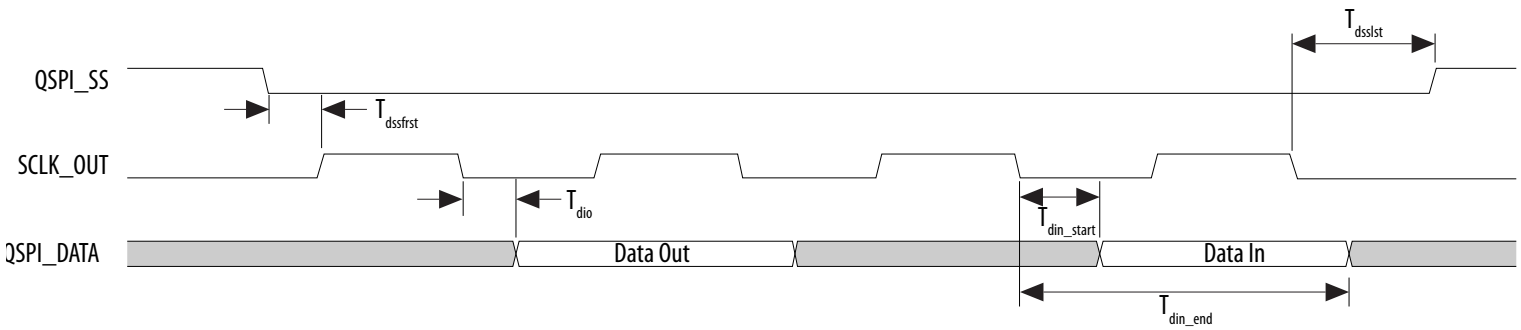
Quad SPI Flash Timing Characteristics

Table 43. Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (68)	ns
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (68)	—	—	ns

Figure 6. Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



(68) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Intel provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the *Quad SPI Flash Controller chapter in the Cyclone V Hard Processor System Technical Reference Manual*.

Figure 7. SPI Master Timing Diagram

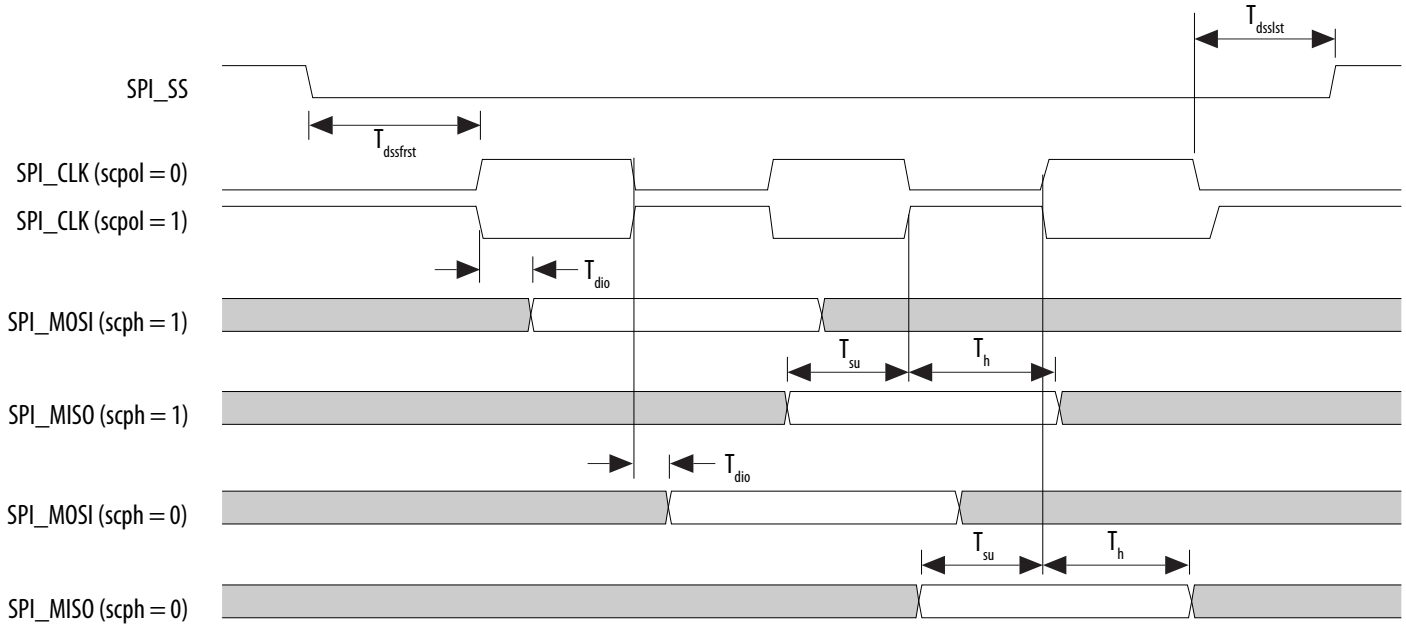
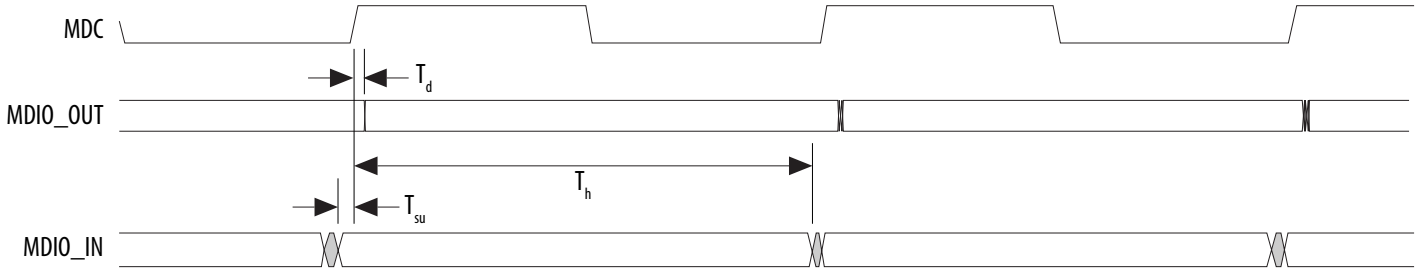


Table 45. SPI Slave Timing Requirements for Cyclone V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	20	—	ns
T_s	MOSI Setup time	5	—	ns
T_h	MOSI Hold time	5	—	ns
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	ns
T_d	MISO output delay	—	6	ns

Figure 13. MDIO Timing Diagram

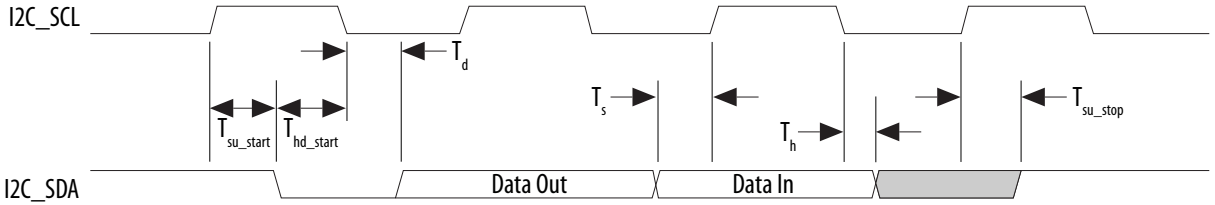


I²C Timing Characteristics

Table 51. I²C Timing Requirements for Cyclone V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

Figure 14. I²C Timing Diagram



NAND Timing Characteristics

Table 52. NAND ONFI 1.0 Timing Requirements for Cyclone V Devices

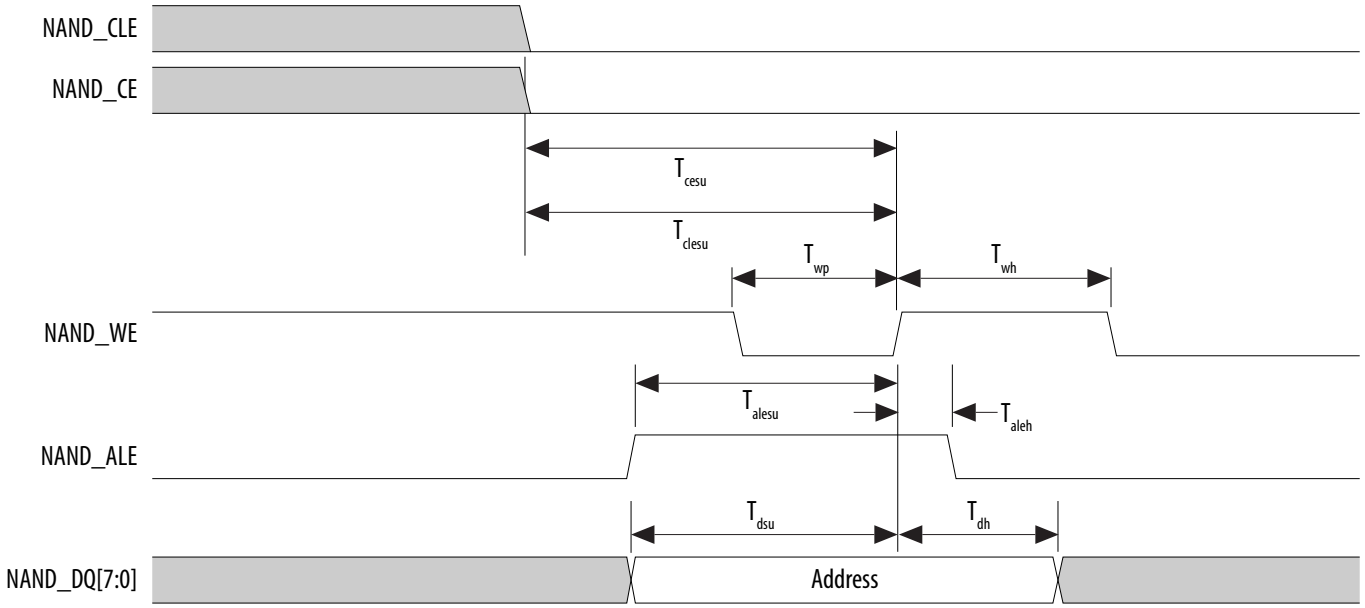
The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T_{wp} (72)	Write enable pulse width	10	—	ns
T_{wh} (72)	Write enable hold time	7	—	ns
T_{rp} (72)	Read enable pulse width	10	—	ns
T_{reh} (72)	Read enable hold time	7	—	ns
T_{clesu} (72)	Command latch enable to write enable setup time	10	—	ns
T_{cleh} (72)	Command latch enable to write enable hold time	5	—	ns
T_{cesu} (72)	Chip enable to write enable setup time	15	—	ns
T_{ceh} (72)	Chip enable to write enable hold time	5	—	ns
T_{alesu} (72)	Address latch enable to write enable setup time	10	—	ns
T_{aleh} (72)	Address latch enable to write enable hold time	5	—	ns
T_{dsu} (72)	Data to write enable setup time	10	—	ns
T_{dh} (72)	Data to write enable hold time	5	—	ns

continued...

(72) Timing of the NAND interface is controlled through the NAND configuration registers.

Figure 16. NAND Address Latch Timing Diagram



Related Information

Configuration Files on page 76

Remote System Upgrades

Table 66. Remote System Upgrade Circuitry Timing Specifications for Cyclone V Devices

Parameter	Minimum	Unit
$t_{RU\_nCONFIG}$ (98)	250	ns
$t_{RU\_nRSTIMER}$ (99)	250	ns

Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about `reset_timer` (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 67. User Watchdog Internal Oscillator Frequency Specifications for Cyclone V Devices

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

Intel offers two ways to determine I/O timing—the Excel-based I/O timing and the Intel Quartus Prime Timing Analyzer.

(98) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(99) This is equivalent to strobing the reset timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

Date	Version	Changes
July 2014	3.9	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20. • Updated h2f_user2_clk specification for –C6, –C7, and –I7 speed grades in Table 34. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 35. • Updated T_d and T_h specifications in Table 41. • Added T_h specification in Table 43 and Figure 10. • Updated a note in Figure 17, Figure 18, and Figure 20 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 54. • Added DCLK device initialization clock source specification in Table 56. • Added description in "Configuration Files" section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature. • Added "Recommended EPCQ Serial Configuration Device" values in Table 57. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 59.
February 2014	3.8	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.7	• Updated Table 1, Table 3, Table 19, Table 20, Table 23, Table 25, Table 27, Table 34, Table 44, Table 51, Table 52, Table 55, and Table 61. • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 24, Table 25, Table 26, Table 27, Table 28, Table 32, Table 33, Table 49, Table 50, Table 51, Table 52, Table 53, Table 54, Table 55, Table 57, Table 58, Table 59, Table 60, and Table 62.
November 2013	3.6	Updated Table 23, Table 30, and Table 31.
October 2013	3.5	• Added "HPS PLL Specifications". • Added Table 23, Table 35, and Table 36. • Updated Table 1, Table 5, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, Table 28, Table 34, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, and Table 53. • Updated Figure 1, Figure 2, Figure 4, Figure 10, Figure 12, Figure 13, and Figure 16. • Removed table: GPIO Pulse Width for Cyclone V Devices.

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Date	Version	Changes
June 2013	3.4	• Updated Table 20, Table 27, and Table 34. • Updated "UART Interface" and "CAN Interface" sections. • Removed the following tables: — Table 45: UART Baud Rate for Cyclone V Devices — Table 47: CAN Pulse Width for Cyclone V Devices
May 2013	3.3	• Added Table 33. • Updated Figure 5, Figure 6, Figure 17, Figure 19, and Figure 20. • Updated Table 1, Table 4, Table 5, Table 10, Table 13, Table 19, Table 20, Table 26, Table 32, Table 35, Table 36, Table 43, Table 53, Table 54, Table 57, and Table 61.
March 2013	3.2	• Added HPS reset information in the "HPS Specifications" section. • Added Table 57. • Updated Table 1, Table 2, Table 17, Table 20, Table 52, and Table 56. • Updated Figure 18.
January 2013	3.1	Updated Table 4, Table 20, and Table 56.
November 2012	3.0	• Updated Table 1, Table 4, Table 5, Table 9, Table 14, Table 16, Table 17, Table 19, Table 20, Table 25, Table 28, Table 52, Table 55, Table 56, and Table 59. • Removed table: Transceiver Block Jitter Specifications for Cyclone V GX Devices. • Added HPS information: — Added "HPS Specifications" section. — Added Table 33, Table 34, Table 35, Table 36, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, and Table 46. — Added Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, and Figure 16. — Updated Table 3.
June 2012	2.0	Updated for the Quartus Prime software v12.0 release: • Restructured document. • Removed "Power Consumption" section. • Updated Table 1,Table 3, Table 19, Table 20, Table 25, Table 27, Table 28, Table 30, Table 31, Table 34, Table 36, Table 37, Table 38, Table 39, Table 41, Table 43, and Table 46. • Added Table 22, Table 23, and Table 29. • Added Figure 1 and Figure 2. • Added "Initialization" and "Configuration Files" sections.

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Date	Version	Changes
February 2012	1.2	• Added automotive speed grade information. • Added Figure 2–1. • Updated Table 2–3, Table 2–8, Table 2–9, Table 2–19, Table 2–20, Table 2–21, Table 2–22, Table 2–23, Table 2–24, Table 2–25, Table 2–26, Table 2–27, Table 2–28, Table 2–30, Table 2–35, and Table 2–43. • Minor text edits.
November 2011	1.1	• Added Table 2–5. • Updated Table 2–3, Table 2–4, Table 2–11, Table 2–13, Table 2–20, and Table 2–21.
October 2011	1.0	Initial release.