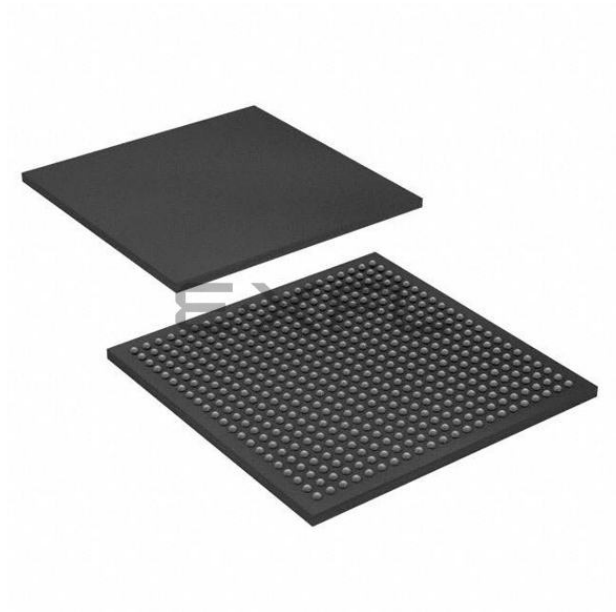

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Single ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba5u19c7sn

Recommended Operating Conditions

Table 4. Recommended Operating Conditions for Cyclone V Devices

This table lists the steady-state voltage values expected from Cyclone V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum(2)	Typical	Maximum(2)	Unit
V_{CC}	Core voltage, periphery circuitry power supply, transceiver physical coding sublayer (PCS) power supply, and transceiver PCI Express* (PCIe*) hard IP digital power supply	Devices without internal scrubbing feature	1.07	1.1	1.13	V
		Devices with internal scrubbing feature (with SC suffix) (3)	1.12	1.15	1.18	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCPD}(4)	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V

continued...

(2) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(3) The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

(4) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	TX V_{CM} = 0.65 V and slew rate of 15 ps	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode	—	—	180	—	—	180	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew	×*N* PMA bonded mode	—	—	500	—	—	500	—	—	500	ps

Table 25. CMU PLL Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported data range	—	614	—	5000/6144[35]	614	—	3125	614	—	2500	Mbps
fPLL supported data range	—	614	—	3125	614	—	3125	614	—	2500	Mbps

Table 26. Transceiver-FPGA Fabric Interface Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Interface speed (single-width mode)	—	25	—	187.5	25	—	187.5	25	—	163.84	MHz
Interface speed (double-width mode)	—	25	—	163.84	25	—	163.84	25	—	156.25	MHz

Related Information

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 32
- CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain on page 33
- PCIe Supported Configurations and Placement Guidelines
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.

Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting	Intel Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Intel Devices
Provides the Cyclone V HSSI HSPICE models.

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–C6	–C7, –I7	–C8, –A7	
	ROM, all supported width	0	1	420	350	300	MHz
M10K Block	Single-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port with the **read-during-write** option set to **Old Data**, all supported widths	0	1	275	240	180	MHz
	True dual port, all supported widths	0	1	315	275	240	MHz
	ROM, all supported widths	0	1	315	275	240	MHz

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		Emulated Differential I/O Standards										
	t_{RISE} and t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
	TCCS	True Differential I/O Standards	—	—	200	—	—	250	—	—	250	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	300	—	—	300	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
Receiver	f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	875(67)	(65)	—	840(67)	(65)	—	640(67)	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
Sampling Window		—	—	—	350	—	—	350	—	—	350	ps

OCT Calibration Block Specifications

Table 38. OCT Calibration Block Specifications for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT/R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for oe and dyn_term_ctrl Signals

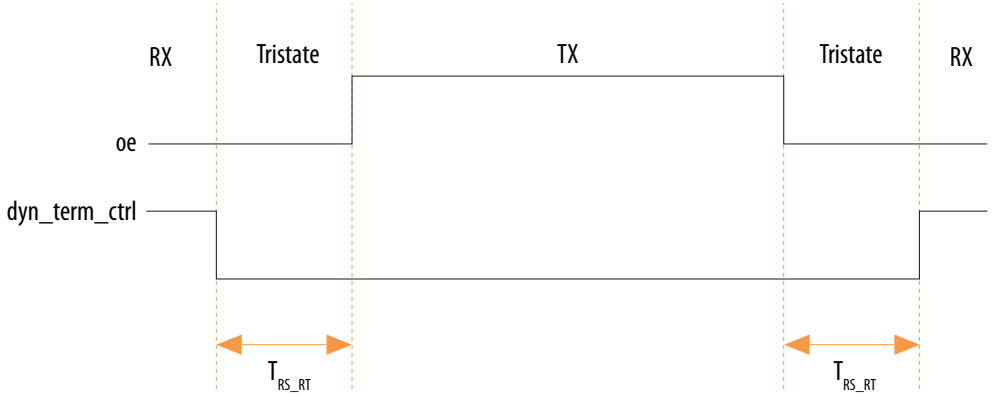
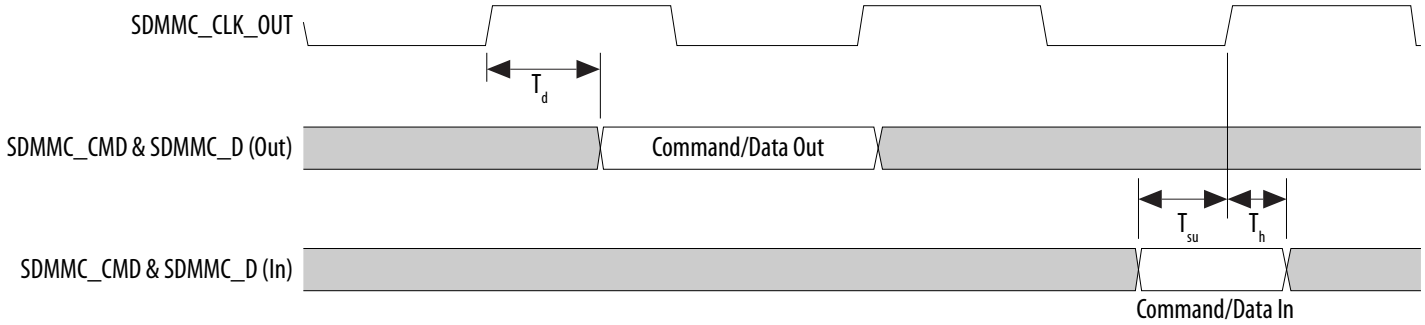


Figure 9. SD/MMC Timing Diagram



Related Information

Booting and Configuration Chapter, Cyclone V Hard Processor System Technical Reference Manual
Provides more information about CSEL pin settings in the *SD/MMC Controller CSEL Pin Settings* table.

USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 47. USB Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	—	11	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Symbol	Description	Min	Max	Unit
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Figure 15. NAND Command Latch Timing Diagram

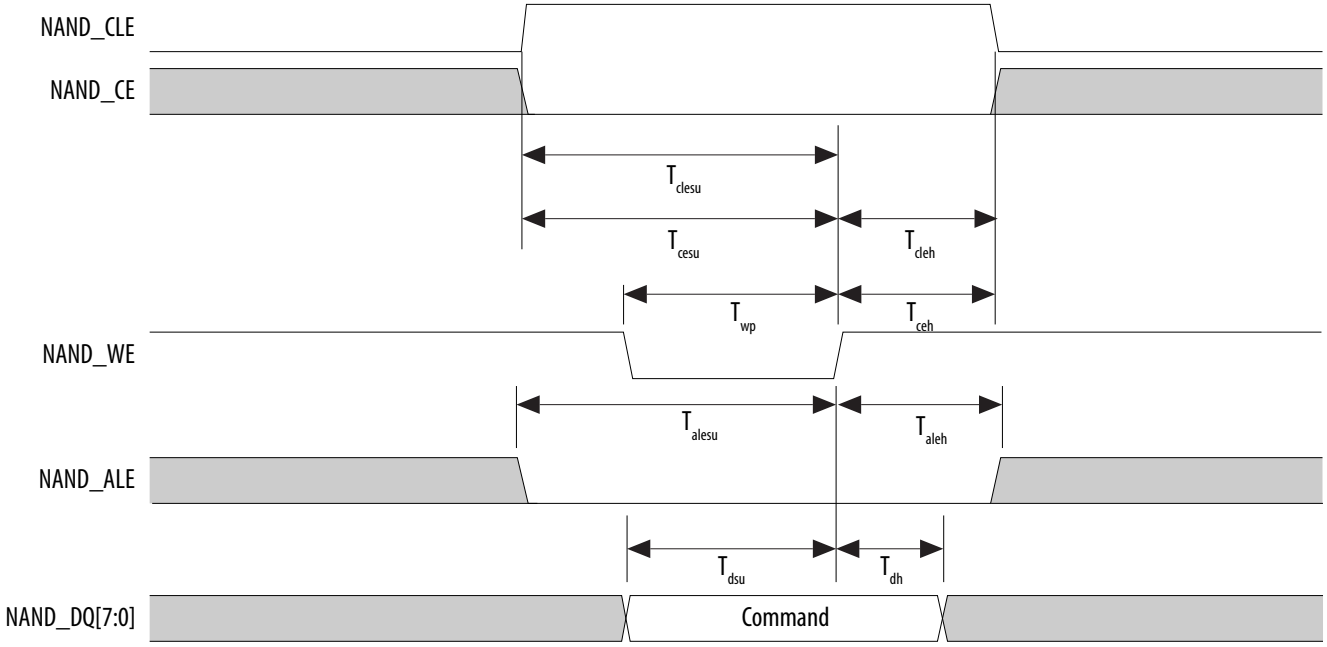
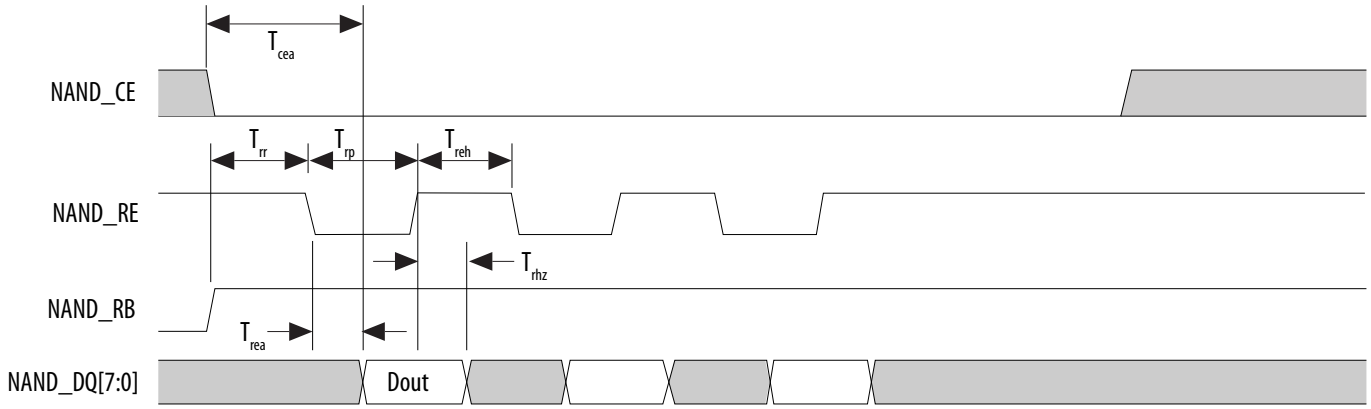


Figure 18. NAND Data Read Timing Diagram



Arm Trace Timing Characteristics

Table 53. Arm Trace Timing Requirements for Cyclone V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK}[83]	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}[83]	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$[84]	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode[85]	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times$ CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(82) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

(83) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(84) *N* is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

(85) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

DCLK Frequency Specification in the AS Configuration Scheme

Table 61. DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

Passive Serial (PS) Configuration Timing

Table 62. PS Timing Parameters for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(89)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(90)	µs
t_{CF2CK}(91)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(91)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns

continued...

(89) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(90) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

(91) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Configuration Files

Table 64. Uncompressed .rbf Sizes for Cyclone V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (`.rbf`) size is specifically for the Configuration via Protocol (CvP) feature.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device(94)
Cyclone V E (95)	A2	21,061,280	275,608	EPCQ64
	A4	21,061,280	275,608	EPCQ64
	A5	33,958,560	322,072	EPCQ128
	A7	56,167,552	435,288	EPCQ128
	A9	102,871,776	400,408	EPCQ256
Cyclone V GX	C3	14,510,912	320,280	EPCQ32
	C4	33,958,560	322,072	EPCQ128
	C5	33,958,560	322,072	EPCQ128
	C7	56,167,552	435,288	EPCQ128
	C9	102,871,776	400,408	EPCQ256
Cyclone V GT	D5	33,958,560	322,072	EPCQ128
	D7	56,167,552	435,288	EPCQ128
	D9	102,871,776	400,408	EPCQ256
Cyclone V SE (95)	A2	33,958,560	322,072	EPCQ128

continued...

(94) The recommended EPCQ serial configuration devices are able to store more than one image.

(95) No PCIe hard IP, configuration via protocol (CvP) is not supported in this family.

Variant	Member Code	Active Serial[96]			Fast Passive Parallel[97]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A9	4	100	257	16	125	51
Cyclone V GX	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Programmable Output Buffer Delay

Table 69. Programmable Output Buffer Delay for Cyclone V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Intel Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

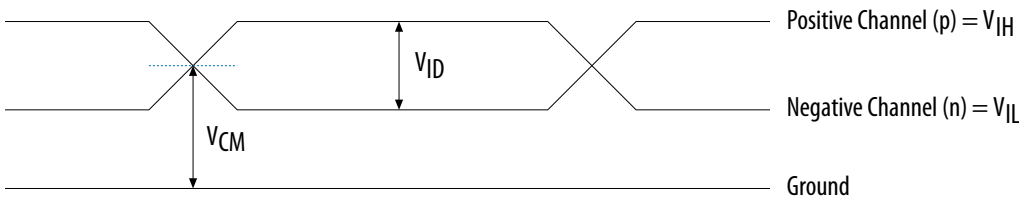
Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

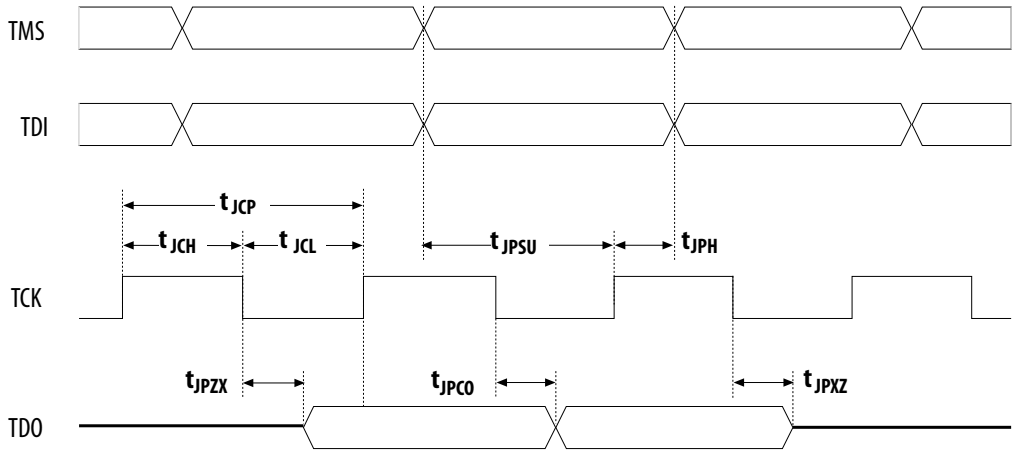
Table 70. Glossary

Term	Definition
Differential I/O standards	Receiver Input Waveforms

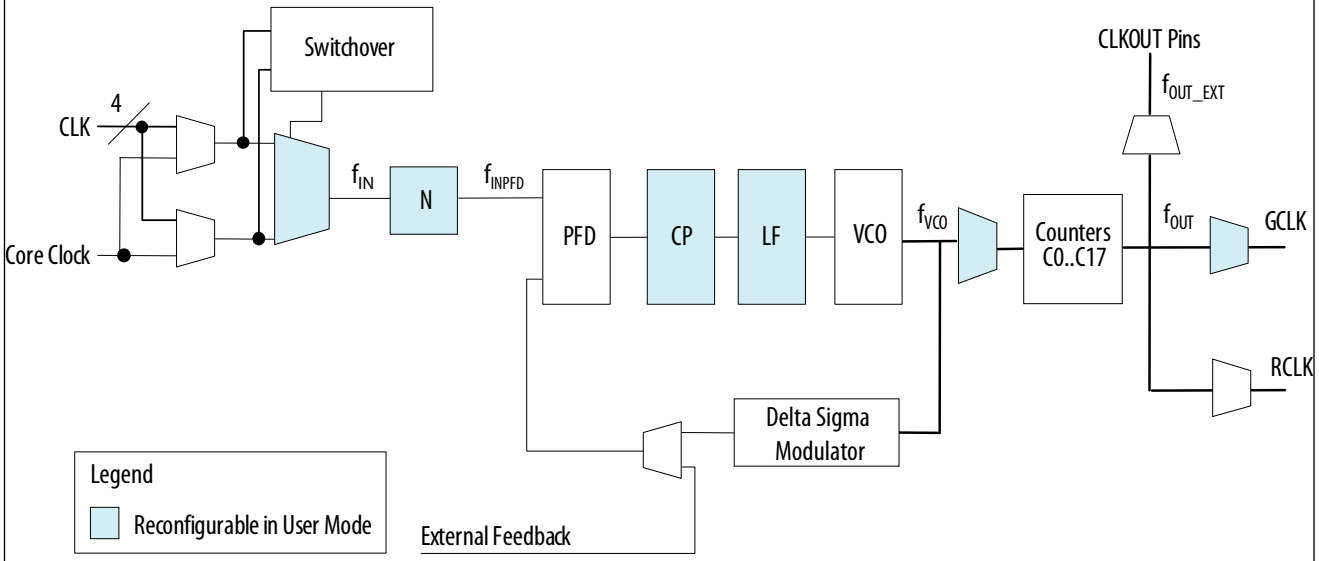
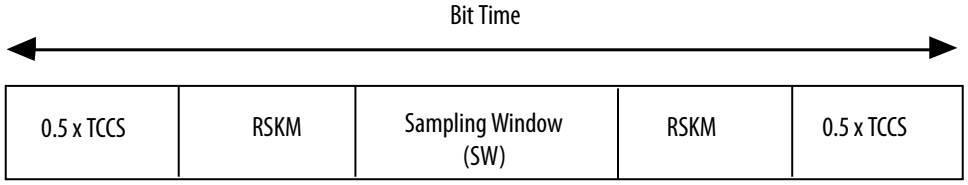
continued...

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms

continued...

Term	Definition
	
PLL specifications	Diagram of PLL specifications

continued...

Term	Definition
	 Note: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.
R_L	Receiver differential input discrete resistor (external to the Cyclone V device).
Sampling window (SW)	Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 

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Document Revision History for Cyclone V Device Datasheet

Document Version	Changes
2018.05.07	• Added description about the low-power option ("L" suffix) for Cyclone V SE and SX devices. • Added the *Cyclone V Devices Overshoot Duration* diagram. • Removed the description on SD/MMC interface calibration support in the *Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices* table. This feature is currently supported in the preloader. • Removed the note to Cyclone V SE A2 and A4 devices, and Cyclone V SX C2 and C4 devices in the *Uncompressed .rbf Sizes for Cyclone V Devices* table. These devices are currently supported in the Intel Quartus Prime software. • Removed PowerPlay text from tool name. • Updated the IP name from ALTREMOTE_UPDATE to Remote Update Intel FPGA IP. • Rebranded as Intel. • Added the Low Power Variants table and the estimating power consumption steps to the "Cyclone V Device Datasheet" Overview section. • Updated the minimum value for t_{DH} to 2.5 for -6 speed grade/2.9 for -7 and -8 speed grade.

Date	Version	Changes
December 2016	2016.12.09	• Updated V_{ICM} (AC coupled) specifications for 1.5 V PCML in Receiver Specifications for Cyclone V GX, GT, SX, and ST Devices table. • Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Cyclone V Devices table. • Updated T_{init} specifications in the following tables: — FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices — FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices — AS Timing Parameters for AS ×1 and ×4 Configurations in Cyclone V Devices — PS Timing Parameters for Cyclone V Devices
June 2016	2016.06.10	• Changed pin capacitance to maximum values. • Updated SPI Master Timing Requirements for Cyclone V Devices table. — Added T_{su} and T_h specifications. — Removed T_{dinmax} specifications. • Updated SPI Master Timing Diagram. • Updated T_{clk} spec from maximum to minimum in I^2C Timing Requirements for Cyclone V Devices table.

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Date	Version	Changes
January 2015	2015.01.23	• Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps. Updated the note in the following tables: — Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices — Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices — Transceiver Compliance Specification for All Supported Protocol for Cyclone V Devices • Updated the description for $V_{CC\_AUX\_SHARED}$ to "HPS auxiliary power supply". Added a note to state that $V_{CC\_AUX\_SHARED}$ must be powered by the same source as VCC_AUX for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices. Updated in the following tables: — Absolute Maximum Ratings for Cyclone V Devices — HPS Power Supply Operating Conditions for Cyclone V SE, SX, and ST Devices • Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. • Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification. • Updated f_{VCO} maximum value from 1400 MHz to 1600 MHz for –C7 and –I7 speed grades in the PLL specifications table. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Added the following notes in the High-Speed I/O Specifications for Cyclone V Devices table: — The Cyclone V devices support true RSDS output standard with data rates of up to 230 Mbps using true LVDS output buffer types on all I/O banks. — The Cyclone V devices support true mini-LVDS output standard with data rates of up to 340 Mbps using true LVDS output buffer types on all I/O banks. • Updated HPS Clock Performance main_base_clk specifications from 462 MHz to 400 MHz for –C6 speed grade. • Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C7, –I7, –A7, and –C8 speed grades) and 1,850 MHz (for –C6 speed grade). • Changed the symbol for HPS PLL input jitter divide value from NR to N. • Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables: — SPI Master Timing Requirements for Cyclone V Devices — SPI Slave Timing Requirements for Cyclone V Devices • Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board. • Added HPS JTAG timing specifications. • Updated the configuration `.rbf` size (bits) for Cyclone V devices. • Added a note to Uncompressed .rbf Sizes for Cyclone V Devices table: The recommended EPCQ serial configuration devices are able to store more than one image.

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Date	Version	Changes
July 2014	3.9	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20. • Updated h2f_user2_clk specification for –C6, –C7, and –I7 speed grades in Table 34. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 35. • Updated T_d and T_h specifications in Table 41. • Added T_h specification in Table 43 and Figure 10. • Updated a note in Figure 17, Figure 18, and Figure 20 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 54. • Added DCLK device initialization clock source specification in Table 56. • Added description in "Configuration Files" section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature. • Added "Recommended EPCQ Serial Configuration Device" values in Table 57. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 59.
February 2014	3.8	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.7	• Updated Table 1, Table 3, Table 19, Table 20, Table 23, Table 25, Table 27, Table 34, Table 44, Table 51, Table 52, Table 55, and Table 61. • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 24, Table 25, Table 26, Table 27, Table 28, Table 32, Table 33, Table 49, Table 50, Table 51, Table 52, Table 53, Table 54, Table 55, Table 57, Table 58, Table 59, Table 60, and Table 62.
November 2013	3.6	Updated Table 23, Table 30, and Table 31.
October 2013	3.5	• Added "HPS PLL Specifications". • Added Table 23, Table 35, and Table 36. • Updated Table 1, Table 5, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, Table 28, Table 34, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, and Table 53. • Updated Figure 1, Figure 2, Figure 4, Figure 10, Figure 12, Figure 13, and Figure 16. • Removed table: GPIO Pulse Width for Cyclone V Devices.

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