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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

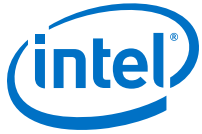
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Single ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba5u19i7sn



Transceiver Power Supply Operating Conditions

Table 5. Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices

Symbol	Description	Minimum ⁽⁸⁾	Typical	Maximum ⁽⁸⁾	Unit
V _{CCH_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V _{CCE_GXBL} ⁽⁹⁾⁽¹⁰⁾	Transmitter and receiver power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V
V _{CCL_GXBL} ⁽⁹⁾⁽¹⁰⁾	Clock network power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V

Related Information

- [PCIe Supported Configurations and Placement Guidelines](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.
- [6.144-Gbps Support Capability in Cyclone V GT Devices](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

⁽⁸⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁹⁾ Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which require full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

⁽¹⁰⁾ Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.



HPS Power Supply Operating Conditions

Table 6. HPS Power Supply Operating Conditions for Cyclone V SX and ST Devices

This table lists the steady-state voltage and current values expected from Cyclone V system-on-a-chip (SoC) devices with Arm*-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions for Cyclone V Devices* table for the steady-state voltage values expected from the FPGA portion of the Cyclone V SoC devices.

Symbol	Description	Condition	Minimum ⁽¹¹⁾	Typical	Maximum ⁽¹¹⁾	Unit
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	—	1.07	1.1	1.13	V
V _{CCPD_HPS} ⁽¹²⁾	HPS I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V _{CCIO_HPS}	HPS I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V ⁽¹³⁾	1.283	1.35	1.418	V
		1.2 V	1.14	1.2	1.26	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

continued...

- ⁽¹¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.
- ⁽¹²⁾ V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.
- ⁽¹³⁾ V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.



Symbol	Description	Condition	Minimum ⁽¹¹⁾	Typical	Maximum ⁽¹¹⁾	Unit
		1.8 V	1.71	1.8	1.89	V
V _{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CC_AUX_SHARED} ⁽¹⁴⁾	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

[Recommended Operating Conditions](#) on page 8

Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based EPE and the Intel® Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- [Early Power Estimator User Guide](#)
Provides more information about power estimation tools.
- [Power Analysis chapter, Intel Quartus Prime Handbook](#)
Provides more information about power estimation tools.

⁽¹¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹⁴⁾ V_{CC_AUX_SHARED} must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.



I/O Standard	V _{CCIO} (V)			V _{ID} (mV) ⁽²¹⁾			V _{ICM(DC)} (V)			V _{OD} (V) ⁽²²⁾			V _{OCM} (V) ⁽²²⁾⁽²³⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL ⁽²⁹⁾	—	—	—	300	—	—	0.60	D _{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D _{MAX} > 700 Mbps	1.60						
SLVS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
Sub-LVDS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
HiSpi	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—

Related Information

- [AN522: Implementing Bus LVDS Interface in Supported Intel Device Families](#)
Provides more information about BLVDS interface support in Intel devices.
- [Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices](#) on page 25
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

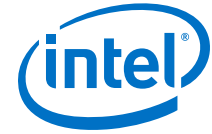
This section provides performance characteristics of Cyclone V core and periphery blocks.

⁽²¹⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

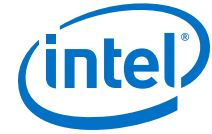
⁽²²⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²³⁾ This applies to default pre-emphasis setting only.

⁽²⁹⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

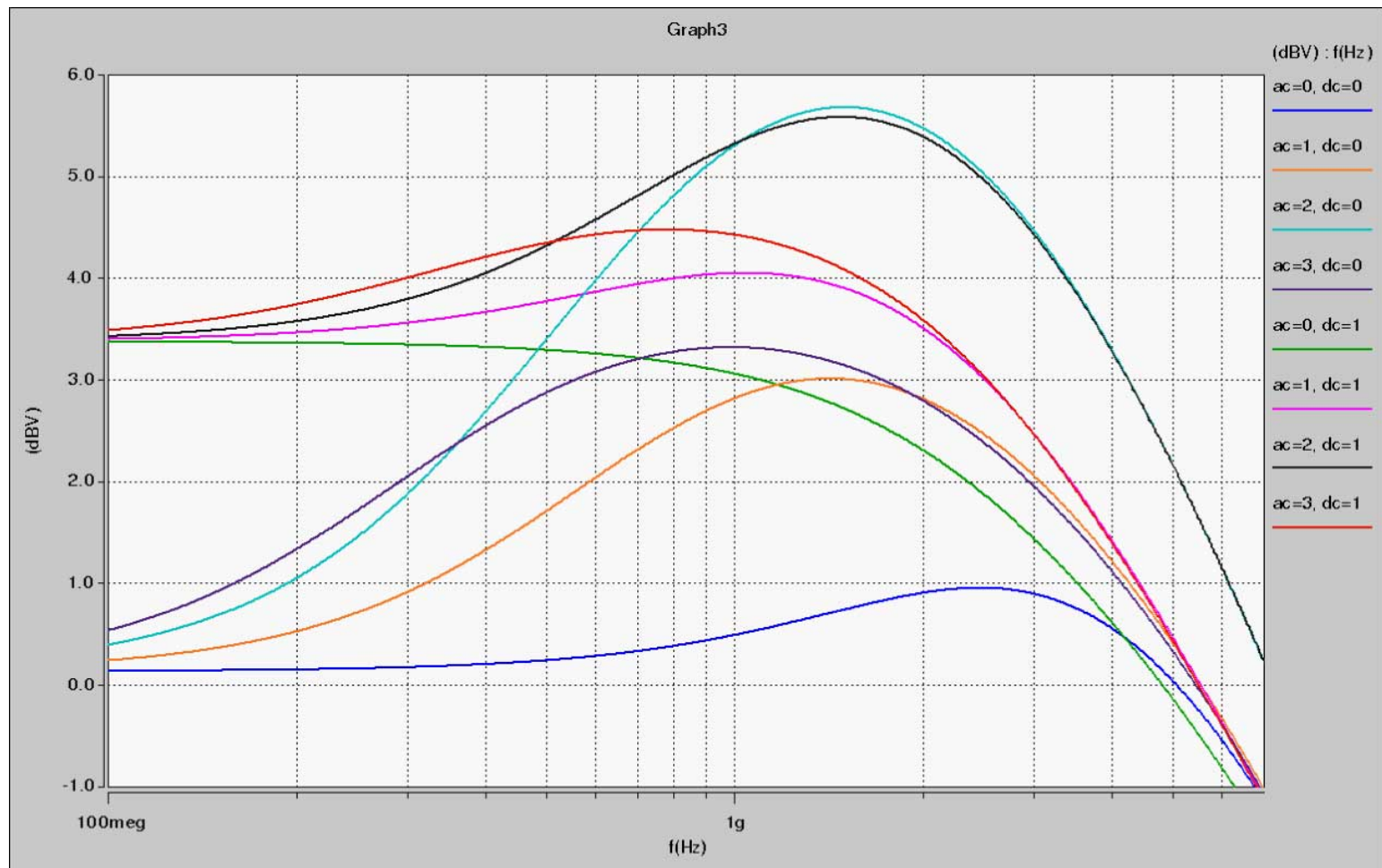


- [6.144-Gbps Support Capability in Cyclone V GT Devices](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.



CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 4. CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices





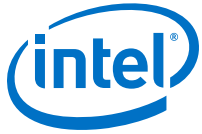
Protocol	Sub-protocol	Data Rate (Mbps)
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII ⁽⁵¹⁾	4,915.2
	CPRI E60LVII ⁽⁵¹⁾	6,144
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970
VbyOne	VbyOne 3750	3,750
HiGig+	HIGIG 3750	3,750

Related Information

- [PCIe Supported Configurations and Placement Guidelines](#)

Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.

⁽⁵¹⁾ For CPRI E48LVII and E60LVII, Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144 Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.



High-Speed I/O Specifications

Table 34. High-Speed I/O Specifications for Cyclone V Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The Cyclone V devices support the following output standards using true LVDS output buffer types on all I/O banks.

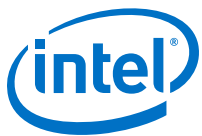
- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	-C6			-C7, -17			-C8, -A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40 ⁽⁶³⁾	5	—	437.5	5	—	420	5	—	320	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40 ⁽⁶³⁾	5	—	320	5	—	320	5	—	275	MHz
$f_{\text{HCLK_OUT}}$ (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 4 to 10 ⁽⁶⁴⁾	⁽⁶⁵⁾	—	840	⁽⁶⁵⁾	—	740	⁽⁶⁵⁾	—	640	Mbps
continued...												

⁽⁶³⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁶⁴⁾ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁶⁵⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

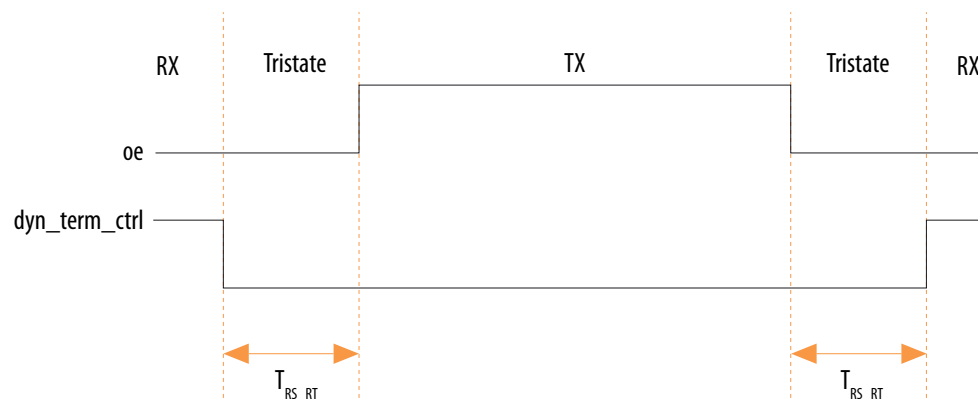


OCT Calibration Block Specifications

Table 38. OCT Calibration Block Specifications for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT/ R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for `oe` and `dyn_term_ctrl` Signals



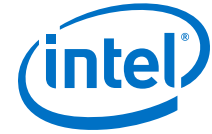


Figure 7. SPI Master Timing Diagram

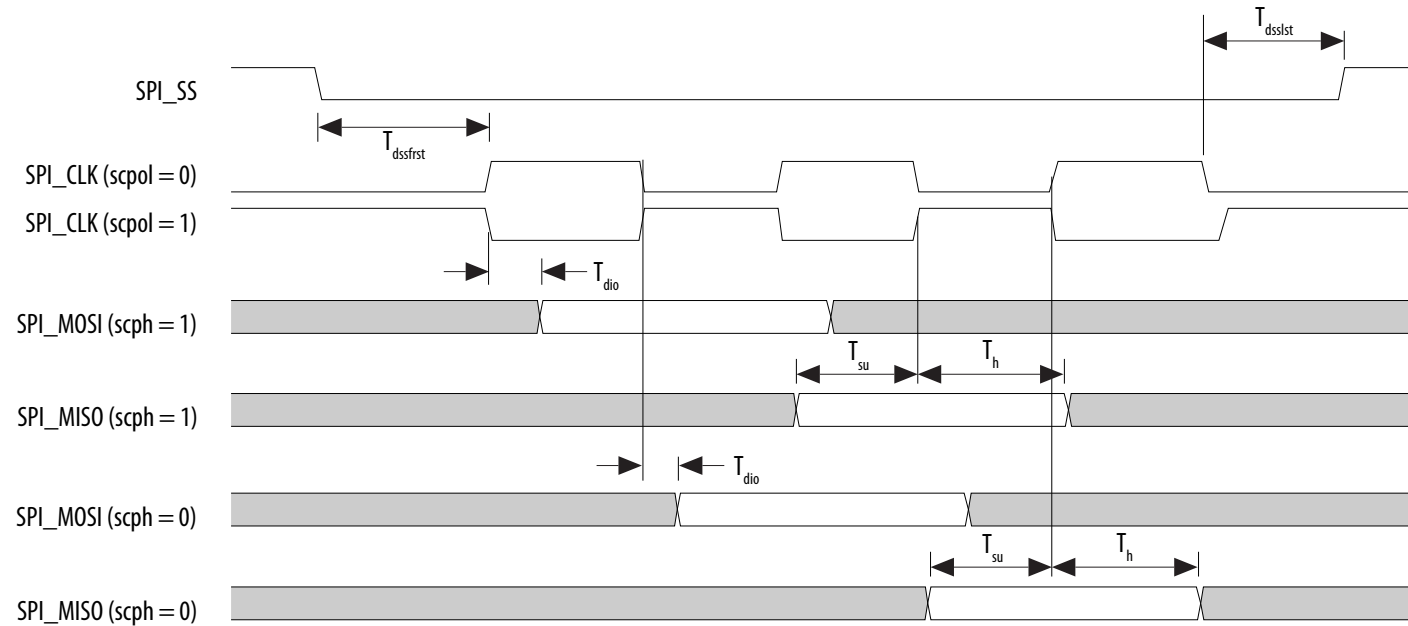


Table 45. SPI Slave Timing Requirements for Cyclone V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	20	—	ns
T_s	MOSI Setup time	5	—	ns
T_h	MOSI Hold time	5	—	ns
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	ns
T_d	MISO output delay	—	6	ns



Symbol	Description	Min	Max	Unit
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Figure 15. NAND Command Latch Timing Diagram

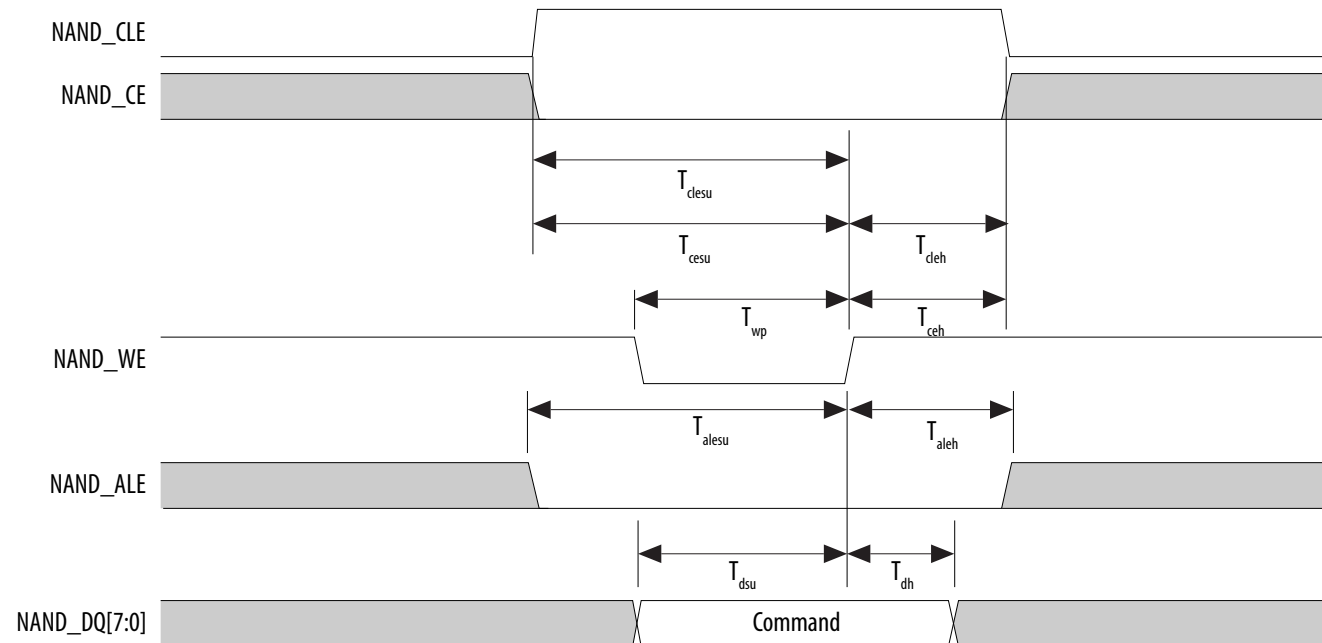


Figure 16. NAND Address Latch Timing Diagram

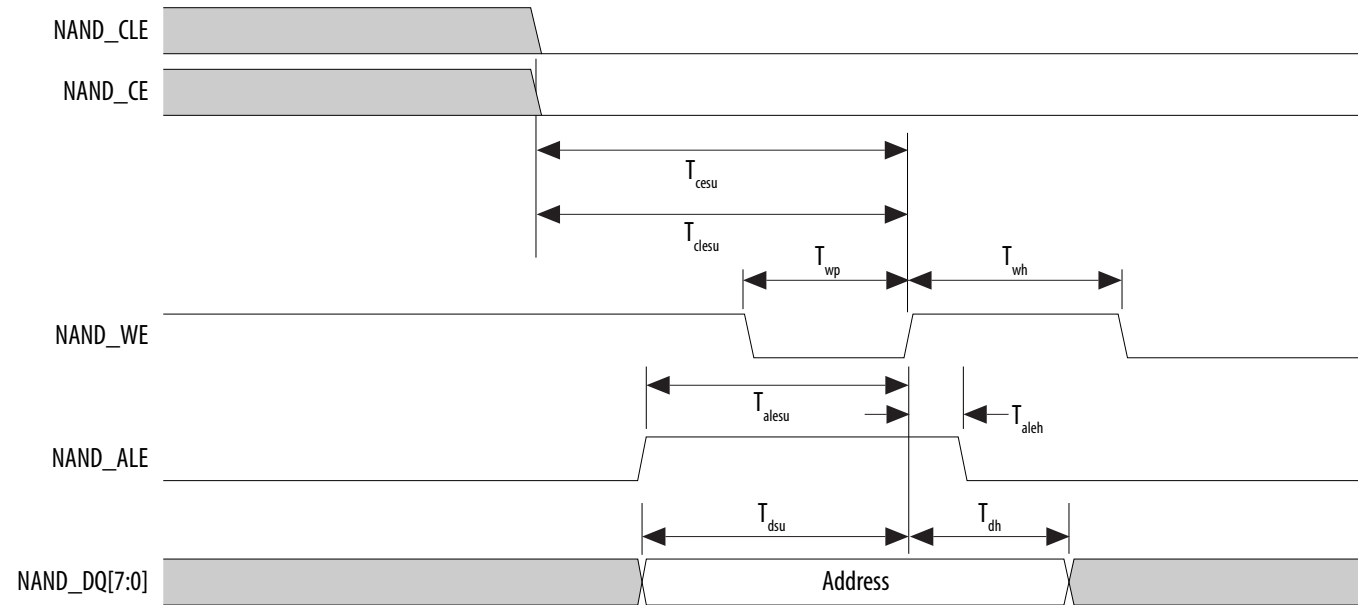
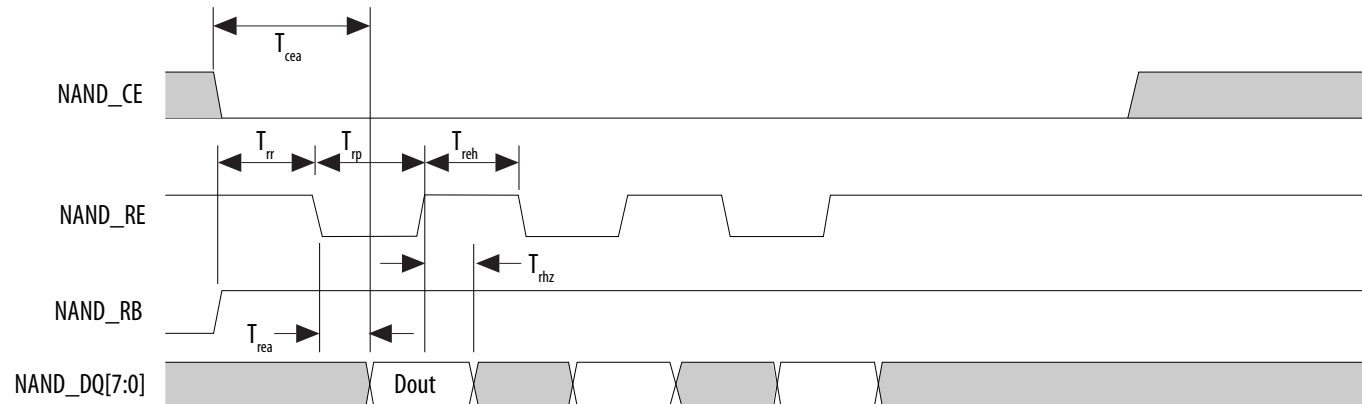


Figure 18. NAND Data Read Timing Diagram



Arm Trace Timing Characteristics

Table 53. Arm Trace Timing Requirements for Cyclone V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 μ s. The pulse width is based on a debounce clock frequency of 1 MHz.



Symbol	Description	Min	Max	Unit
t _{JPCO}	JTAG port clock to output	—	11 ⁽⁷⁶⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁷⁶⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁷⁶⁾	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP $\times 16$ where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

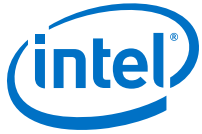
Cyclone V devices use additional clock cycles to decrypt and decompress the configuration data. If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio - 1) clock cycles after the last data is latched into the Cyclone V device.

Table 57. DCLK-to-DATA[] Ratio for Cyclone V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1

continued...

⁽⁷⁶⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.



Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CK}^{(83)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
$t_{ST2CK}^{(83)}$	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}^{(84)}$	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/ \times 16$)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽⁸⁵⁾	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing

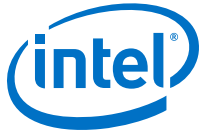
Provides the FPP configuration timing waveforms.

⁽⁸²⁾ This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

⁽⁸³⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽⁸⁴⁾ N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

⁽⁸⁵⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.



DCLK Frequency Specification in the AS Configuration Scheme

Table 61. DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

Passive Serial (PS) Configuration Timing

Table 62. PS Timing Parameters for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μs
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁸⁹⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽⁹⁰⁾	μs
t _{CF2CK} ⁽⁹¹⁾	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽⁹¹⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns

continued...

⁽⁸⁹⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽⁹⁰⁾ You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

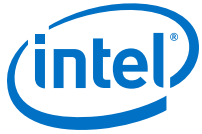
⁽⁹¹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.



Variant	Member Code	Active Serial ⁽⁹⁶⁾			Fast Passive Parallel ⁽⁹⁷⁾		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Cyclone V GX	A9	4	100	257	16	125	51
	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

⁽⁹⁶⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽⁹⁷⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Cyclone V I/O Timing Spreadsheet](#)

Provides the Cyclone V Excel-based I/O timing spreadsheet.

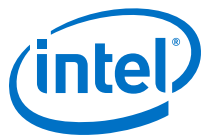
Programmable IOE Delay

Table 68. I/O element (IOE) Programmable Delay for Cyclone V Devices

Parameter ⁽¹⁰⁰⁾	Available Settings	Minimum Offset ⁽¹⁰¹⁾	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C6	–C7	–C8	–I7	–A7	
D1	32	0	0.508	0.517	0.971	1.187	1.194	1.179	1.160	ns
D3	8	0	1.761	1.793	3.291	4.022	3.961	3.999	3.929	ns
D4	32	0	0.510	0.519	1.180	1.187	1.195	1.180	1.160	ns
D5	32	0	0.508	0.517	0.970	1.186	1.194	1.179	1.179	ns

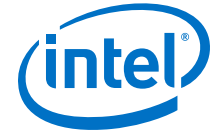
⁽¹⁰⁰⁾ You can set this value in the Intel Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹⁰¹⁾ Minimum offset does not include the intrinsic delay.



Term	Definition
	<p>The diagram illustrates the timing relationships for the PLL specifications. It shows four signals: TMS, TDI, TCK, and TDO. TMS and TDI are represented by rectangular pulses. TCK is a clock signal with a period t_{JCH} and a high pulse width t_{JCP}. TDO is a data signal with a setup time t_{JPCO} before a clock edge and a hold time t_{JPH} after a clock edge. The diagram also shows the time between a clock edge and the data signal t_{JPXZ}.</p>
PLL specifications	Diagram of PLL specifications

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Date	Version	Changes
July 2014	3.9	<ul style="list-style-type: none"> Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20. Updated h2f_user2_clk specification for -C6, -C7, and -I7 speed grades in Table 34. Updated description in "HPS PLL Specifications" section. Updated VCO range maximum specification in Table 35. Updated T_d and T_h specifications in Table 41. Added T_h specification in Table 43 and Figure 10. Updated a note in Figure 17, Figure 18, and Figure 20 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. Removed "Remote update only in AS mode" specification in Table 54. Added DCLK device initialization clock source specification in Table 56. Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. Added "Recommended EPCQ Serial Configuration Device" values in Table 57. Removed $f_{MAX_RU_CLK}$ specification in Table 59.
February 2014	3.8	<ul style="list-style-type: none"> Updated $V_{CCRSTCLK_HPS}$ maximum specification in Table 1. Added $V_{CC_AUX_SHARED}$ specification in Table 1.
December 2013	3.7	<ul style="list-style-type: none"> Updated Table 1, Table 3, Table 19, Table 20, Table 23, Table 25, Table 27, Table 34, Table 44, Table 51, Table 52, Table 55, and Table 61. Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 24, Table 25, Table 26, Table 27, Table 28, Table 32, Table 33, Table 49, Table 50, Table 51, Table 52, Table 53, Table 54, Table 55, Table 57, Table 58, Table 59, Table 60, and Table 62.
November 2013	3.6	Updated Table 23, Table 30, and Table 31.
October 2013	3.5	<ul style="list-style-type: none"> Added "HPS PLL Specifications". Added Table 23, Table 35, and Table 36. Updated Table 1, Table 5, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, Table 28, Table 34, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, and Table 53. Updated Figure 1, Figure 2, Figure 4, Figure 10, Figure 12, Figure 13, and Figure 16. Removed table: GPIO Pulse Width for Cyclone V Devices.
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