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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-FBGA
Supplier Device Package	672-UBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba5u23c8n



Table 2. Absolute Maximum Ratings for Cyclone V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage and periphery circuitry power supply	-0.5	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.5	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.5	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.90	V
V _{CCIO}	I/O power supply	-0.5	3.90	V
V _{CCA_FPLL}	Phase-locked loop (PLL) analog power supply	-0.5	3.25	V
V _{CCH_GXB}	Transceiver high voltage power	-0.5	3.25	V
V _{CCE_GXB}	Transceiver power	-0.5	1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.5	1.50	V
V _I	DC input voltage	-0.5	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.5	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.5	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.5	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.5	3.90	V
V _{CCPLL_HPS}	HPS PLL analog power supply	-0.5	3.25	V
V _{CC_AUX_SHARED} ⁽¹⁾	HPS auxiliary power supply	-0.5	3.25	V
I _{OUT}	DC output current per pin	-25	40	mA
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (no bias)	-65	150	°C

⁽¹⁾ V_{CC_AUX_SHARED} must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.



Transceiver Power Supply Operating Conditions

Table 5. Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices

Symbol	Description	Minimum ⁽⁸⁾	Typical	Maximum ⁽⁸⁾	Unit
V _{CCH_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V _{CCE_GXBL} ⁽⁹⁾⁽¹⁰⁾	Transmitter and receiver power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V
V _{CCL_GXBL} ⁽⁹⁾⁽¹⁰⁾	Clock network power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V

Related Information

- [PCIe Supported Configurations and Placement Guidelines](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.
- [6.144-Gbps Support Capability in Cyclone V GT Devices](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

⁽⁸⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁹⁾ Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which require full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

⁽¹⁰⁾ Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.



I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	—	—	—

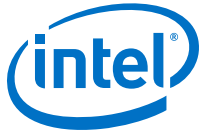
Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 17. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Cyclone V Devices

I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁹⁾ (mA)	I _{OH} ⁽¹⁹⁾ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} - 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} - 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} - 0.25	V _{REF} + 0.25	V _{TT} - 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} - 0.25	V _{REF} + 0.25	0.28	V _{CCIO} - 0.28	13.4	-13.4

continued...

⁽¹⁹⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



Differential SSTL I/O Standards

Table 18. Differential SSTL I/O Standards for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.2	—	V _{CCIO} /2 + 0.2	0.62	V _{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.175	—	V _{CCIO} /2 + 0.175	0.5	V _{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	⁽²⁰⁾	V _{CCIO} /2 - 0.15	—	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-135	1.283	1.35	1.45	0.18	⁽²⁰⁾	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-125	1.19	1.25	1.31	0.18	⁽²⁰⁾	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})

Differential HSTL and HSUL I/O Standards

Table 19. Differential HSTL and HSUL I/O Standards for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	—	0.5 × V _{CCIO}	—	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V _{CCIO} - 0.12	0.5 × V _{CCIO}	0.5 × V _{CCIO} + 0.12	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44	0.44

⁽²⁰⁾ The maximum value for V_{SWING(DC)} is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V_{IH(DC)} and V_{IL(DC)}).



I/O Standard	V _{CCIO} (V)			V _{ID} (mV) ⁽²¹⁾			V _{ICM(DC)} (V)			V _{OD} (V) ⁽²²⁾			V _{OCM} (V) ⁽²²⁾⁽²³⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL ⁽²⁹⁾	—	—	—	300	—	—	0.60	D _{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D _{MAX} > 700 Mbps	1.60						
SLVS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
Sub-LVDS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
HiSpi	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—

Related Information

- [AN522: Implementing Bus LVDS Interface in Supported Intel Device Families](#)
Provides more information about BLVDS interface support in Intel devices.
- [Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices](#) on page 25
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Cyclone V core and periphery blocks.

⁽²¹⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

⁽²²⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽²³⁾ This applies to default pre-emphasis setting only.

⁽²⁹⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.



- [6.144-Gbps Support Capability in Cyclone V GT Devices](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
		-C8, -A7 speed grades	600	—	1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f _{OUT}	Output frequency for internal global or regional clock	-C6, -C7, -I7 speed grades	—	—	550 ⁽⁵⁴⁾	MHz
		-C8, -A7 speed grades	—	—	460 ⁽⁵⁴⁾	MHz
f _{OUT_EXT}	Output frequency for external clock output	-C6, -C7, -I7 speed grades	—	—	667 ⁽⁵⁴⁾	MHz
		-C8, -A7 speed grades	—	—	533 ⁽⁵⁴⁾	MHz
t _{OUTDUTY}	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
t _{DYCONFIGCLK}	Dynamic configuration clock for <code>mgmt_clk</code> and <code>scanclk</code>	—	—	—	100	MHz
t _{LOCK}	Time required to lock from end-of-device configuration or deassertion of <code>areset</code>	—	—	—	1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f _{CLBW}	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High ⁽⁵⁵⁾	—	4	—	MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps

continued...

- (53) The VCO frequency reported by the Intel Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.
- (54) This specification is limited by the lower of the two: $I/O f_{MAX}$ or F_{OUT} of the PLL.
- (55) High bandwidth PLL settings are not supported in external feedback mode.



Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	-C6	-C7, -I7	-C8, -A7	
	ROM, all supported width	0	1	420	350	300	MHz
M10K Block	Single-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	275	240	180	MHz
	True dual port, all supported widths	0	1	315	275	240	MHz
	ROM, all supported widths	0	1	315	275	240	MHz

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.



High-Speed I/O Specifications

Table 34. High-Speed I/O Specifications for Cyclone V Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The Cyclone V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	-C6			-C7, -I7			-C8, -A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40 ⁽⁶³⁾	5	—	437.5	5	—	420	5	—	320	MHz
f _{HCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40 ⁽⁶³⁾	5	—	320	5	—	320	5	—	275	MHz
f _{HCLK_OUT} (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J = 4 to 10 ⁽⁶⁴⁾	⁽⁶⁵⁾	—	840	⁽⁶⁵⁾	—	740	⁽⁶⁵⁾	—	640	Mbps
<i>continued...</i>												

⁽⁶³⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁶⁴⁾ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁶⁵⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.



DLL Frequency Range Specifications

Table 35. DLL Frequency Range Specifications for Cyclone V Devices

Parameter	-C6	-C7, -I7	-C8	Unit
DLL operating frequency range	167 – 400	167 – 400	167 – 333	MHz

DQS Logic Block Specifications

Table 36. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Cyclone V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	-C6	-C7, -I7	-C8	Unit
2	40	80	80	ps

Memory Output Clock Jitter Specifications

Table 37. Memory Output Clock Jitter Specifications for Cyclone V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma.

Intel recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Parameter	Clock Network	Symbol	-C6		-C7, -I7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	-60	60	-70	70	-70	70	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	—	90	—	100	—	100	ps



HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 41. HPS PLL VCO Frequency Range for Cyclone V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	-C7, -I7, -A7, -C8	320	1,600	MHz
	-C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

[Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 42. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

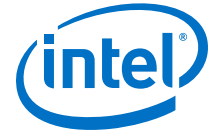
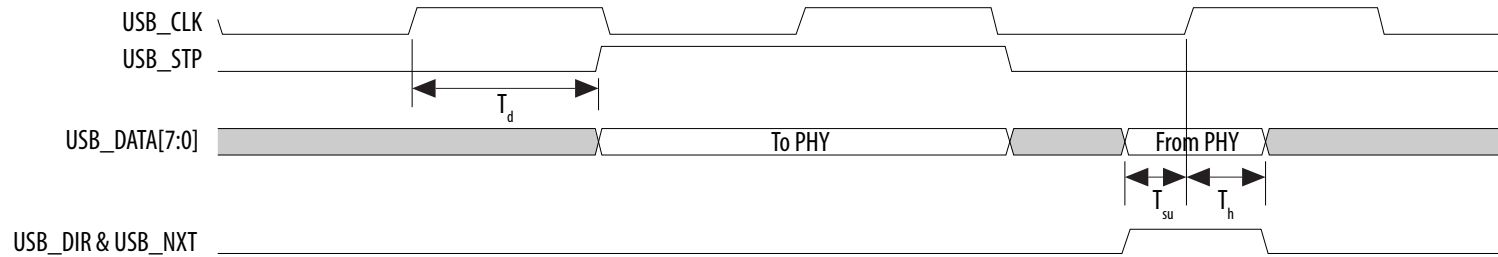


Figure 10. USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 48. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
T_{duty}	TX_CLK duty cycle	45	—	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	-0.85	—	0.15	ns

Figure 11. RGMII TX Timing Diagram

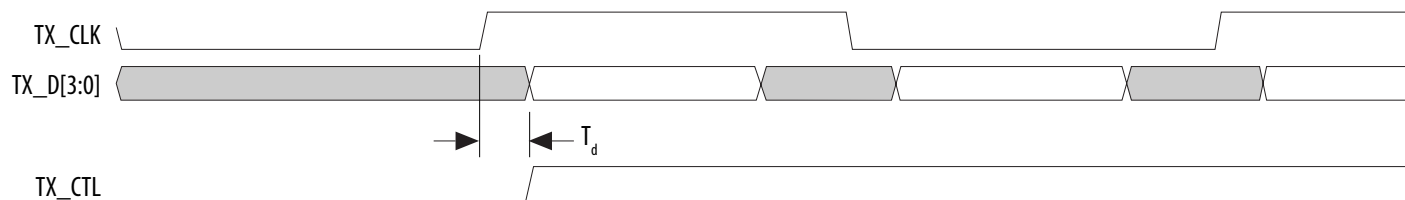
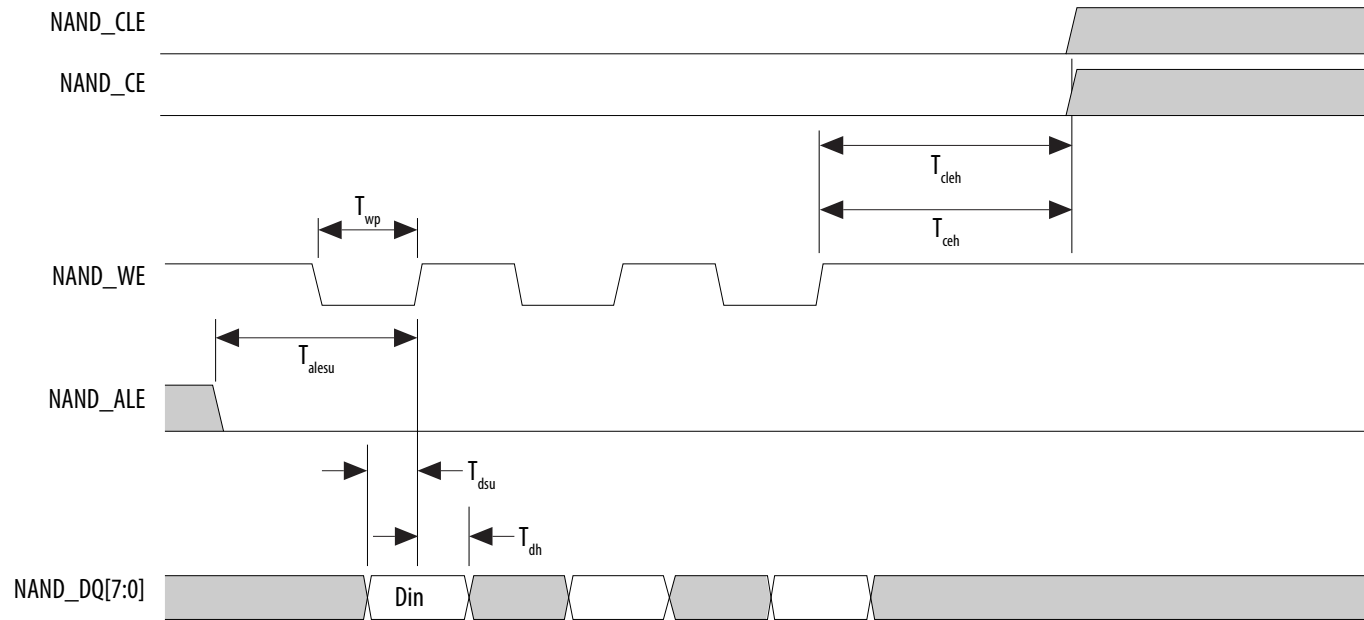




Figure 17. NAND Data Write Timing Diagram





CAN Interface

The maximum controller area network (CAN) data rate is 1 Mbps.

HPS JTAG Timing Specifications

Table 54. HPS JTAG Timing Parameters and Values for Cyclone V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30	—	ns
t _{JCH}	TCK clock high time	14	—	ns
t _{JCL}	TCK clock low time	14	—	ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	—	ns
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	12 ⁽⁷³⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁷³⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁷³⁾	ns

Configuration Specifications

This section provides configuration specifications and timing for Cyclone V devices.

⁽⁷³⁾ A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.



Symbol	Description	Min	Max	Unit
t _{JPCO}	JTAG port clock to output	—	11 ⁽⁷⁶⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁷⁶⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁷⁶⁾	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Cyclone V devices use additional clock cycles to decrypt and decompress the configuration data. If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Cyclone V device.

Table 57. DCLK-to-DATA[] Ratio for Cyclone V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1

continued...

⁽⁷⁶⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.



Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CK}^{(83)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
$t_{ST2CK}^{(83)}$	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}^{(84)}$	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/ \times 16$)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽⁸⁵⁾	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

⁽⁸²⁾ This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

⁽⁸³⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽⁸⁴⁾ N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

⁽⁸⁵⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.



Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Cyclone V I/O Timing Spreadsheet](#)

Provides the Cyclone V Excel-based I/O timing spreadsheet.

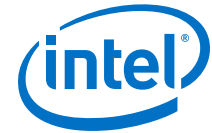
Programmable IOE Delay

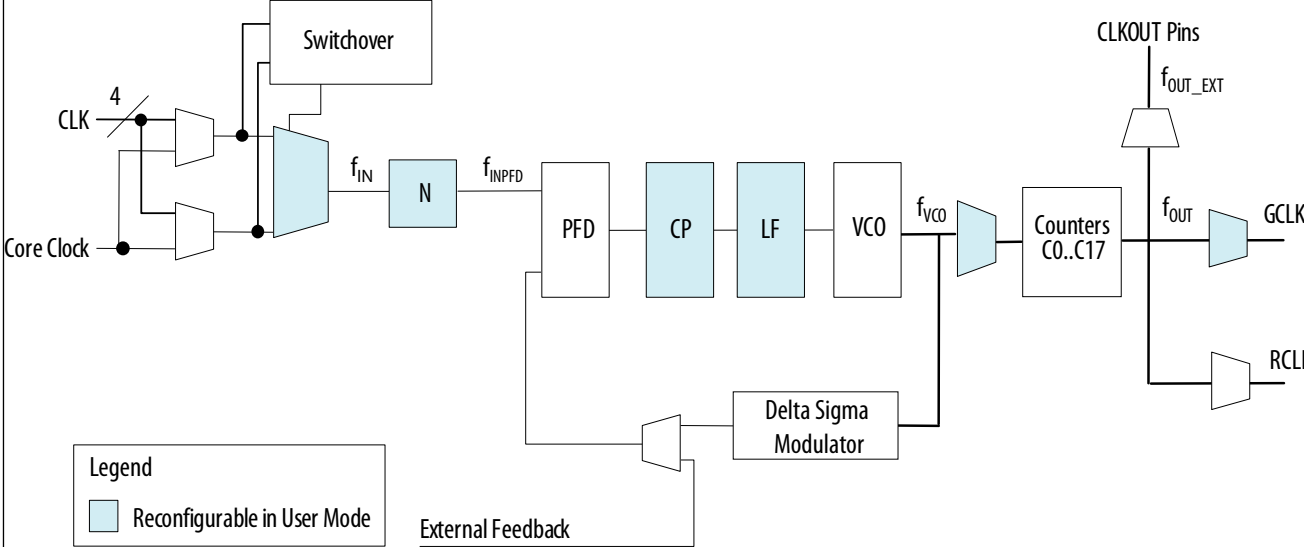
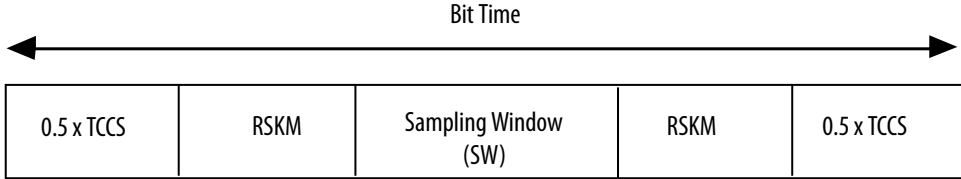
Table 68. I/O element (IOE) Programmable Delay for Cyclone V Devices

Parameter ⁽¹⁰⁰⁾	Available Settings	Minimum Offset ⁽¹⁰¹⁾	Fast Model		Slow Model					Unit
			Industrial	Commercial	-C6	-C7	-C8	-I7	-A7	
D1	32	0	0.508	0.517	0.971	1.187	1.194	1.179	1.160	ns
D3	8	0	1.761	1.793	3.291	4.022	3.961	3.999	3.929	ns
D4	32	0	0.510	0.519	1.180	1.187	1.195	1.180	1.160	ns
D5	32	0	0.508	0.517	0.970	1.186	1.194	1.179	1.179	ns

⁽¹⁰⁰⁾ You can set this value in the Intel Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹⁰¹⁾ Minimum offset does not include the intrinsic delay.



Term	Definition
	 <p>The diagram illustrates the PLL architecture. It starts with a 'Core Clock' input that branches into a '4' divider and a 'Switchover' block. The 'Switchover' block selects between the divided core clock and an external 'External Feedback' signal. The selected signal, labeled f_{IN}, passes through a divider 'N' to become f_{INPFD}. This signal then goes through a 'PFD' (Phase-Frequency Detector), a 'CP' (Charge Pump), a 'LF' (Loop Filter), and a 'VCO' (Voltage-Controlled Oscillator) to produce f_{VCO}. The f_{VCO} signal is then divided by a 'Counters CO..C17' block to produce f_{OUT}. This output is available at 'CLKOUT Pins' as f_{OUT_EXT} and also passes through a divider to become 'RCLK'. A 'Delta Sigma Modulator' block is connected to the feedback path between the PFD and the VCO.</p> <p>Legend Reconfigurable in User Mode</p> <p>Note: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>
R _L	Receiver differential input discrete resistor (external to the Cyclone V device).
Sampling window (SW)	<p>Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:</p>  <p>The timing diagram shows a horizontal axis labeled 'Bit Time'. A double-headed arrow spans the width of the diagram. Below the axis, a sequence of five rectangular blocks is shown: '0.5 x TCCS', 'RSKM', 'Sampling Window (SW)', 'RSKM', and '0.5 x TCCS'. The 'Sampling Window (SW)' is the central block, and the 'RSKM' blocks are positioned on either side of it.</p>

continued...



Term	Definition
Single-ended voltage referenced I/O standard	<p>The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.</p> <p>Single-Ended Voltage Referenced I/O Standard</p>
t_c	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input

continued...



Term	Definition
t _{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t _{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t _{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t _c /w)
V _{CM(DC)}	DC common mode input voltage.
V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage
V _{IH(DC)}	High-level DC input voltage
V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL(AC)}	Low-level AC input voltage
V _{IL(DC)}	Low-level DC input voltage
V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V _{SWING}	Differential input voltage
V _X	Input differential cross point voltage
V _{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor