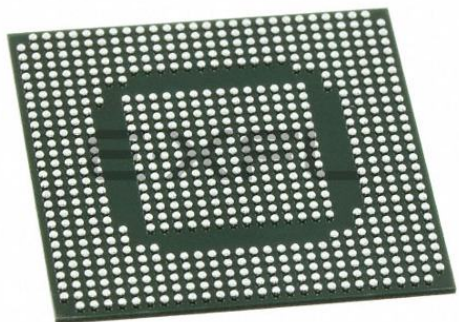


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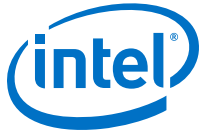
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Single ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-FBGA
Supplier Device Package	672-UBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba5u23c8sn



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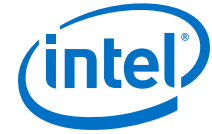
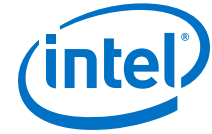


Table 2. Absolute Maximum Ratings for Cyclone V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage and periphery circuitry power supply	-0.5	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.5	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.5	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.90	V
V _{CCIO}	I/O power supply	-0.5	3.90	V
V _{CCA_FPLL}	Phase-locked loop (PLL) analog power supply	-0.5	3.25	V
V _{CCH_GXB}	Transceiver high voltage power	-0.5	3.25	V
V _{CCE_GXB}	Transceiver power	-0.5	1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.5	1.50	V
V _I	DC input voltage	-0.5	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.5	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.5	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.5	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.5	3.90	V
V _{CCPLL_HPS}	HPS PLL analog power supply	-0.5	3.25	V
V _{CC_AUX_SHARED} ⁽¹⁾	HPS auxiliary power supply	-0.5	3.25	V
I _{OUT}	DC output current per pin	-25	40	mA
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (no bias)	-65	150	°C

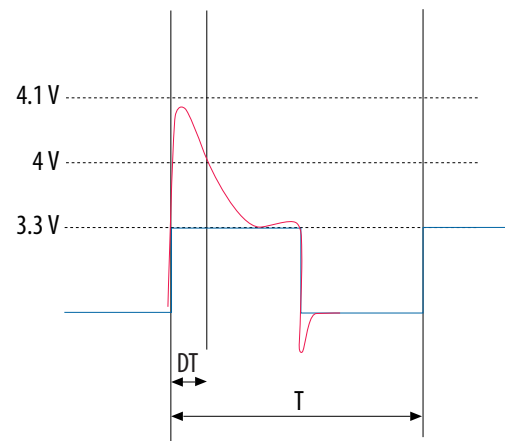
⁽¹⁾ V_{CC_AUX_SHARED} must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.



Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

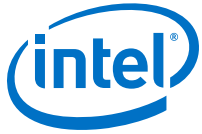
For an overshoot of 3.8 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

Figure 1. Cyclone V Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Cyclone V devices.



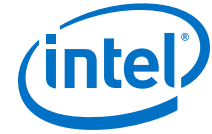
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 11. OCT Variation after Power-Up Calibration for Cyclone V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0°C to 85°C .

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	



Single-Ended I/O Standards

Table 15. Single-Ended I/O Standards for Cyclone V Devices

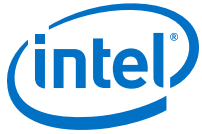
I/O Standard	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁸⁾ (mA)	I _{OH} ⁽¹⁸⁾ (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} - 0.2	2	-2
3.0-V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} - 0.2	0.1	-0.1
3.0-V PCI*	2.85	3	3.15	—	0.3 × V _{CCIO}	0.5 × V _{CCIO}	V _{CCIO} + 0.3	0.1 × V _{CCIO}	0.9 × V _{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V _{CCIO}	0.5 × V _{CCIO}	V _{CCIO} + 0.3	0.1 × V _{CCIO}	0.9 × V _{CCIO}	1.5	-0.5
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V _{CCIO}	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} - 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 × V _{CCIO}	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.25 × V _{CCIO}	0.75 × V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 × V _{CCIO}	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.25 × V _{CCIO}	0.75 × V _{CCIO}	2	-2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
<i>continued...</i>									

⁽¹⁸⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



Differential SSTL I/O Standards

Table 18. Differential SSTL I/O Standards for Cyclone V Devices

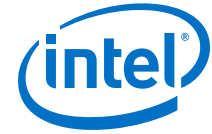
I/O Standard	V _{CCIO} (V)			V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.2	—	V _{CCIO} /2 + 0.2	0.62	V _{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.175	—	V _{CCIO} /2 + 0.175	0.5	V _{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	⁽²⁰⁾	V _{CCIO} /2 – 0.15	—	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	2(V _{IL(AC)} – V _{REF})
SSTL-135	1.283	1.35	1.45	0.18	⁽²⁰⁾	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	2(V _{IL(AC)} – V _{REF})
SSTL-125	1.19	1.25	1.31	0.18	⁽²⁰⁾	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	2(V _{IL(AC)} – V _{REF})

Differential HSTL and HSUL I/O Standards

Table 19. Differential HSTL and HSUL I/O Standards for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	—	0.5 × V _{CCIO}	—	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V _{CCIO} – 0.12	0.5 × V _{CCIO}	0.5 × V _{CCIO} + 0.12	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44	0.44

⁽²⁰⁾ The maximum value for V_{SWING(DC)} is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V_{IH(DC)} and V_{IL(DC)}).



Differential I/O Standard Specifications

Table 20. Differential I/O Standard Specifications for Cyclone V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) ⁽²¹⁾			$V_{ICM(DC)}$ (V)			V_{OD} (V) ⁽²²⁾			V_{OCM} (V) ⁽²²⁾⁽²³⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to <i>Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices</i> table.														
2.5 V LVDS ⁽²⁴⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.05	$D_{MAX} \leq 700$ Mbps	1.80	0.247	—	0.6	1.125	1.25	1.375
							1.05	$D_{MAX} > 700$ Mbps	1.55						
BLVDS ⁽²⁵⁾⁽²⁶⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO) ⁽²⁷⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) (28)	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
continued...															

⁽²¹⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM} .

⁽²²⁾ R_L range: $90 \leq R_L \leq 110 \Omega$.

⁽²³⁾ This applies to default pre-emphasis setting only.

⁽²⁴⁾ For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rate above 700 Mbps and 0.00 V to 1.85 V for data rate below 700 Mbps.

⁽²⁵⁾ There are no fixed V_{ICM} , V_{OD} , and V_{OCM} specifications for BLVDS. They depend on the system topology.

⁽²⁶⁾ For more information about BLVDS interface support in Intel devices, refer to *AN522: Implementing Bus LVDS Interface in Supported Intel Device Families*.

⁽²⁷⁾ For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

⁽²⁸⁾ For optimized mini-LVDS receiver performance, the receiver voltage input range must be within 0.300 V to 1.425 V.



Table 22. Transceiver Clocks Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5 ⁽³⁰⁾			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	100/125 ⁽³⁷⁾	75	—	100/125 ⁽³⁷⁾	75	—	100/125 ⁽³⁷⁾	MHz

Table 23. Receiver Specifications for Cyclone V GX, GT, SX, and ST Devices

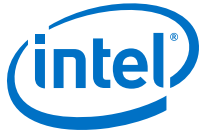
Symbol/Description	Condition	Transceiver Speed Grade 5 ⁽³⁰⁾			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS										
Data rate ⁽³⁸⁾	—	614	—	5000/6144 ⁽³⁵⁾	614	—	3125	614	—	2500	Mbps
Absolute V _{MAX} for a receiver pin ⁽³⁹⁾	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V _{MIN} for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	—	—	2.2	V
continued...											

continued...

⁽³⁷⁾ The maximum supported clock frequency is 100 MHz if the PCIe hard IP block is enabled or 125 MHz if the PCIe hard IP block is not enabled.

⁽³⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

⁽³⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.



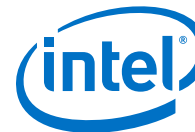
Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

Table 27. Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting ⁽⁴⁸⁾	V_{OD} Value (mV)	V_{OD} Setting ⁽⁴⁸⁾	V_{OD} Value (mV)
V_{OD} differential peak-to-peak typical	6 ⁽⁴⁹⁾	120	34	680
	7 ⁽⁴⁹⁾	140	35	700
	8 ⁽⁴⁹⁾	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040
continued...				

(48) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

(49) Only valid for data rates ≤ 5 Gbps.



Symbol	V _{OD} Setting ⁽⁴⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁴⁸⁾	V _{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

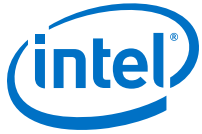
- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Cyclone V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100 \Omega$ and $|C| = 1st\ post\ tap\ pre-emphasis\ setting$.
- $|B| - |C| > 5$ for data rates $< 5\ Gbps$ and $|B| - |C| > 8.25$ for data rates $> 5\ Gbps$.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

⁽⁴⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.



Exceptions for PCIe Gen2 design:

- V_{OD} setting = 50 and pre-emphasis setting = 22 are allowed for PCIe Gen2 design with transmit de-emphasis -6dB setting (pipe_txdeemp = 1'b0) using Intel PCIe Hard IP and PIPE IP cores.
- V_{OD} setting = 50 and pre-emphasis setting = 12 are allowed for PCIe Gen2 design with transmit de-emphasis -3.5dB setting (pipe_txdeemp = 1'b1) using Intel PCIe Hard IP and PIPE IP cores.

For example, when $V_{OD} = 800$ mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Cyclone V HSSI HSPICE models.

Table 28. Transmitter Pre-Emphasis Levels for Cyclone V Devices

Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting	Intel Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
continued...								

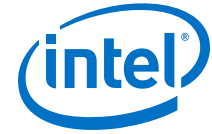


Symbol		Condition	-C6			-C7, -I7			-C8, -A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
	Emulated Differential I/O Standards with Three External Output Resistor Networks- f_{HSDR} (data rate) ⁽⁶⁷⁾	SERDES factor J = 4 to 10	(65)	—	640	(65)	—	640	(65)	—	550	Mbps
	Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)	SERDES factor J = 4 to 10	(65)	—	170	(65)	—	170	(65)	—	170	Mbps
	$t_{x \text{ Jitter}}$ -True Differential I/O Standards ⁽⁶⁷⁾	Total Jitter for Data Rate, 600 Mbps – 840 Mbps	—	—	350	—	—	380	—	—	500	ps
		Total Jitter for Data Rate < 600Mbps	—	—	0.21	—	—	0.23	—	—	0.30	UI
	$t_{x \text{ Jitter}}$ -Emulated Differential I/O Standards with Three External Output Resistor Networks	Total Jitter for Data Rate < 640Mbps	—	—	500	—	—	500	—	—	500	ps
	$t_{x \text{ Jitter}}$ -Emulated Differential I/O Standards with One External Output Resistor Network	Total Jitter for Data Rate < 640Mbps	—	—	0.15	—	—	0.15	—	—	0.15	UI
	t_{DUTY}	TX output clock duty cycle for both True and	45	50	55	45	50	55	45	50	55	%

continued...

⁽⁶⁶⁾ The maximum ideal data rate is the SERDES factor (J) × PLL max output frequency (f_{out}), provided you can close the design timing and the signal integrity simulation is clean. You can estimate the achievable maximum data rate by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

⁽⁶⁷⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.



DLL Frequency Range Specifications

Table 35. DLL Frequency Range Specifications for Cyclone V Devices

Parameter	-C6	-C7, -I7	-C8	Unit
DLL operating frequency range	167 – 400	167 – 400	167 – 333	MHz

DQS Logic Block Specifications

Table 36. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Cyclone V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	-C6	-C7, -I7	-C8	Unit
2	40	80	80	ps

Memory Output Clock Jitter Specifications

Table 37. Memory Output Clock Jitter Specifications for Cyclone V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma.

Intel recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Parameter	Clock Network	Symbol	-C6		-C7, -I7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	-60	60	-70	70	-70	70	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	—	90	—	100	—	100	ps



Duty Cycle Distortion (DCD) Specifications

Table 39. Worst-Case DCD on Cyclone V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Symbol	-C6		-C7, -I7		-C8, -A7		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

HPS Specifications

This section provides HPS specifications and timing for Cyclone V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

HPS Clock Performance

Table 40. HPS Clock Performance for Cyclone V Devices

Symbol/Description	-C6	-C7, -I7	-A7	-C8	Unit
mpu_base_clk (microprocessor unit clock)	925	800	700	600	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	350	300	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	160	160	MHz

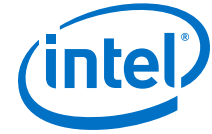
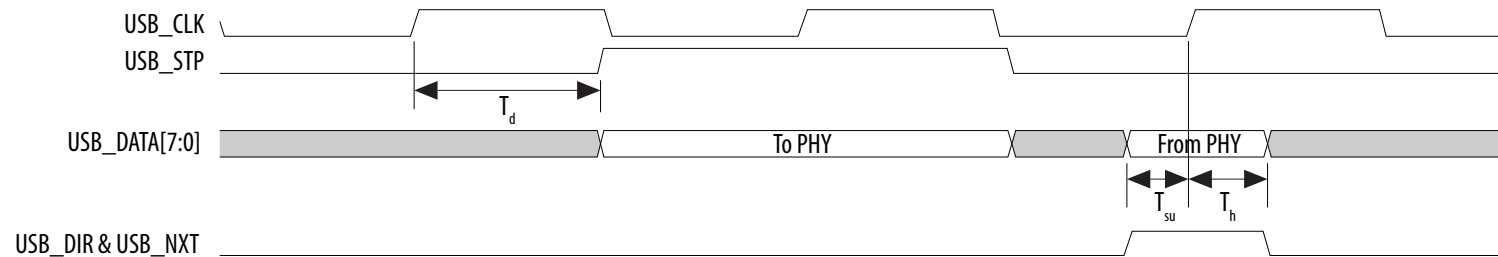


Figure 10. USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 48. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{duty cycle}$	TX_CLK duty cycle	45	—	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	-0.85	—	0.15	ns

Figure 11. RGMII TX Timing Diagram

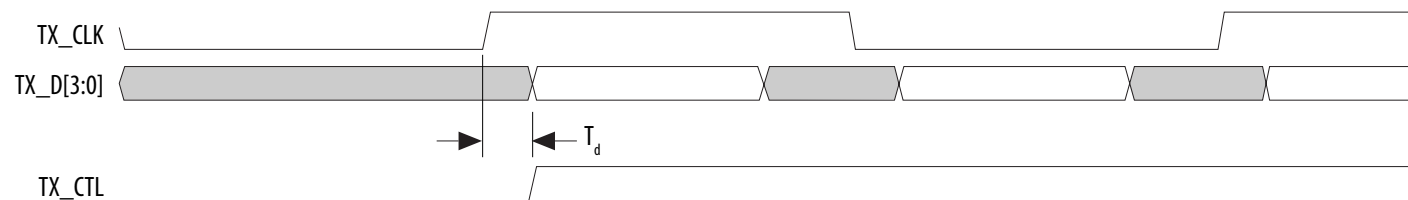
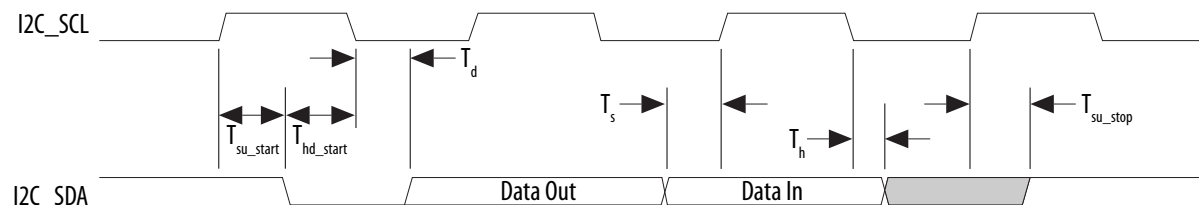


Figure 14. I²C Timing Diagram



NAND Timing Characteristics

Table 52. NAND ONFI 1.0 Timing Requirements for Cyclone V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
$T_{wp}^{(72)}$	Write enable pulse width	10	—	ns
$T_{wh}^{(72)}$	Write enable hold time	7	—	ns
$T_{rp}^{(72)}$	Read enable pulse width	10	—	ns
$T_{reh}^{(72)}$	Read enable hold time	7	—	ns
$T_{clesu}^{(72)}$	Command latch enable to write enable setup time	10	—	ns
$T_{cleh}^{(72)}$	Command latch enable to write enable hold time	5	—	ns
$T_{cesu}^{(72)}$	Chip enable to write enable setup time	15	—	ns
$T_{ceh}^{(72)}$	Chip enable to write enable hold time	5	—	ns
$T_{alesu}^{(72)}$	Address latch enable to write enable setup time	10	—	ns
$T_{aleh}^{(72)}$	Address latch enable to write enable hold time	5	—	ns
$T_{dsu}^{(72)}$	Data to write enable setup time	10	—	ns
$T_{dh}^{(72)}$	Data to write enable hold time	5	—	ns

continued...

⁽⁷²⁾ Timing of the NAND interface is controlled through the NAND configuration registers.

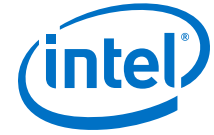
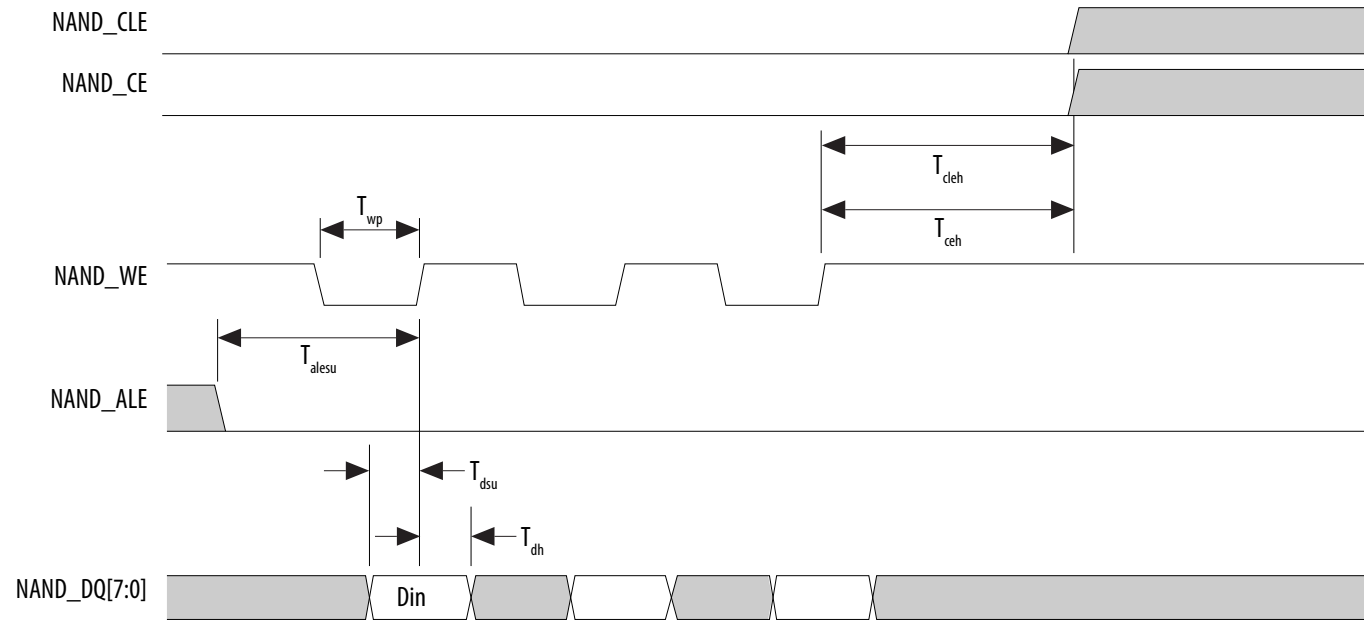
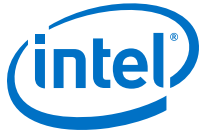


Figure 17. NAND Data Write Timing Diagram





POR Specifications

Table 55. Fast and Standard POR Delay Specification for Cyclone V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 ⁽⁷⁴⁾	ms
Standard	100	300	ms

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

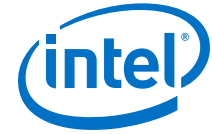
FPGA JTAG Configuration Timing

Table 56. FPGA JTAG Timing Parameters and Values for Cyclone V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30, 167 ⁽⁷⁵⁾	—	ns
t _{JCH}	TCK clock high time	14	—	ns
t _{JCL}	TCK clock low time	14	—	ns
t _{JPSU} (TDI)	TDI JTAG port setup time	1	—	ns
t _{JPSU} (TMS)	TMS JTAG port setup time	3	—	ns
t _{JPH}	JTAG port hold time	5	—	ns
<i>continued...</i>				

⁽⁷⁴⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

⁽⁷⁵⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.



Symbol	Parameter	Minimum	Maximum	Unit
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode ⁽⁹²⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.

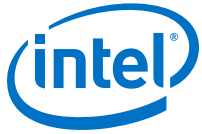
Initialization

Table 63. Initialization Clock Source Option and the Maximum Frequency for Cyclone V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T_{init}
CLKUSR ⁽⁹³⁾	PS and FPP	125	
	AS	100	
DCLK	PS and FPP	125	

⁽⁹²⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽⁹³⁾ To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Intel Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.



Date	Version	Changes
January 2015	2015.01.23	- Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps. Updated the note in the following tables: - Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices - Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices - Transceiver Compliance Specification for All Supported Protocol for Cyclone V Devices - Updated the description for $V_{CC_AUX_SHARED}$ to "HPS auxiliary power supply". Added a note to state that $V_{CC_AUX_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices. Updated in the following tables: - Absolute Maximum Ratings for Cyclone V Devices - HPS Power Supply Operating Conditions for Cyclone V SE, SX, and ST Devices - Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. - Updated the conditions for transceiver reference clock rise time and fall time: Measure at ± 60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification. - Updated f_{VCO} maximum value from 1400 MHz to 1600 MHz for -C7 and -I7 speed grades in the PLL specifications table. - Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. - Added the following notes in the High-Speed I/O Specifications for Cyclone V Devices table: - The Cyclone V devices support true RSDS output standard with data rates of up to 230 Mbps using true LVDS output buffer types on all I/O banks. - The Cyclone V devices support true mini-LVDS output standard with data rates of up to 340 Mbps using true LVDS output buffer types on all I/O banks. - Updated HPS Clock Performance main_base_clk specifications from 462 MHz to 400 MHz for -C6 speed grade. - Updated HPS PLL VCO maximum frequency to 1,600 MHz (for -C7, -I7, -A7, and -C8 speed grades) and 1,850 MHz (for -C6 speed grade). - Changed the symbol for HPS PLL input jitter divide value from NR to N. - Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables: - SPI Master Timing Requirements for Cyclone V Devices - SPI Slave Timing Requirements for Cyclone V Devices - Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board. - Added HPS JTAG timing specifications. - Updated the configuration .rbf size (bits) for Cyclone V devices. - Added a note to Uncompressed .rbf Sizes for Cyclone V Devices table: The recommended EPCQ serial configuration devices are able to store more than one image.
continued...		