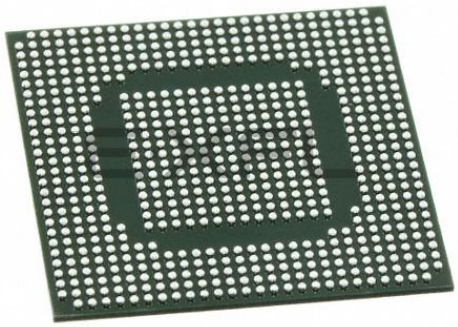

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Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-FBGA
Supplier Device Package	672-UBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba5u23i7n

Cyclone V Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Cyclone® V devices.

Cyclone V devices are offered in commercial and industrial grades. Commercial devices are offered in –C6 (fastest), –C7, and –C8 speed grades. Industrial grade devices are offered in the –I7 speed grade. Automotive devices are offered in the –A7 speed grade.

Cyclone V SoC devices are also offered in a low-power variant, as indicated by the L power option in the device part number. These devices have 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE. Note that the L power option devices are only available in –I7 speed grade, and have the equivalent operating conditions and timing specifications as the standard –I7 speed grade devices.

Table 1. Low Power Variants

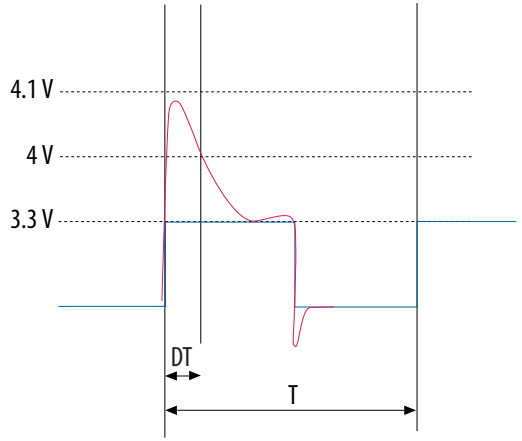
Density	Ordering Part Number (OPN)	Static Power Reduction
25K LE	5CSEBA2U19I7LN	30%
	5CSEBA2U23I7LN	
	5CSXFC2C6U23I7LN	
40K LE	5CSEBA4U19I7LN	
	5CSEBA4U23I7LN	
	5CSXFC4C6U23I7LN	
85K LE	5CSEBA5U19I7LN	20%
	5CSEBA5U23I7LN	
	5CSXC5C6U23I7LN	

continued...

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

For an overshoot of 3.8 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

Figure 1. Cyclone V Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Cyclone V devices.

Transceiver Power Supply Operating Conditions

Table 5. Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices

Symbol	Description	Minimum[8]	Typical	Maximum[8]	Unit
V_{CCH_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V_{CCE_GXBL}[9][10]	Transmitter and receiver power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V
V_{CCL_GXBL}[9][10]	Clock network power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V

Related Information

- PCIe Supported Configurations and Placement Guidelines
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.
- 6.144-Gbps Support Capability in Cyclone V GT Devices
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

(8) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which require full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

(10) Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

Table 9. OCT Calibration Accuracy Specifications for Cyclone V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–C6	–I7, –C7	–C8, –A7	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

Transceiver Performance Specifications

Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Table 21. Reference Clock Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL[31], HCSL, and LVDS										
Input frequency from REFCLK input pins[32]	—	27	—	550	27	—	550	27	—	550	MHz
Rise time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω

continued...

(30) Transceiver Speed Grade 5 covers specifications for Cyclone V GT and ST devices.

(31) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(32) The reference clock frequency must be ≥ 307.2 MHz to be fully compliance to CPRI transmit jitter specification at 6.144 Gbps. For more information about CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

(33) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

Table 22. Transceiver Clocks Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	100/125[37]	75	—	100/125[37]	75	—	100/125[37]	MHz

Table 23. Receiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS										
Data rate[38]	—	614	—	5000/6144[35]	614	—	3125	614	—	2500	Mbps
Absolute V_{MAX} for a receiver pin[39]	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	—	—	2.2	V

continued...

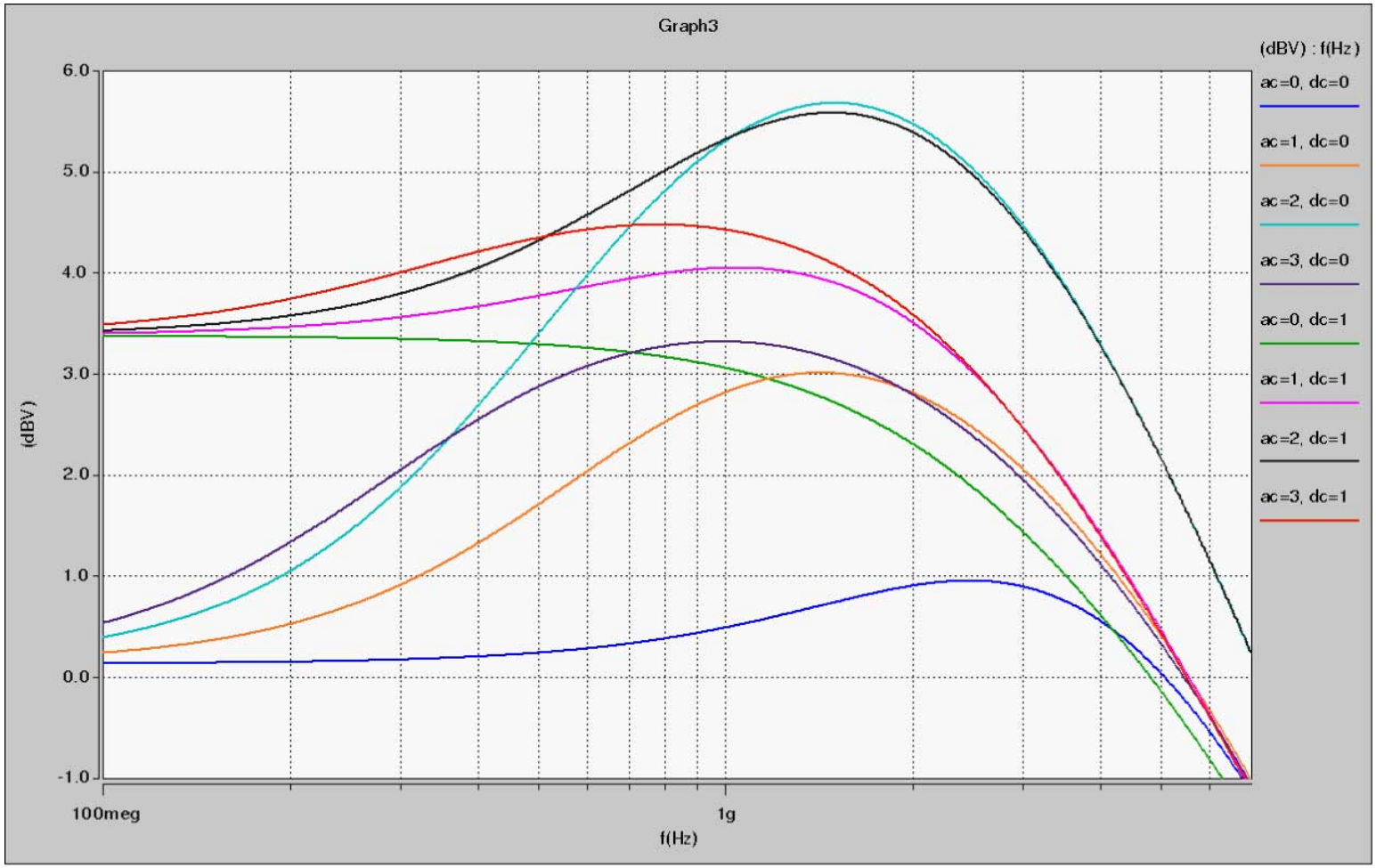
(37) The maximum supported clock frequency is 100 MHz if the PCIe hard IP block is enabled or 125 MHz if the PCIe hard IP block is not enabled.

(38) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

(39) The device cannot tolerate prolonged operation at this absolute maximum.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 4. CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices



Protocol	Sub-protocol	Data Rate (Mbps)
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII(51)	4,915.2
	CPRI E60LVII(51)	6,144
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970
VbyOne	VbyOne 3750	3,750
HiGig+	HIGIG 3750	3,750

Related Information

- PCIe Supported Configurations and Placement Guidelines
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.

(51) For CPRI E48LVII and E60LVII, Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144 Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		–C8, –A7 speed grades	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	–C6, –C7, –I7 speed grades	—	—	550(54)	MHz
		–C8, –A7 speed grades	—	—	460(54)	MHz
f_{OUT_EXT}	Output frequency for external clock output	–C6, –C7, –I7 speed grades	—	—	667(54)	MHz
		–C8, –A7 speed grades	—	—	533(54)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$t_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High(55)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps

continued...

(53) The VCO frequency reported by the Intel Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(54) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

(55) High bandwidth PLL settings are not supported in external feedback mode.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ}[56][57]	Input clock cycle-to-cycle jitter	F_{REF} ≥ 100 MHz	—	—	0.15	UI (p-p)
		F_{REF} < 100 MHz	—	—	±750	ps (p-p)
t_{OUTPJ_DC}[58]	Period jitter for dedicated clock output in integer PLL	F_{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F_{OUT} < 100 MHz	—	—	30	mUI (p-p)
t_{FOUTPJ_DC}[58]	Period jitter for dedicated clock output in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	425[61], 300[59]	ps (p-p)
		F_{OUT} < 100 MHz	—	—	42.5[61], 30[59]	mUI (p-p)
t_{OUTCCJ_DC}[58]	Cycle-to-cycle jitter for dedicated clock output in integer PLL	F_{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F_{OUT} < 100 MHz	—	—	30	mUI (p-p)
$t_{FOUTCCJ\_DC}$[58]	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	425[61], 300[59]	ps (p-p)
		F_{OUT} < 100 MHz	—	—	42.5[61], 30[59]	mUI (p-p)
t_{OUTPJ_IO}[58][60]	Period jitter for clock output on a regular I/O in integer PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
t_{FOUTPJ_IO}[58][60][61]	Period jitter for clock output on a regular I/O in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)

continued...

(56) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(57) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(58) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in *Memory Output Clock Jitter Specification for Cyclone V Devices* table.

(59) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

(60) External memory interface clock output jitter specifications use a different measurement method, which are available in *Memory Output Clock Jitter Specification for Cyclone V Devices* table.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
t_{OUTCCJ_IO}(58)(60)	Cycle-to-cycle jitter for clock output on regular I/O in integer PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
$t_{FOUTCCJ\_IO}$(58)(60)(61)	Cycle-to-cycle jitter for clock output on regular I/O in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$(58)(62)	Period jitter for dedicated clock output in cascaded PLLs	F_{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F_{OUT} < 100 MHz	—	—	30	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	Bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	f_{INPFD} = 100 MHz	390625	5.96	0.023	Hz

Related Information

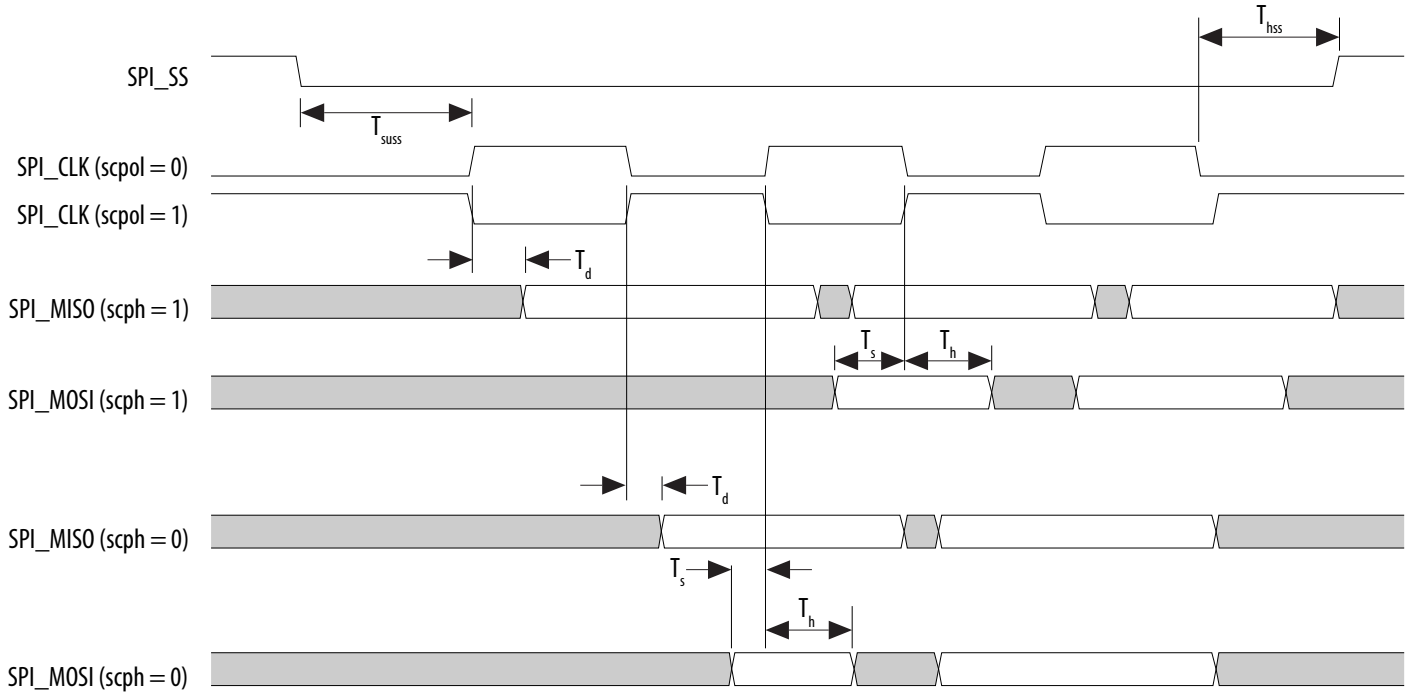
Memory Output Clock Jitter Specifications on page 49
Provides more information about the external memory interface clock output jitter specifications.

(61) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(62) The cascaded PLL specification is only applicable with the following conditions:
- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		Emulated Differential I/O Standards										
	t_{RISE} and t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
	TCCS	True Differential I/O Standards	—	—	200	—	—	250	—	—	250	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	300	—	—	300	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
Receiver	f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	875(67)	(65)	—	840(67)	(65)	—	640(67)	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
Sampling Window		—	—	—	350	—	—	350	—	—	350	ps

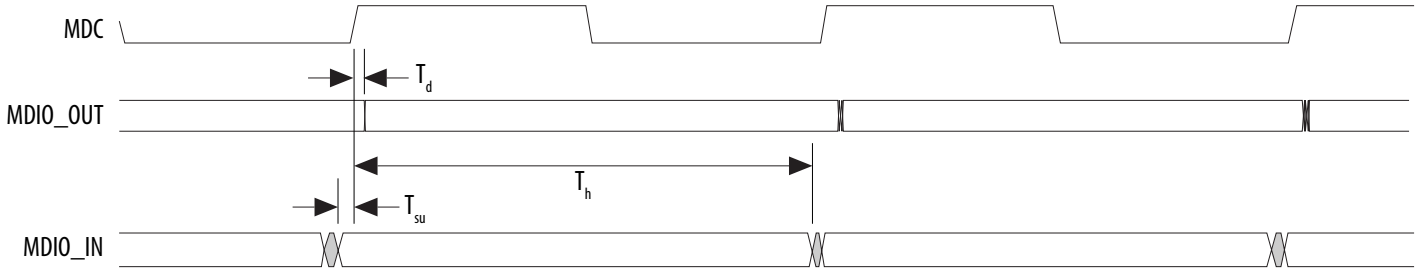
Figure 8. SPI Slave Timing Diagram



Related Information

SPI Controller, Cyclone V Hard Processor System Technical Reference Manual
Provides more information about `rx_sample_delay`.

Figure 13. MDIO Timing Diagram



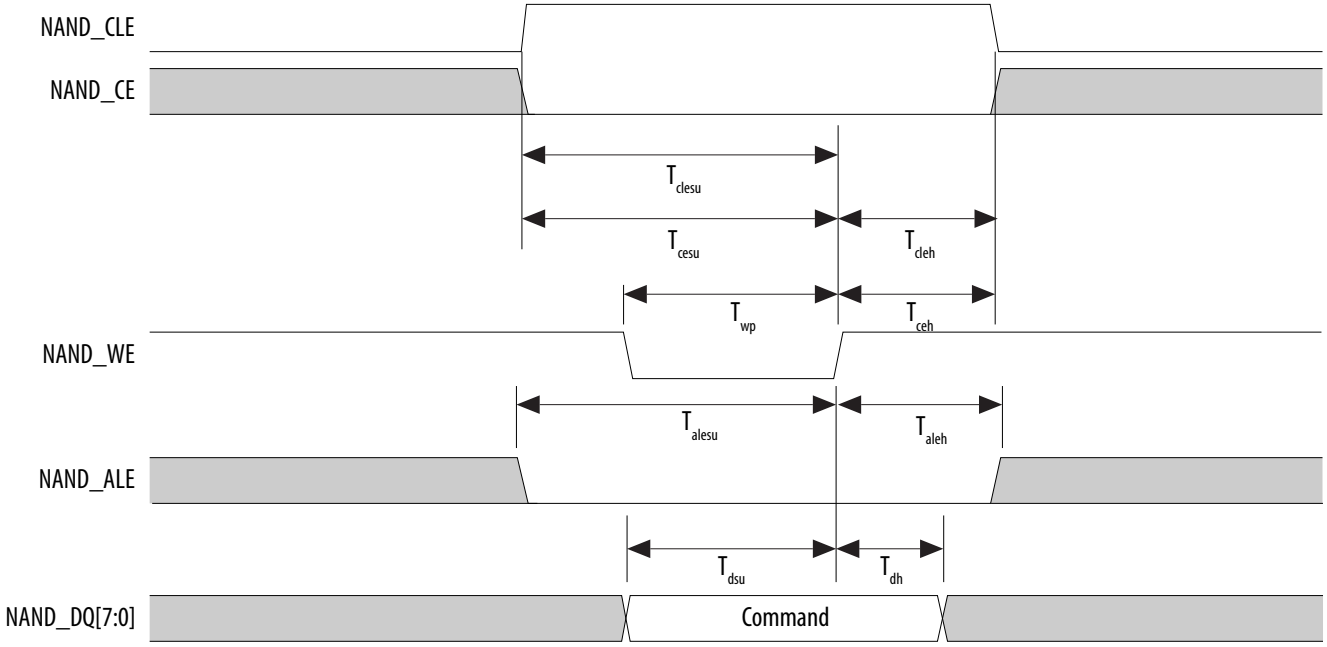
I²C Timing Characteristics

Table 51. I²C Timing Requirements for Cyclone V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

Symbol	Description	Min	Max	Unit
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Figure 15. NAND Command Latch Timing Diagram



Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Cyclone V Devices table.

Table 58. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(77)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(78)	µs
t_{CF2CK}(79)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(79)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × $1/f_{MAX}$	—	s

continued...

(77) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

(78) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(79) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Active Serial (AS) Configuration Timing

Table 60. AS Timing Parameters for AS ×1 and ×4 Configurations in Cyclone V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in *PS Timing Parameters for Cyclone V Devices* table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}[86]	Data hold time after the falling edge on DCLK	2.5[87]/2.9[88]	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

- Passive Serial (PS) Configuration Timing on page 74
- AS Configuration Timing
  Provides the AS configuration timing waveform.
- AN822: Intel FPGA Configuration Device Migration Guideline

(86) *Note:* To evaluate the data setup (t_{SU}) and data hold time (t_{DH}) slack on your board in order to ensure you are meeting the t_{SU} and t_{DH} requirement, you are recommended to follow the guideline in the "Evaluating Data Setup and Hold Timing Slack" chapter in *AN822: Intel FPGA Configuration Device Migration Guideline*.

(87) Specification for -6 speed grade

(88) Specification for -7 and -8 speed grade

Related Information

Configuration Files on page 76

Remote System Upgrades

Table 66. Remote System Upgrade Circuitry Timing Specifications for Cyclone V Devices

Parameter	Minimum	Unit
$t_{RU\_nCONFIG}$ (98)	250	ns
$t_{RU\_nRSTIMER}$ (99)	250	ns

Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about `reset_timer` (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 67. User Watchdog Internal Oscillator Frequency Specifications for Cyclone V Devices

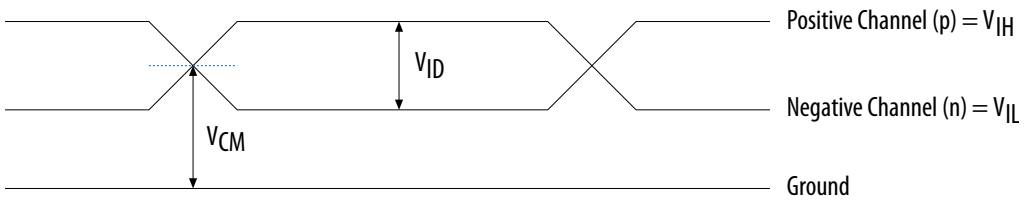
Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

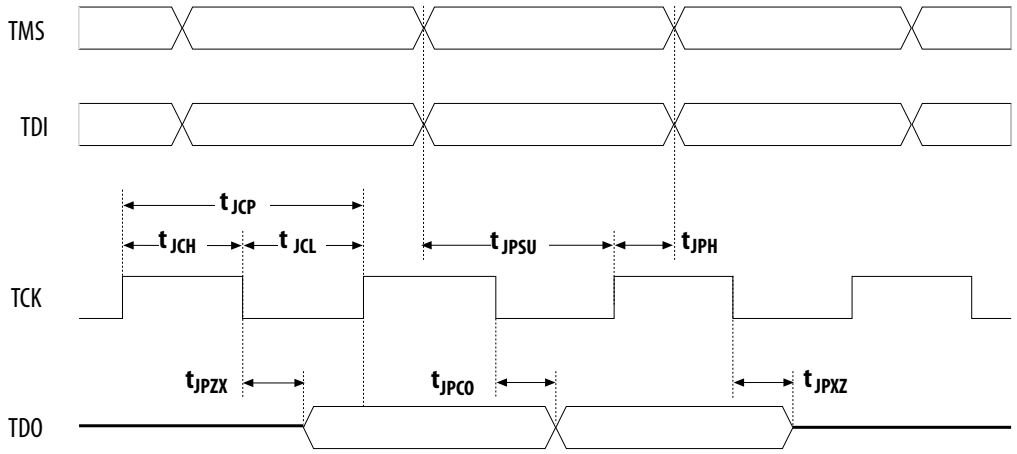
Intel offers two ways to determine I/O timing—the Excel-based I/O timing and the Intel Quartus Prime Timing Analyzer.

(98) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(99) This is equivalent to strobing the reset timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms

continued...

Term	Definition
	
PLL specifications	Diagram of PLL specifications

continued...