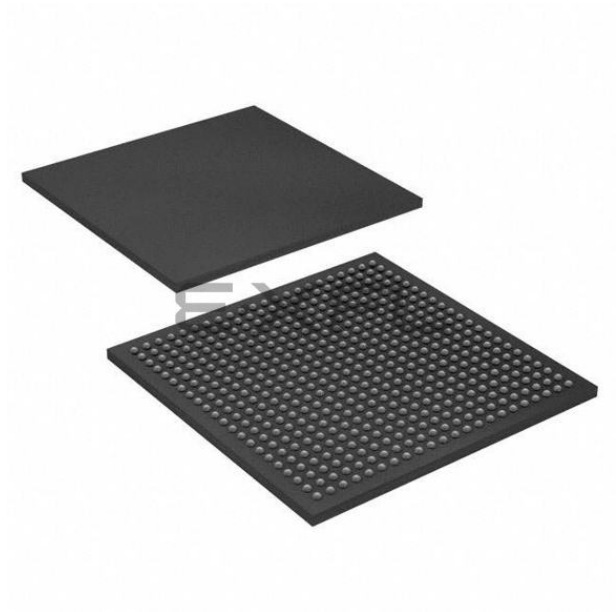

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 110K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-FBGA
Supplier Device Package	484-UBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cseba6u19i7n

Table 2. Absolute Maximum Ratings for Cyclone V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.5	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO}	I/O power supply	–0.5	3.90	V
V_{CCA_FPLL}	Phase-locked loop (PLL) analog power supply	–0.5	3.25	V
V_{CCH_GXB}	Transceiver high voltage power	–0.5	3.25	V
V_{CCE_GXB}	Transceiver power	–0.5	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.5	1.50	V
V_I	DC input voltage	–0.5	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.5	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.5	3.90	V
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.5	3.25	V
$V_{CC\_AUX\_SHARED}$ (1)	HPS auxiliary power supply	–0.5	3.25	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

(1) $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 3. Maximum Allowed Overshoot During Transitions for Cyclone V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%

continued...

OCT Without Calibration Resistance Tolerance Specifications

Table 10. OCT Without Calibration Resistance Tolerance Specifications for Cyclone V Devices

This table lists the Cyclone V OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			–C6	–I7, –C7	–C8, –A7	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8, 1.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5	±25	±40	±40	%

Figure 2. Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.

Differential SSTL I/O Standards

Table 18. Differential SSTL I/O Standards for Cyclone V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(20)	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	(20)	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$
SSTL-125	1.19	1.25	1.31	0.18	(20)	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 19. Differential HSTL and HSUL I/O Standards for Cyclone V Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.44	0.44

(20) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Transceiver Performance Specifications

Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Table 21. Reference Clock Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL[31], HCSL, and LVDS										
Input frequency from REFCLK input pins[32]	—	27	—	550	27	—	550	27	—	550	MHz
Rise time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω

continued...

(30) Transceiver Speed Grade 5 covers specifications for Cyclone V GT and ST devices.

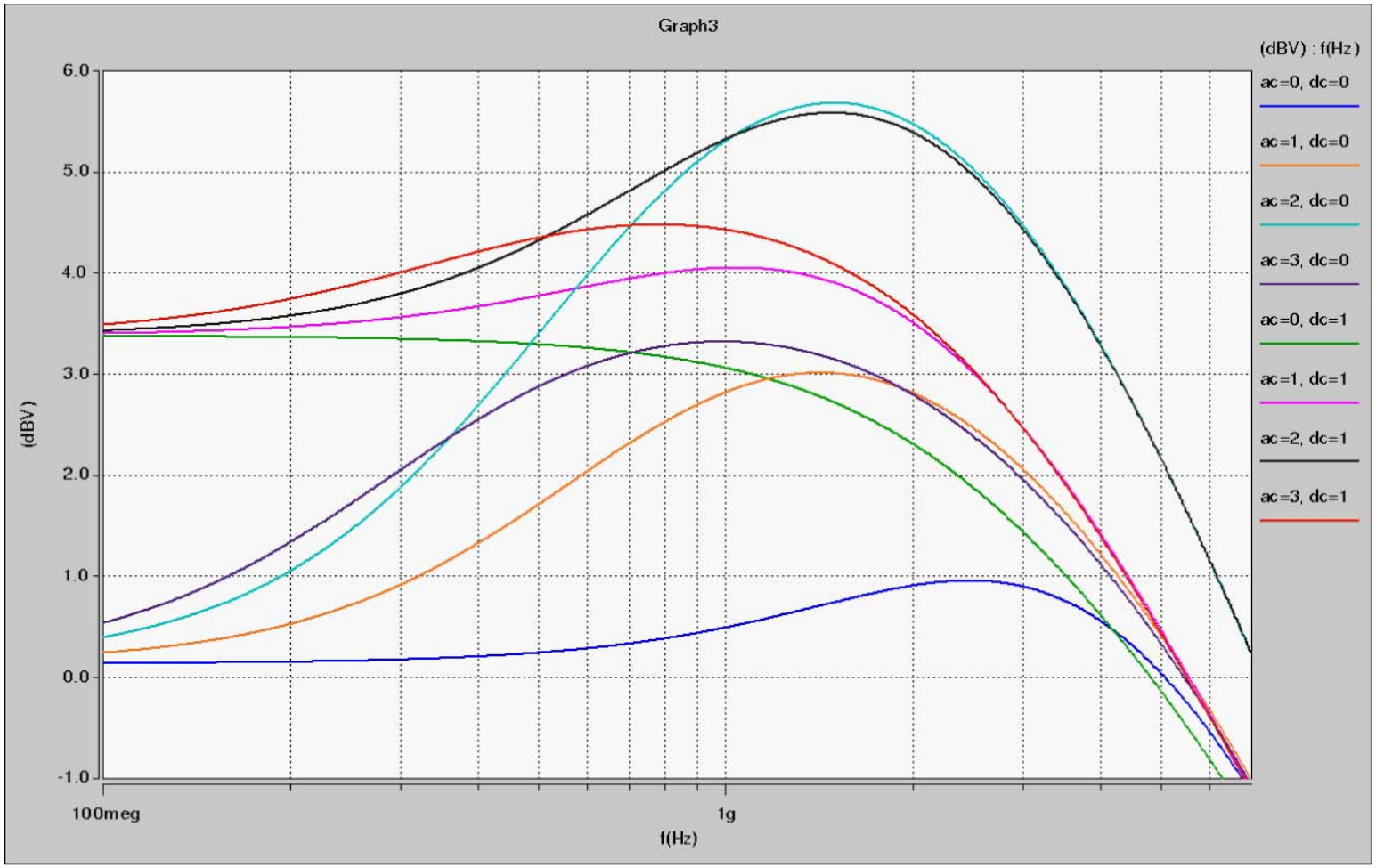
(31) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(32) The reference clock frequency must be ≥ 307.2 MHz to be fully compliance to CPRI transmit jitter specification at 6.144 Gbps. For more information about CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

(33) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 4. CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices



High-Speed I/O Specifications

Table 34. High-Speed I/O Specifications for Cyclone V Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The Cyclone V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	437.5	5	—	420	5	—	320	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	320	5	—	320	5	—	275	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	840	(65)	—	740	(65)	—	640	Mbps

continued...

(63) Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

(64) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(65) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
	Emulated Differential I/O Standards with Three External Output Resistor Networks- f_{HSDR} (data rate)(67)	SERDES factor J = 4 to 10	(65)	—	640	(65)	—	640	(65)	—	550	Mbps
	Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)	SERDES factor J = 4 to 10	(65)	—	170	(65)	—	170	(65)	—	170	Mbps
	$t_{x\ Jitter}$ -True Differential I/O Standards(67)	Total Jitterfor Data Rate, 600 Mbps – 840 Mbps	—	—	350	—	—	380	—	—	500	ps
		Total Jitter for Data Rate < 600Mbps	—	—	0.21	—	—	0.23	—	—	0.30	UI
	$t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Networks	Total Jitter for Data Rate < 640Mbps	—	—	500	—	—	500	—	—	500	ps
	$t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network	Total Jitter for Data Rate < 640Mbps	—	—	0.15	—	—	0.15	—	—	0.15	UI
	t_{DUTY}	TX output clock duty cycle for both True and	45	50	55	45	50	55	45	50	55	%

continued...

(66) The maximum ideal data rate is the SERDES factor (J) × PLL max output frequency (f_{out}), provided you can close the design timing and the signal integrity simulation is clean. You can estimate the achievable maximum data rate by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(67) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

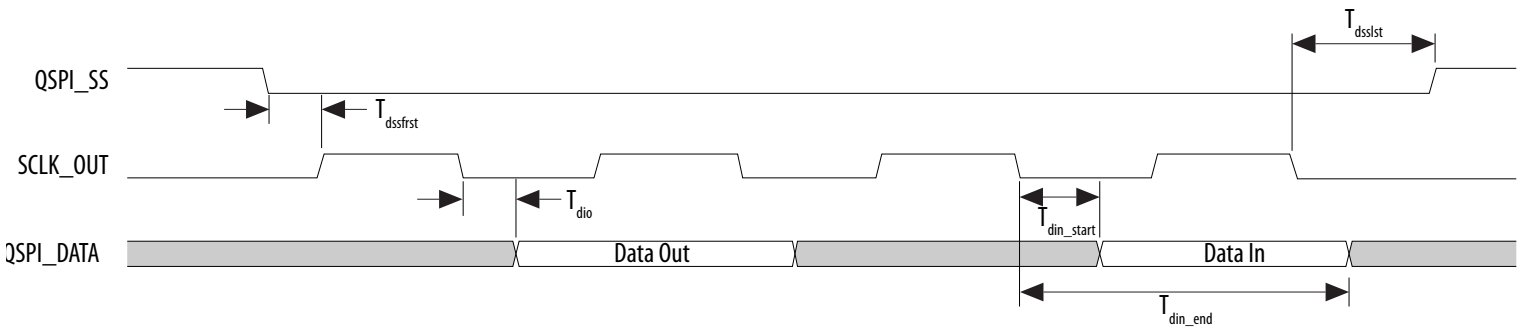
Quad SPI Flash Timing Characteristics

Table 43. Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (68)	ns
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (68)	—	—	ns

Figure 6. Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



(68) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Intel provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the *Quad SPI Flash Controller chapter in the Cyclone V Hard Processor System Technical Reference Manual*.

Figure 7. SPI Master Timing Diagram

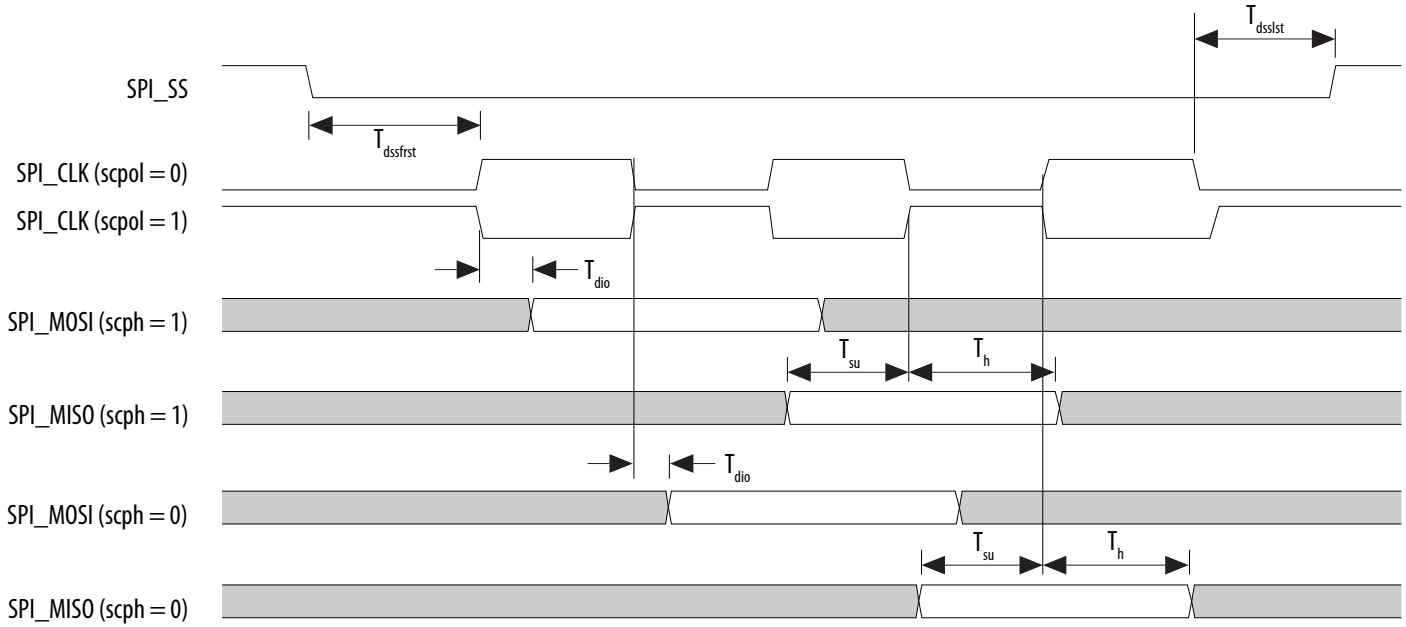


Table 45. SPI Slave Timing Requirements for Cyclone V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	20	—	ns
T_s	MOSI Setup time	5	—	ns
T_h	MOSI Hold time	5	—	ns
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	ns
T_d	MISO output delay	—	6	ns

SD/MMC Timing Characteristics

Table 46. Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices

After power up or cold reset, the Boot ROM uses `drvsel` = 3 and `smplsel` = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock SDMMC_CLK_OUT changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock SDMMC_CLK and the CSEL setting. The value of SDMMC_CLK is based on the external oscillator frequency and has a maximum value of 50 MHz.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smplsel` via the system manager. `drvsel` can be set from 1 to 7 and `smplsel` can be set from 0 to 7. While the preloader is executing, the values for SDMMC_CLK and SDMMC_CLK_OUT increase to a maximum of 200 MHz and 50 MHz respectively.

Symbol	Description	Min	Max	Unit
T_{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{sdmmc\_clk\_out}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
$T_{dutycycle}$	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	(T_{sdmmc_clk} × `drvsel`)/2 – 1.23 (70)	(T_{sdmmc_clk} × `drvsel`)/2 + 1.69 (70)	ns
T_{su}	Input setup time	1.05 – (T_{sdmmc_clk} × `smplsel`)/2 (71)	—	ns
T_h	Input hold time	(T_{sdmmc_clk} × `smplsel`)/2 (71)	—	ns

(70) `drvsel` is the drive clock phase shift select value.

(71) `smplsel` is the sample clock phase shift select value.

Symbol	Description	Min	Max	Unit
t_{JPCO}	JTAG port clock to output	—	11[76]	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14[76]	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14[76]	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Cyclone V devices use additional clock cycles to decrypt and decompress the configuration data. If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Cyclone V device.

Table 57. DCLK-to-DATA[] Ratio for Cyclone V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1

continued...

(76) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Cyclone V Devices table.

Table 58. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(77)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(78)	µs
t_{CF2CK}(79)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(79)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × $1/f_{MAX}$	—	s

continued...

(77) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

(78) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(79) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Variant	Member Code	Active Serial[96]			Fast Passive Parallel[97]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A9	4	100	257	16	125	51
Cyclone V GX	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Related Information

Configuration Files on page 76

Remote System Upgrades

Table 66. Remote System Upgrade Circuitry Timing Specifications for Cyclone V Devices

Parameter	Minimum	Unit
$t_{RU\_nCONFIG}$ (98)	250	ns
$t_{RU\_nRSTIMER}$ (99)	250	ns

Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about `reset_timer` (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 67. User Watchdog Internal Oscillator Frequency Specifications for Cyclone V Devices

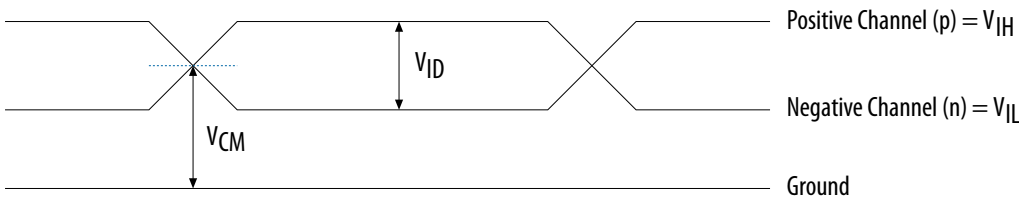
Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

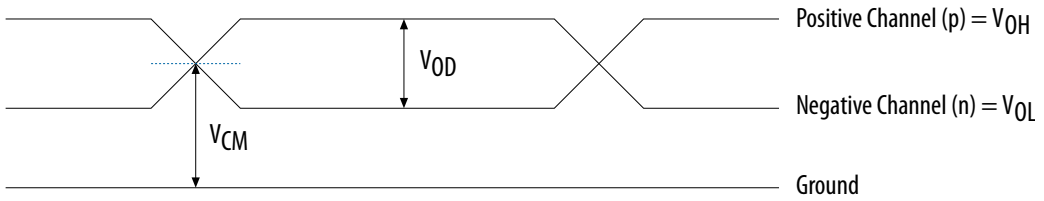
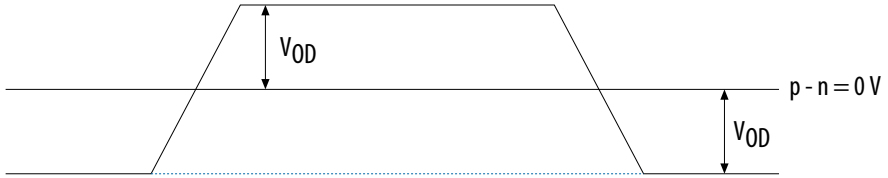
Intel offers two ways to determine I/O timing—the Excel-based I/O timing and the Intel Quartus Prime Timing Analyzer.

(98) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(99) This is equivalent to strobing the reset timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms

continued...

Term	Definition
	Single-Ended Waveform  **Differential Waveform** 
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} =1/TUI).
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG timing specifications	JTAG Timing Specifications

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Date	Version	Changes
December 2015	2015.12.04	• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices table. — Updated F_{clk}, $T_{dutycycle}$, and $T_{dssfrst}$ specifications. — Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications. — Removed T_{dinmax} specifications. • Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Cyclone V Devices table. • Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices table. — Updated T_{clk} to $T_{sdmmc\_clk\_out}$ symbol. — Updated $T_{sdmmc\_clk\_out}$ and T_d specifications. — Added T_{sdmmc_clk}, T_{su}, and T_h specifications. — Removed T_{dinmax} specifications. • Updated the following diagrams: — Quad SPI Flash Timing Diagram — SD/MMC Timing Diagram • Updated configuration .rbf sizes for Cyclone V devices. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Updated the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Cyclone V Devices table: — True RSDS output standard: data rates of up to 360 Mbps — True mini-LVDS output standard: data rates of up to 400 Mbps • Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash. • Updated T_h location in I^2C Timing Diagram. • Updated T_{wp} location in NAND Address Latch Timing Diagram. • Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Cyclone V Devices table. • Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Cyclone V Devices chapter. — FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1 — FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1 — AS Configuration Timing Waveform — PS Configuration Timing Waveform
March 2015	2015.03.31	• Added V_{CC} specifications for devices with internal scrubbing feature (with SC suffix) in Recommended Operating Conditions table. • Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices table.

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Date	Version	Changes
January 2015	2015.01.23	• Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps. Updated the note in the following tables: — Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices — Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices — Transceiver Compliance Specification for All Supported Protocol for Cyclone V Devices • Updated the description for $V_{CC\_AUX\_SHARED}$ to "HPS auxiliary power supply". Added a note to state that $V_{CC\_AUX\_SHARED}$ must be powered by the same source as VCC_AUX for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices. Updated in the following tables: — Absolute Maximum Ratings for Cyclone V Devices — HPS Power Supply Operating Conditions for Cyclone V SE, SX, and ST Devices • Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. • Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification. • Updated f_{VCO} maximum value from 1400 MHz to 1600 MHz for –C7 and –I7 speed grades in the PLL specifications table. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Added the following notes in the High-Speed I/O Specifications for Cyclone V Devices table: — The Cyclone V devices support true RSDS output standard with data rates of up to 230 Mbps using true LVDS output buffer types on all I/O banks. — The Cyclone V devices support true mini-LVDS output standard with data rates of up to 340 Mbps using true LVDS output buffer types on all I/O banks. • Updated HPS Clock Performance main_base_clk specifications from 462 MHz to 400 MHz for –C6 speed grade. • Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C7, –I7, –A7, and –C8 speed grades) and 1,850 MHz (for –C6 speed grade). • Changed the symbol for HPS PLL input jitter divide value from NR to N. • Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables: — SPI Master Timing Requirements for Cyclone V Devices — SPI Slave Timing Requirements for Cyclone V Devices • Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board. • Added HPS JTAG timing specifications. • Updated the configuration `.rbf` size (bits) for Cyclone V devices. • Added a note to Uncompressed .rbf Sizes for Cyclone V Devices table: The recommended EPCQ serial configuration devices are able to store more than one image.

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Date	Version	Changes
July 2014	3.9	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20. • Updated h2f_user2_clk specification for –C6, –C7, and –I7 speed grades in Table 34. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 35. • Updated T_d and T_h specifications in Table 41. • Added T_h specification in Table 43 and Figure 10. • Updated a note in Figure 17, Figure 18, and Figure 20 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 54. • Added DCLK device initialization clock source specification in Table 56. • Added description in "Configuration Files" section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature. • Added "Recommended EPCQ Serial Configuration Device" values in Table 57. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 59.
February 2014	3.8	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.7	• Updated Table 1, Table 3, Table 19, Table 20, Table 23, Table 25, Table 27, Table 34, Table 44, Table 51, Table 52, Table 55, and Table 61. • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 24, Table 25, Table 26, Table 27, Table 28, Table 32, Table 33, Table 49, Table 50, Table 51, Table 52, Table 53, Table 54, Table 55, Table 57, Table 58, Table 59, Table 60, and Table 62.
November 2013	3.6	Updated Table 23, Table 30, and Table 31.
October 2013	3.5	• Added "HPS PLL Specifications". • Added Table 23, Table 35, and Table 36. • Updated Table 1, Table 5, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, Table 28, Table 34, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, and Table 53. • Updated Figure 1, Figure 2, Figure 4, Figure 10, Figure 12, Figure 13, and Figure 16. • Removed table: GPIO Pulse Width for Cyclone V Devices.

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