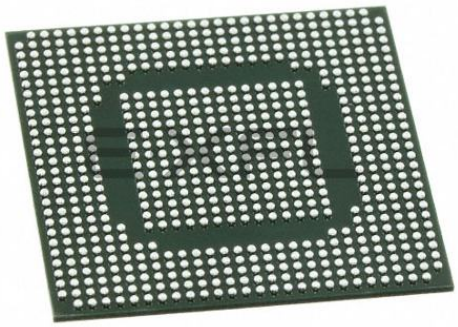

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 64KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 800MHz |
| Primary Attributes | FPGA - 110K Logic Elements |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 672-FBGA |
| Supplier Device Package | 672-UBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5cseba6u23i7n |

# Contents

| Density | Ordering Part Number (OPN) | Static Power Reduction |
|---|---|---|
| 110K LE | 5CSEBA6U19I7LN | |
| | 5CSEBA6U23I7LN | |
| | 5CSXFC6C6U23I7LN | |

To estimate total power consumption for a low-power device, listed in Table 1 on page 3:

1. Multiply the Total Static Power reported by the Early Power Estimator (EPE) by the appropriate scale factor:
   - For 25K LE and 40K LE devices, use 0.7
   - For 85K LE and 110K LE devices, use 0.8
2. Add the result from Step 1 on page 4 to the Total Dynamic Power reported by the EPE.

**Related Information**

Cyclone V Device Overview
Provides more information about the densities and packages of devices in the Cyclone V family.

# Electrical Characteristics

The following sections describe the operating conditions and power consumption of Cyclone V devices.

## Operating Conditions

Cyclone V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Cyclone V devices, you must consider the operating requirements described in this section.

### Absolute Maximum Ratings

This section defines the maximum operating conditions for Cyclone V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

***Caution:*** Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | — | — | — |

## Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

### Table 17. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Cyclone V Devices

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$[19] (mA) | $I_{OH}$[19] (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |

*continued...*

(19) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

| Symbol/Description | Condition | Transceiver Speed Grade 5[30] | | | Transceiver Speed Grade 6 | | | Transceiver Speed Grade 7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Minimum differential eye opening at the receiver serial input pins[40] | — | 110 | — | — | 110 | — | — | 110 | — | — | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | — | 85 | — | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | — | 100 | — | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | — | 120 | — | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | — | 150 | — | — | 150 | — | Ω |
| $V_{ICM}$ (AC coupled) | 2.5 V PCML, LVPECL, and LVDS | $V_{CCE\_GXBL}$ supply[34][35] | | | $V_{CCE\_GXBL}$ supply | | | $V_{CCE\_GXBL}$ supply | | | V |
| | 1.5 V PCML | 0.65/0.75/0.8 [41] | | | | | | | | | V |
| $t_{LTR}$[42] | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$[43] | — | — | — | 4 | — | — | 4 | — | — | 4 | µs |
| $t_{LTD\_manual}$[44] | — | — | — | 4 | — | — | 4 | — | — | 4 | µs |
| $t_{LTR\_LTD\_manual}$[45] | — | 15 | — | — | 15 | — | — | 15 | — | — | µs |

continued...

(40) The differential eye opening specification at the receiver input pins assumes that you have disabled the Receiver Equalization feature. If you enable the Receiver Equalization feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(41) The AC coupled $V_{ICM}$ = 650 mV for Cyclone V GX and SX in PCIe mode only. The AC coupled $V_{ICM}$ = 750mV for Cyclone V GT and ST in PCIe mode only.

(42) $t_{LTR}$ is the time required for the receive clock data recovery (CDR) to lock to the input reference clock frequency after coming out of reset.

(43) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(44) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

| Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting | Intel Quartus Prime $V_{OD}$ Setting | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 11 | — | 10.2 | 6.09 | 5.01 | 4.23 | 3.61 | — | dB |
| 12 | — | 11.56 | 6.74 | 5.51 | 4.68 | 3.97 | — | dB |
| 13 | — | 12.9 | 7.44 | 6.1 | 5.12 | 4.36 | — | dB |
| 14 | — | 14.44 | 8.12 | 6.64 | 5.57 | 4.76 | — | dB |
| 15 | — | — | 8.87 | 7.21 | 6.06 | 5.14 | — | dB |
| 16 | — | — | 9.56 | 7.73 | 6.49 | — | — | dB |
| 17 | — | — | 10.43 | 8.39 | 7.02 | — | — | dB |
| 18 | — | — | 11.23 | 9.03 | 7.52 | — | — | dB |
| 19 | — | — | 12.18 | 9.7 | 8.02 | — | — | dB |
| 20 | — | — | 13.17 | 10.34 | 8.59 | — | — | dB |
| 21 | — | — | 14.2 | 11.1 | — | — | — | dB |
| 22 | — | — | 15.38 | 11.87 | — | — | — | dB |
| 23 | — | — | — | 12.67 | — | — | — | dB |
| 24 | — | — | — | 13.48 | — | — | — | dB |
| 25 | — | — | — | 14.37 | — | — | — | dB |
| 26 | — | — | — | — | — | — | — | dB |
| 27 | — | — | — | — | — | — | — | dB |
| 28 | — | — | — | — | — | — | — | dB |
| 29 | — | — | — | — | — | — | — | dB |
| 30 | — | — | — | — | — | — | — | dB |
| 31 | — | — | — | — | — | — | — | dB |

## Related Information

SPICE Models for Intel Devices
Provides the Cyclone V HSSI HSPICE models.

## Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Cyclone V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Intel Sales Representative.

**Table 29. Transceiver Compliance Specification for All Supported Protocol for Cyclone V GX, GT, SX, and ST Devices**

| Protocol | Sub-protocol | Data Rate (Mbps) |
|---|---|---|
| PCIe | PCIe Gen1 | 2,500 |
| | PCIe Gen2(50) | 5,000 |
| | PCIe Cable | 2,500 |
| XAUI | XAUI 2135 | 3,125 |
| Serial RapidIO® (SRIO) | SRIO 1250 SR | 1,250 |
| | SRIO 1250 LR | 1,250 |
| | SRIO 2500 SR | 2,500 |
| | SRIO 2500 LR | 2,500 |
| | SRIO 3125 SR | 3,125 |
| | SRIO 3125 LR | 3,125 |
| | SRIO 5000 SR | 5,000 |
| | SRIO 5000 MR | 5,000 |
| | SRIO 5000 LR | 5,000 |
| Common Public Radio Interface (CPRI) | CPRI E6LV | 614.4 |
| | CPRI E6HV | 614.4 |
| | CPRI E6LVII | 614.4 |

*continued...*

(50) For PCIe Gen2 sub-protocol, Intel recommends increasing the $V_{CCE\_GXBL}$ and $V_{CCL\_GXBL}$ typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which ensure full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

- 6.144-Gbps Support Capability in Cyclone V GT Devices
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

# Core Performance Specifications

## Clock Tree Specifications

### Table 30. Clock Tree Specifications for Cyclone V Devices

| Parameter | Performance | | | Unit |
|---|---|---|---|---|
| | –C6 | –C7, –I7 | –C8, –A7 | |
| Global clock and Regional clock | 550 | 550 | 460 | MHz |
| Peripheral clock | 155 | 155 | 155 | MHz |

## PLL Specifications

### Table 31. PLL Specifications for Cyclone V Devices

This table lists the Cyclone V PLL block specifications. Cyclone V PLL block does not include HPS PLL.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | –C6 speed grade | 5 | — | 670(52) | MHz |
| | | –C7, –I7 speed grades | 5 | — | 622(52) | MHz |
| | | –C8, –A7 speed grades | 5 | — | 500(52) | MHz |
| $f_{INPFD}$ | Integer input clock frequency to the phase frequency detector (PFD) | — | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional input clock frequency to the PFD | — | 50 | — | 160 | MHz |
| $f_{VCO}$(53) | PLL voltage-controlled oscillator (VCO) operating range | –C6, –C7, –I7 speed grades | 600 | — | 1600 | MHz |

continued...

(52) This specification is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

| Memory | Mode | Resources Used | | Performance | | | Unit |
|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | –C6 | –C7, –I7 | –C8, –A7 | |
| | ROM, all supported width | 0 | 1 | 420 | 350 | 300 | MHz |
| M10K Block | Single-port, all supported widths | 0 | 1 | 315 | 275 | 240 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 315 | 275 | 240 | MHz |
| | Simple dual-port with the **read-during-write** option set to **Old Data**, all supported widths | 0 | 1 | 275 | 240 | 180 | MHz |
| | True dual port, all supported widths | 0 | 1 | 315 | 275 | 240 | MHz |
| | ROM, all supported widths | 0 | 1 | 315 | 275 | 240 | MHz |

## Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

| Symbol | | Condition | –C6 | | | –C7, –I7 | | | –C8, –A7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | SERDES factor J = 1 to 2, uses DDR registers | (65) | — | (66) | (65) | — | (66) | (65) | — | (66) | Mbps |
| | Emulated Differential I/O Standards with Three External Output Resistor Networks- $f_{HSDR}$ (data rate)(67) | SERDES factor J = 4 to 10 | (65) | — | 640 | (65) | — | 640 | (65) | — | 550 | Mbps |
| | Emulated Differential I/O Standards with One External Output Resistor Network - $f_{HSDR}$ (data rate) | SERDES factor J = 4 to 10 | (65) | — | 170 | (65) | — | 170 | (65) | — | 170 | Mbps |
| | $t_{x\ Jitter}$ -True Differential I/O Standards(67) | Total Jitterfor Data Rate, 600 Mbps – 840 Mbps | — | — | 350 | — | — | 380 | — | — | 500 | ps |
| | | Total Jitter for Data Rate < 600Mbps | — | — | 0.21 | — | — | 0.23 | — | — | 0.30 | UI |
| | $t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Networks | Total Jitter for Data Rate < 640Mbps | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| | $t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network | Total Jitter for Data Rate < 640Mbps | — | — | 0.15 | — | — | 0.15 | — | — | 0.15 | UI |
| | $t_{DUTY}$ | TX output clock duty cycle for both True and | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |

***continued...***

(66) The maximum ideal data rate is the SERDES factor (J) × PLL max output frequency ($f_{out}$), provided you can close the design timing and the signal integrity simulation is clean. You can estimate the achievable maximum data rate by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

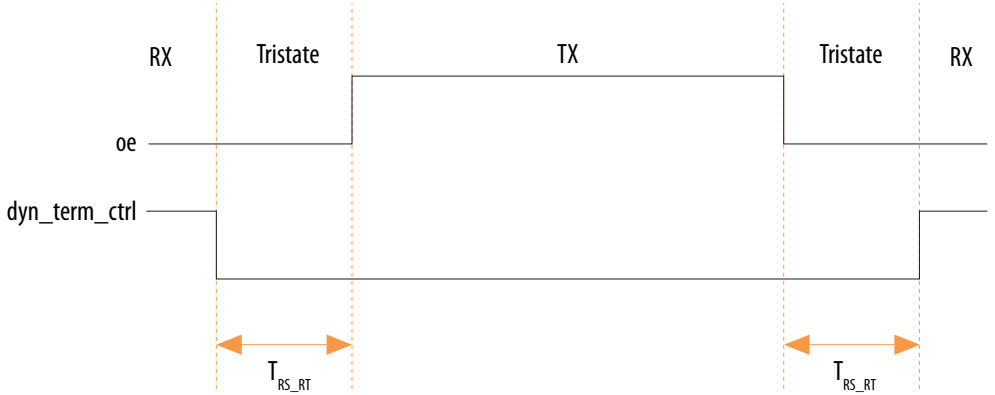
(67) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

## OCT Calibration Block Specifications

### Table 38. OCT Calibration Block Specifications for Cyclone V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for $R_S$ OCT/$R_T$ OCT calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS\_RT}$ | Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between $R_S$ OCT and $R_T$ OCT | — | 2.5 | — | ns |

### Figure 5. Timing Diagram for oe and dyn_term_ctrl Signals



## Duty Cycle Distortion (DCD) Specifications

### Table 39. Worst-Case DCD on Cyclone V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

| Symbol | –C6 | | –C7, –I7 | | –C8, –A7 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

## HPS Specifications

This section provides HPS specifications and timing for Cyclone V devices.

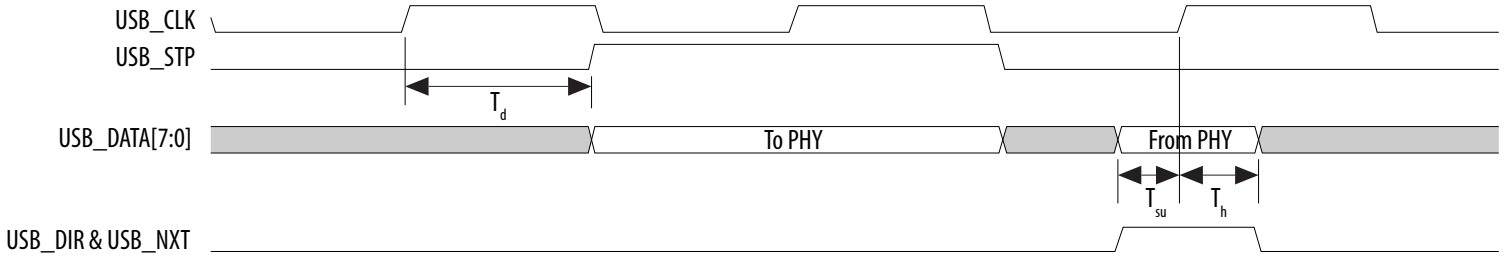
For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

## HPS Clock Performance

### Table 40. HPS Clock Performance for Cyclone V Devices

| Symbol/Description | –C6 | –C7, –I7 | –A7 | –C8 | Unit |
|---|---|---|---|---|---|
| mpu_base_clk (microprocessor unit clock) | 925 | 800 | 700 | 600 | MHz |
| main_base_clk (L3/L4 interconnect clock) | 400 | 400 | 350 | 300 | MHz |
| h2f_user0_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user1_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user2_clk | 200 | 200 | 160 | 160 | MHz |

**Figure 10. USB Timing Diagram**

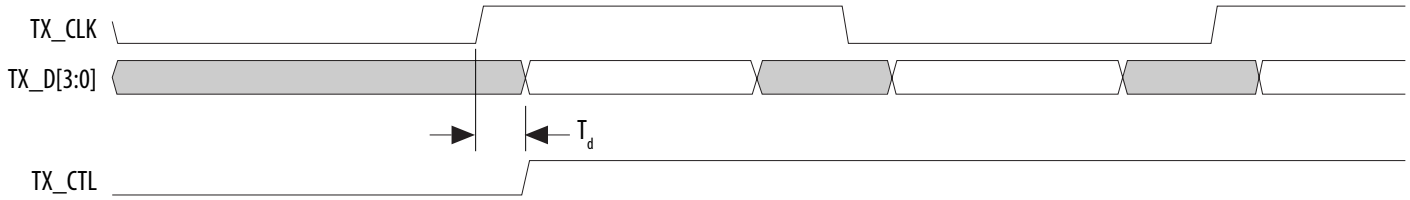



## Ethernet Media Access Controller (EMAC) Timing Characteristics

**Table 48. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Cyclone V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | TX_CLK clock period | — | 8 | — | ns |
| $T_{clk}$ (100Base-T) | TX_CLK clock period | — | 40 | — | ns |
| $T_{clk}$ (10Base-T) | TX_CLK clock period | — | 400 | — | ns |
| $T_{dutycycle}$ | TX_CLK duty cycle | 45 | — | 55 | % |
| $T_d$ | TX_CLK to TXD/TX_CTL output data delay | –0.85 | — | 0.15 | ns |

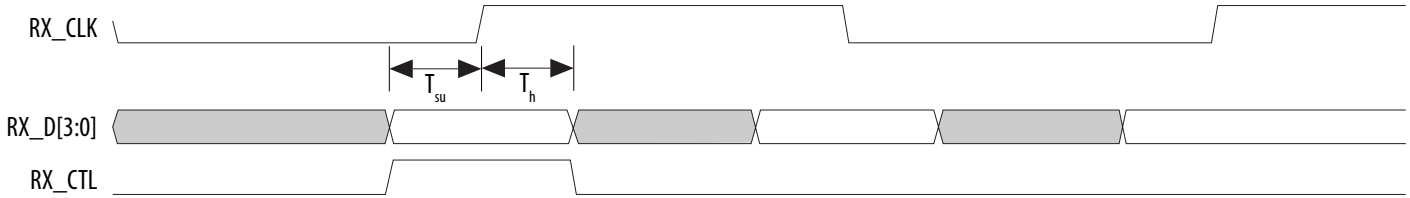
**Figure 11. RGMII TX Timing Diagram**



## Table 49. RGMII RX Timing Requirements for Cyclone V Devices

| Symbol | Description | Min | Typ | Unit |
|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | RX_CLK clock period | — | 8 | ns |
| $T_{clk}$ (100Base-T) | RX_CLK clock period | — | 40 | ns |
| $T_{clk}$ (10Base-T) | RX_CLK clock period | — | 400 | ns |
| $T_{su}$ | RX_D/RX_CTL setup time | 1 | — | ns |
| $T_h$ | RX_D/RX_CTL hold time | 1 | — | ns |

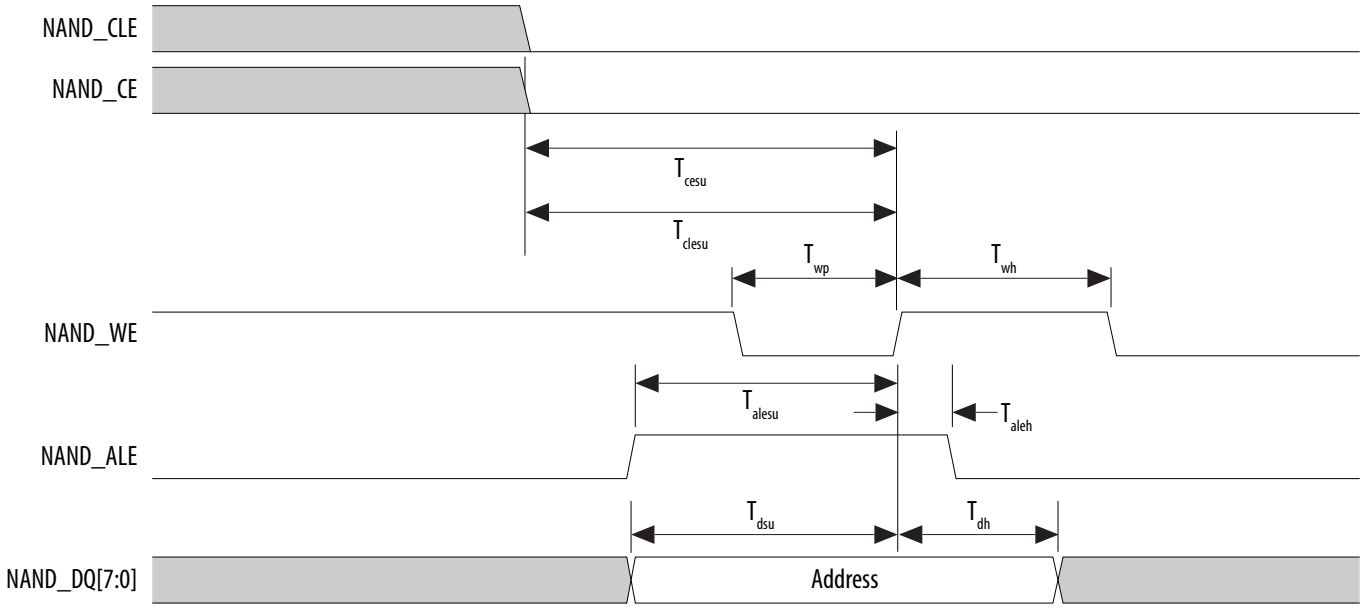
## Figure 12. RGMII RX Timing Diagram




## Table 50. Management Data Input/Output (MDIO) Timing Requirements for Cyclone V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | MDC clock period | — | 400 | — | ns |
| $T_d$ | MDC to MDIO output data delay | 10 | — | 20 | ns |
| $T_s$ | Setup time for MDIO data | 10 | — | — | ns |
| $T_h$ | Hold time for MDIO data | 0 | — | — | ns |

**Figure 16. NAND Address Latch Timing Diagram**



| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode(92) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + ($T_{init}$ × CLKUSR period) | — | — |
| $T_{init}$ | Number of clock cycles required for device initialization | 8,576 | — | Cycles |

### Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

## Initialization

### Table 63. Initialization Clock Source Option and the Maximum Frequency for Cyclone V Devices

| Initialization Clock Source | Configuration Scheme | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|---|---|---|---|
| Internal Oscillator | AS, PS, and FPP | 12.5 | $T_{init}$ |
| CLKUSR(93) | PS and FPP | 125 | |
| | AS | 100 | |
| DCLK | PS and FPP | 125 | |

(92) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(93) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Intel Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

| Variant | Member Code | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) | Recommended EPCQ Serial Configuration Device(94) |
|---|---|---|---|---|
| | A4 | 33,958,560 | 322,072 | EPCQ128 |
| | A5 | 56,057,632 | 324,888 | EPCQ128 |
| | A6 | 56,057,632 | 324,888 | EPCQ128 |
| Cyclone V SX | C2 | 33,958,560 | 322,072 | EPCQ128 |
| | C4 | 33,958,560 | 322,072 | EPCQ128 |
| | C5 | 56,057,632 | 324,888 | EPCQ128 |
| | C6 | 56,057,632 | 324,888 | EPCQ128 |
| Cyclone V ST | D5 | 56,057,632 | 324,888 | EPCQ128 |
| | D6 | 56,057,632 | 324,888 | EPCQ128 |

## Minimum Configuration Time Estimation

### Table 65. Minimum Configuration Time Estimation for Cyclone V Devices

The estimated values are based on the configuration `.rbf` sizes in *Uncompressed .rbf Sizes for Cyclone V Devices* table.

| Variant | Member Code | Active Serial(96) | | | Fast Passive Parallel(97) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Minimum Configuration Time (ms) | Width | DCLK (MHz) | Minimum Configuration Time (ms) |
| Cyclone V E | A2 | 4 | 100 | 53 | 16 | 125 | 11 |
| | A4 | 4 | 100 | 53 | 16 | 125 | 11 |
| | A5 | 4 | 100 | 85 | 16 | 125 | 17 |
| | A7 | 4 | 100 | 140 | 16 | 125 | 28 |

*continued...*

(94) The recommended EPCQ serial configuration devices are able to store more than one image.

(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

### Related Information

Configuration Files on page 76

## Remote System Upgrades

### Table 66. Remote System Upgrade Circuitry Timing Specifications for Cyclone V Devices

| Parameter | Minimum | Unit |
|---|---|---|
| $t_{RU\_nCONFIG}$ (98) | 250 | ns |
| $t_{RU\_nRSTIMER}$ (99) | 250 | ns |

### Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about `reset_timer` (RU_nRSTIMER) signal.

## User Watchdog Internal Oscillator Frequency Specifications

### Table 67. User Watchdog Internal Oscillator Frequency Specifications for Cyclone V Devices

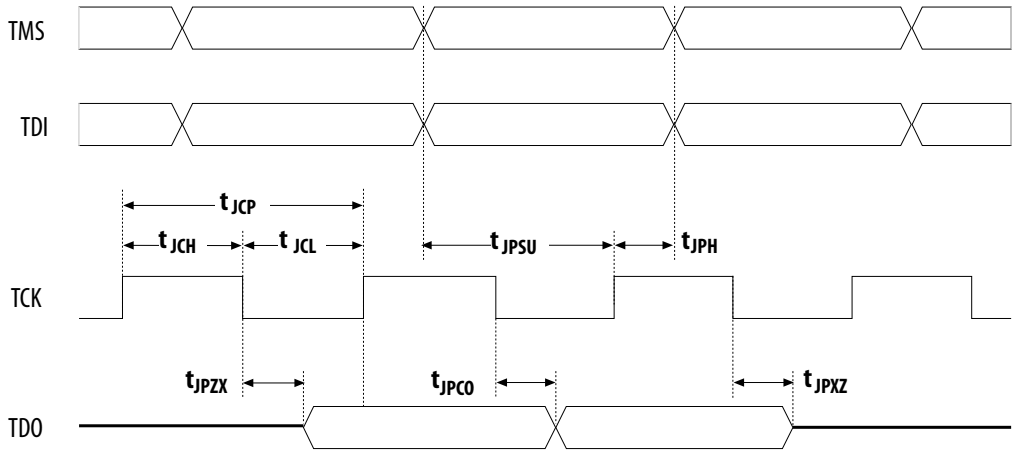
| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| User watchdog internal oscillator frequency | 5.3 | 7.9 | 12.5 | MHz |

## I/O Timing

Intel offers two ways to determine I/O timing—the Excel-based I/O timing and the Intel Quartus Prime Timing Analyzer.

(98) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(99) This is equivalent to strobing the reset timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

| Term | Definition |
|---|---|
| |  |
| PLL specifications | Diagram of PLL specifications |

*continued...*

| Date | Version | Changes |
|---|---|---|
| January 2015 | 2015.01.23 | • Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps. Updated the note in the following tables:<br>— Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices<br>— Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices<br>— Transceiver Compliance Specification for All Supported Protocol for Cyclone V Devices<br>• Updated the description for $V_{CC\_AUX\_SHARED}$ to "HPS auxiliary power supply". Added a note to state that $V_{CC\_AUX\_SHARED}$ must be powered by the same source as VCC_AUX for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices. Updated in the following tables:<br>— Absolute Maximum Ratings for Cyclone V Devices<br>— HPS Power Supply Operating Conditions for Cyclone V SE, SX, and ST Devices<br>• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.<br>• Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification.<br>• Updated $f_{VCO}$ maximum value from 1400 MHz to 1600 MHz for –C7 and –I7 speed grades in the PLL specifications table.<br>• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.<br>• Added the following notes in the High-Speed I/O Specifications for Cyclone V Devices table:<br>— The Cyclone V devices support true RSDS output standard with data rates of up to 230 Mbps using true LVDS output buffer types on all I/O banks.<br>— The Cyclone V devices support true mini-LVDS output standard with data rates of up to 340 Mbps using true LVDS output buffer types on all I/O banks.<br>• Updated HPS Clock Performance main_base_clk specifications from 462 MHz to 400 MHz for –C6 speed grade.<br>• Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C7, –I7, –A7, and –C8 speed grades) and 1,850 MHz (for –C6 speed grade).<br>• Changed the symbol for HPS PLL input jitter divide value from NR to N.<br>• Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables:<br>— SPI Master Timing Requirements for Cyclone V Devices<br>— SPI Slave Timing Requirements for Cyclone V Devices<br>• Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.<br>• Added HPS JTAG timing specifications.<br>• Updated the configuration `.rbf` size (bits) for Cyclone V devices.<br>• Added a note to Uncompressed .rbf Sizes for Cyclone V Devices table: The recommended EPCQ serial configuration devices are able to store more than one image. |

***continued...***

| Date | Version | Changes |
|---|---|---|
| February 2012 | 1.2 | • Added automotive speed grade information.<br>• Added Figure 2–1.<br>• Updated Table 2–3, Table 2–8, Table 2–9, Table 2–19, Table 2–20, Table 2–21, Table 2–22, Table 2–23, Table 2–24, Table 2–25, Table 2–26, Table 2–27, Table 2–28, Table 2–30, Table 2–35, and Table 2–43.<br>• Minor text edits. |
| November 2011 | 1.1 | • Added Table 2–5.<br>• Updated Table 2–3, Table 2–4, Table 2–11, Table 2–13, Table 2–20, and Table 2–21. |
| October 2011 | 1.0 | Initial release. |