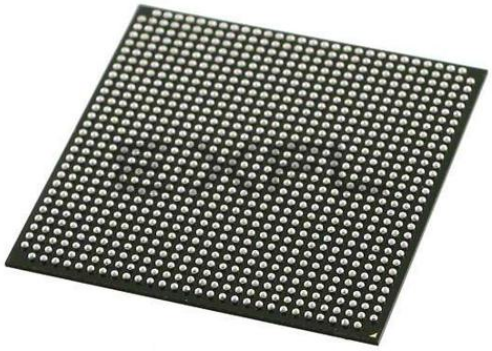

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csema5f31c8n

Contents

Table 9. OCT Calibration Accuracy Specifications for Cyclone V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–C6	–I7, –C7	–C8, –A7	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

Table 14. Internal Weak Pull-Up Resistor Values for Cyclone V Devices

Symbol	Description	Condition (V)[16]	Value[17]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Related Information

Cyclone V Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Cyclone V devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

(16) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(17) Valid with ±10% tolerances to cover changes over PVT.

Transceiver Performance Specifications

Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Table 21. Reference Clock Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL[31], HCSL, and LVDS										
Input frequency from REFCLK input pins[32]	—	27	—	550	27	—	550	27	—	550	MHz
Rise time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω

continued...

(30) Transceiver Speed Grade 5 covers specifications for Cyclone V GT and ST devices.

(31) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(32) The reference clock frequency must be ≥ 307.2 MHz to be fully compliance to CPRI transmit jitter specification at 6.144 Gbps. For more information about CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

(33) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Minimum differential eye opening at the receiver serial input pins[40]	—	110	—	—	110	—	—	110	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
V_{ICM} (AC coupled)	2.5 V PCML, LVPECL, and LVDS	V_{CCE_GXBL} supply[34][35]			V_{CCE_GXBL} supply			V_{CCE_GXBL} supply			V
	1.5 V PCML	0.65/0.75/0.8 [41]									V
t_{LTR}[42]	—	—	—	10	—	—	10	—	—	10	µs
t_{LTD}[43]	—	—	—	4	—	—	4	—	—	4	µs
t_{LTD_manual}[44]	—	—	—	4	—	—	4	—	—	4	µs
$t_{LTR\_LTD\_manual}$[45]	—	15	—	—	15	—	—	15	—	—	µs

continued...

(40) The differential eye opening specification at the receiver input pins assumes that you have disabled the Receiver Equalization feature. If you enable the Receiver Equalization feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(41) The AC coupled V_{ICM} = 650 mV for Cyclone V GX and SX in PCIe mode only. The AC coupled V_{ICM} = 750mV for Cyclone V GT and ST in PCIe mode only.

(42) t_{LTR} is the time required for the receive clock data recovery (CDR) to lock to the input reference clock frequency after coming out of reset.

(43) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(44) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting	Intel Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Intel Devices
Provides the Cyclone V HSSI HSPICE models.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
t_{OUTCCJ_IO}(58)(60)	Cycle-to-cycle jitter for clock output on regular I/O in integer PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
$t_{FOUTCCJ\_IO}$(58)(60)(61)	Cycle-to-cycle jitter for clock output on regular I/O in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$(58)(62)	Period jitter for dedicated clock output in cascaded PLLs	F_{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F_{OUT} < 100 MHz	—	—	30	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	Bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	f_{INPFD} = 100 MHz	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 49
Provides more information about the external memory interface clock output jitter specifications.

(61) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(62) The cascaded PLL specification is only applicable with the following conditions:
- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

High-Speed I/O Specifications

Table 34. High-Speed I/O Specifications for Cyclone V Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The Cyclone V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	437.5	5	—	420	5	—	320	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	320	5	—	320	5	—	275	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	840	(65)	—	740	(65)	—	640	Mbps

continued...

(63) Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

(64) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

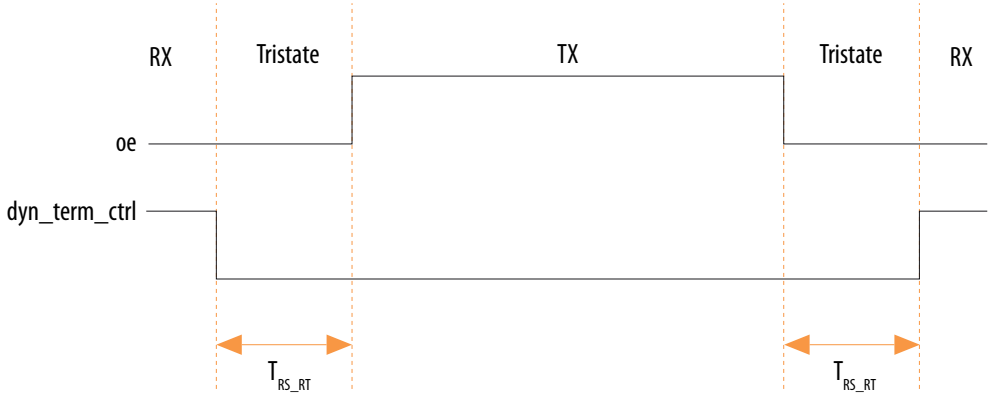
(65) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

OCT Calibration Block Specifications

Table 38. OCT Calibration Block Specifications for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT/R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for oe and dyn_term_ctrl Signals



HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 41. HPS PLL VCO Frequency Range for Cyclone V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C7, –I7, –A7, –C8	320	1,600	MHz
	–C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

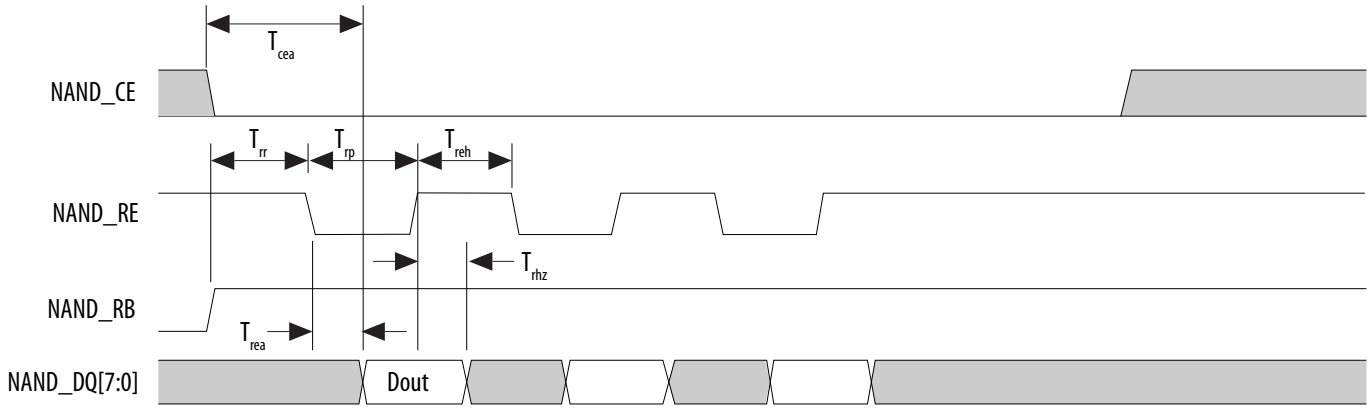
Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 42. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Figure 18. NAND Data Read Timing Diagram



Arm Trace Timing Characteristics

Table 53. Arm Trace Timing Requirements for Cyclone V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.

POR Specifications

Table 55. Fast and Standard POR Delay Specification for Cyclone V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12[74]	ms
Standard	100	300	ms

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 56. FPGA JTAG Timing Parameters and Values for Cyclone V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167[75]	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns

continued...

(74) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

(75) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

Symbol	Description	Min	Max	Unit
t_{JPCO}	JTAG port clock to output	—	11[76]	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14[76]	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14[76]	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Cyclone V devices use additional clock cycles to decrypt and decompress the configuration data. If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Cyclone V device.

Table 57. DCLK-to-DATA[] Ratio for Cyclone V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1

continued...

(76) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CL}	DCLK low time	0.45 × $1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(80)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

- FPP Configuration Timing
  Provides the FPP configuration timing waveforms.
- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 69

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 59. FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(81)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(82)	µs

continued...

(80) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(81) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Active Serial (AS) Configuration Timing

Table 60. AS Timing Parameters for AS ×1 and ×4 Configurations in Cyclone V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in *PS Timing Parameters for Cyclone V Devices* table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}[86]	Data hold time after the falling edge on DCLK	2.5[87]/2.9[88]	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

- Passive Serial (PS) Configuration Timing on page 74
- AS Configuration Timing
  Provides the AS configuration timing waveform.
- AN822: Intel FPGA Configuration Device Migration Guideline

(86) *Note:* To evaluate the data setup (t_{SU}) and data hold time (t_{DH}) slack on your board in order to ensure you are meeting the t_{SU} and t_{DH} requirement, you are recommended to follow the guideline in the "Evaluating Data Setup and Hold Timing Slack" chapter in *AN822: Intel FPGA Configuration Device Migration Guideline*.

(87) Specification for -6 speed grade

(88) Specification for -7 and -8 speed grade

Symbol	Parameter	Minimum	Maximum	Unit
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(92)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

Initialization

Table 63. Initialization Clock Source Option and the Maximum Frequency for Cyclone V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T_{init}
CLKUSR(93)	PS and FPP	125	
	AS	100	
DCLK	PS and FPP	125	

(92) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(93) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Intel Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Related Information

Configuration Files on page 76

Remote System Upgrades

Table 66. Remote System Upgrade Circuitry Timing Specifications for Cyclone V Devices

Parameter	Minimum	Unit
$t_{RU\_nCONFIG}$ (98)	250	ns
$t_{RU\_nRSTIMER}$ (99)	250	ns

Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about `reset_timer` (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 67. User Watchdog Internal Oscillator Frequency Specifications for Cyclone V Devices

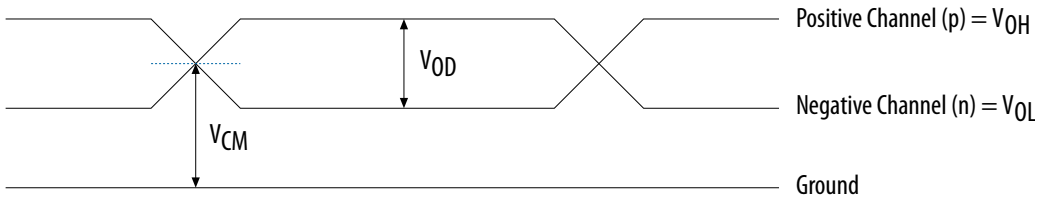
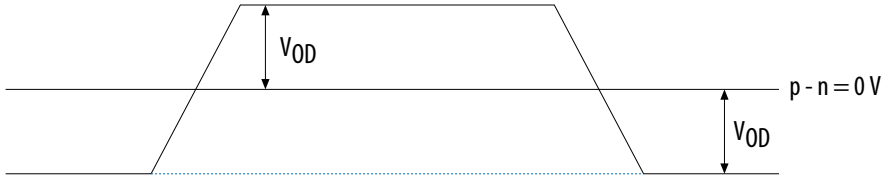
Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

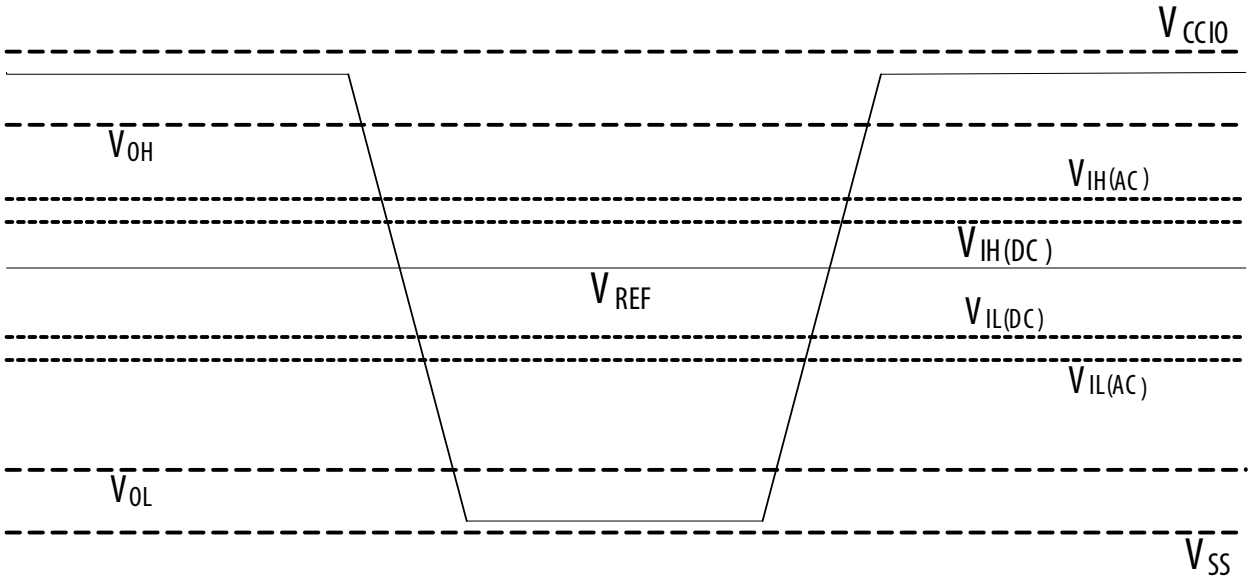
Intel offers two ways to determine I/O timing—the Excel-based I/O timing and the Intel Quartus Prime Timing Analyzer.

(98) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(99) This is equivalent to strobing the reset timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

Term	Definition
	Single-Ended Waveform  **Differential Waveform** 
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} =1/TUI).
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG timing specifications	JTAG Timing Specifications

continued...

Term	Definition
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard 
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input

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Date	Version	Changes
June 2013	3.4	• Updated Table 20, Table 27, and Table 34. • Updated "UART Interface" and "CAN Interface" sections. • Removed the following tables: — Table 45: UART Baud Rate for Cyclone V Devices — Table 47: CAN Pulse Width for Cyclone V Devices
May 2013	3.3	• Added Table 33. • Updated Figure 5, Figure 6, Figure 17, Figure 19, and Figure 20. • Updated Table 1, Table 4, Table 5, Table 10, Table 13, Table 19, Table 20, Table 26, Table 32, Table 35, Table 36, Table 43, Table 53, Table 54, Table 57, and Table 61.
March 2013	3.2	• Added HPS reset information in the "HPS Specifications" section. • Added Table 57. • Updated Table 1, Table 2, Table 17, Table 20, Table 52, and Table 56. • Updated Figure 18.
January 2013	3.1	Updated Table 4, Table 20, and Table 56.
November 2012	3.0	• Updated Table 1, Table 4, Table 5, Table 9, Table 14, Table 16, Table 17, Table 19, Table 20, Table 25, Table 28, Table 52, Table 55, Table 56, and Table 59. • Removed table: Transceiver Block Jitter Specifications for Cyclone V GX Devices. • Added HPS information: — Added "HPS Specifications" section. — Added Table 33, Table 34, Table 35, Table 36, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, and Table 46. — Added Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, and Figure 16. — Updated Table 3.
June 2012	2.0	Updated for the Quartus Prime software v12.0 release: • Restructured document. • Removed "Power Consumption" section. • Updated Table 1,Table 3, Table 19, Table 20, Table 25, Table 27, Table 28, Table 30, Table 31, Table 34, Table 36, Table 37, Table 38, Table 39, Table 41, Table 43, and Table 46. • Added Table 22, Table 23, and Table 29. • Added Figure 1 and Figure 2. • Added "Initialization" and "Configuration Files" sections.

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