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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

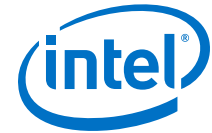
Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

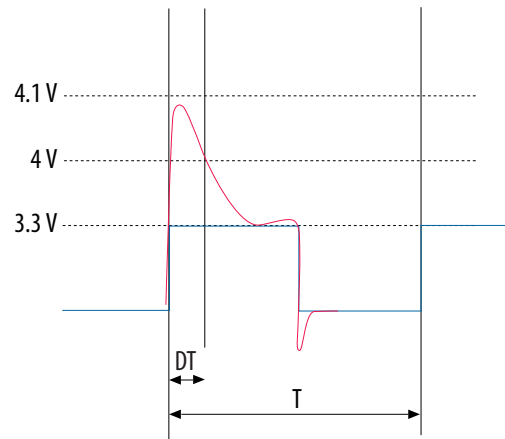
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csema5f31i7n



Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

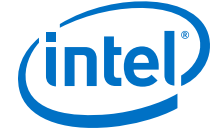
For an overshoot of 3.8 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as $([\Delta T]/T) \times 100$. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

Figure 1. Cyclone V Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Cyclone V devices.



OCT Without Calibration Resistance Tolerance Specifications

Table 10. OCT Without Calibration Resistance Tolerance Specifications for Cyclone V Devices

This table lists the Cyclone V OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			-C6	-I7, -C7	-C8, -A7	
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50-Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
100-Ω R _D	Internal differential termination (100-Ω setting)	V _{CCIO} = 2.5	±25	±40	±40	%

Figure 2. Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.



- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 11. OCT Variation after Power-Up Calibration for Cyclone V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0°C to 85°C .

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	



Table 14. Internal Weak Pull-Up Resistor Values for Cyclone V Devices

Symbol	Description	Condition (V) ⁽¹⁶⁾	Value ⁽¹⁷⁾	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V _{CCIO} = 3.3 ±5%	25	kΩ
		V _{CCIO} = 3.0 ±5%	25	kΩ
		V _{CCIO} = 2.5 ±5%	25	kΩ
		V _{CCIO} = 1.8 ±5%	25	kΩ
		V _{CCIO} = 1.5 ±5%	25	kΩ
		V _{CCIO} = 1.35 ±5%	25	kΩ
		V _{CCIO} = 1.25 ±5%	25	kΩ
		V _{CCIO} = 1.2 ±5%	25	kΩ

Related Information

[Cyclone V Device Family Pin Connection Guidelines](#)

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Cyclone V devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

⁽¹⁶⁾ Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

⁽¹⁷⁾ Valid with ±10% tolerances to cover changes over PVT.



I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	—	—	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 17. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Cyclone V Devices

I/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁹⁾ (mA)	I _{OH} ⁽¹⁹⁾ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} - 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} - 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} - 0.25	V _{REF} + 0.25	V _{TT} - 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} - 0.25	V _{REF} + 0.25	0.28	V _{CCIO} - 0.28	13.4	-13.4

continued...

⁽¹⁹⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



I/O Standard	V _{CCIO} (V)			V _{ID} (mV) ⁽²¹⁾			V _{ICM(DC)} (V)			V _{OD} (V) ⁽²²⁾			V _{OCM} (V) ⁽²²⁾⁽²³⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL ⁽²⁹⁾	—	—	—	300	—	—	0.60	D _{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D _{MAX} > 700 Mbps	1.60						
SLVS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
Sub-LVDS	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
HiSpi	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—

Related Information

- [AN522: Implementing Bus LVDS Interface in Supported Intel Device Families](#)
Provides more information about BLVDS interface support in Intel devices.
- [Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices](#) on page 25
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

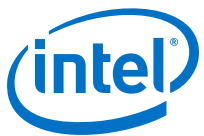
This section provides performance characteristics of Cyclone V core and periphery blocks.

⁽²¹⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

⁽²²⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

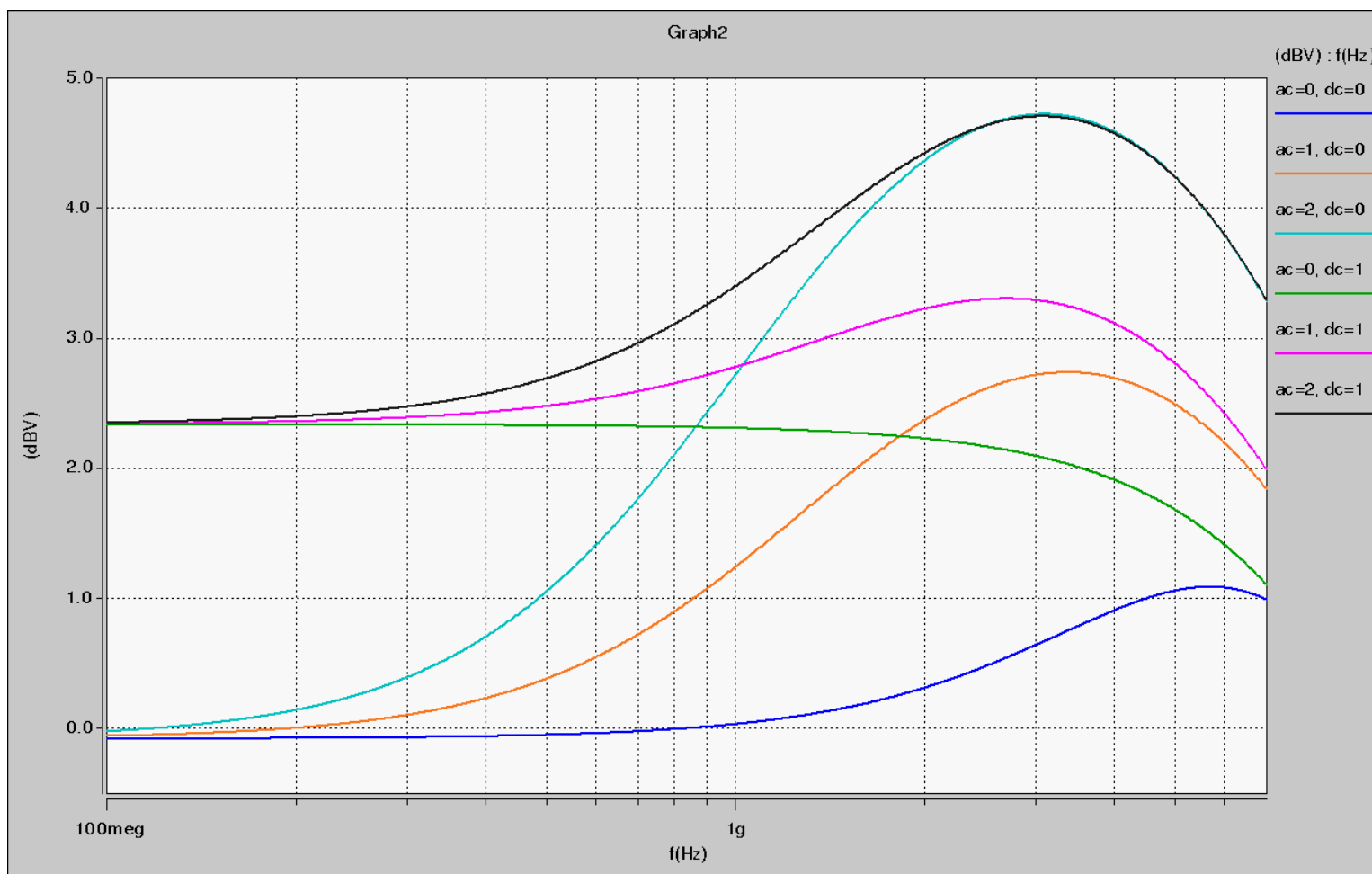
⁽²³⁾ This applies to default pre-emphasis setting only.

⁽²⁹⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.



CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

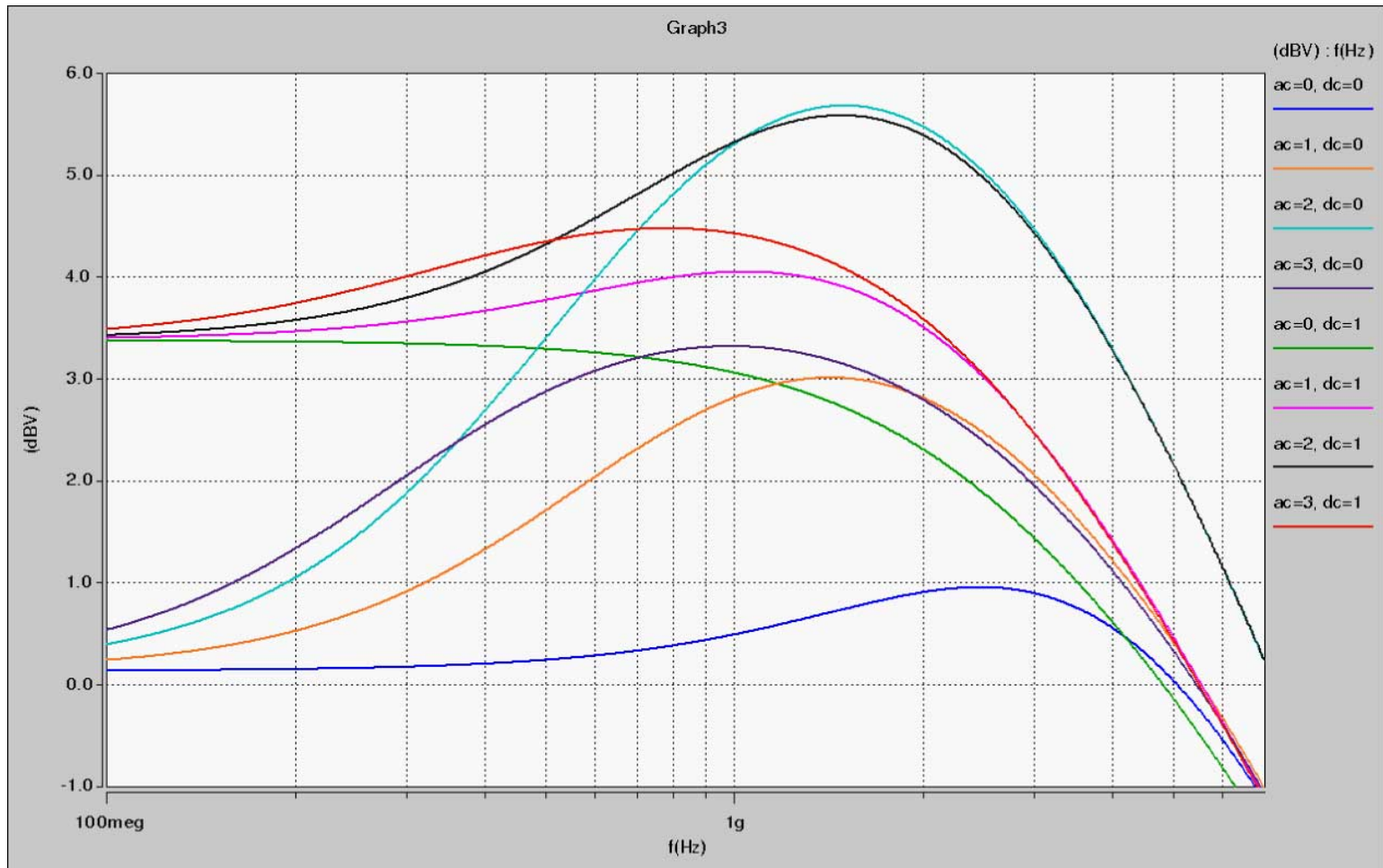
Figure 3. Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices





CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 4. CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices





Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

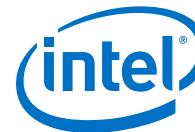
Table 27. Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting ⁽⁴⁸⁾	V_{OD} Value (mV)	V_{OD} Setting ⁽⁴⁸⁾	V_{OD} Value (mV)
V _{OD} differential peak-to-peak typical	6 ⁽⁴⁹⁾	120	34	680
	7 ⁽⁴⁹⁾	140	35	700
	8 ⁽⁴⁹⁾	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
23	460	51	1020	
24	480	52	1040	

continued...

⁽⁴⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

⁽⁴⁹⁾ Only valid for data rates \leq 5 Gbps.



Symbol	V _{OD} Setting ⁽⁴⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁴⁸⁾	V _{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Cyclone V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100 \Omega$ and $|C| = 1st$ post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

⁽⁴⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
t _{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t _{INCCJ} ⁽⁵⁶⁾⁽⁵⁷⁾	Input clock cycle-to-cycle jitter	F _{REF} ≥ 100 MHz	—	—	0.15	UI (p-p)
		F _{REF} < 100 MHz	—	—	±750	ps (p-p)
t _{OUTPJ_DC} ⁽⁵⁸⁾	Period jitter for dedicated clock output in integer PLL	F _{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F _{OUT} < 100 MHz	—	—	30	mUI (p-p)
t _{FOUTPJ_DC} ⁽⁵⁸⁾	Period jitter for dedicated clock output in fractional PLL	F _{OUT} ≥ 100 MHz	—	—	425 ⁽⁶¹⁾ , 300 ⁽⁵⁹⁾	ps (p-p)
		F _{OUT} < 100 MHz	—	—	42.5 ⁽⁶¹⁾ , 30 ⁽⁵⁹⁾	mUI (p-p)
t _{OUTCCJ_DC} ⁽⁵⁸⁾	Cycle-to-cycle jitter for dedicated clock output in integer PLL	F _{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F _{OUT} < 100 MHz	—	—	30	mUI (p-p)
t _{FOUTCCJ_DC} ⁽⁵⁸⁾	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	F _{OUT} ≥ 100 MHz	—	—	425 ⁽⁶¹⁾ , 300 ⁽⁵⁹⁾	ps (p-p)
		F _{OUT} < 100 MHz	—	—	42.5 ⁽⁶¹⁾ , 30 ⁽⁵⁹⁾	mUI (p-p)
t _{OUTPJ_IO} ⁽⁵⁸⁾⁽⁶⁰⁾	Period jitter for clock output on a regular I/O in integer PLL	F _{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F _{OUT} < 100 MHz	—	—	65	mUI (p-p)
t _{FOUTPJ_IO} ⁽⁵⁸⁾⁽⁶⁰⁾⁽⁶¹⁾	Period jitter for clock output on a regular I/O in fractional PLL	F _{OUT} ≥ 100 MHz	—	—	650	ps (p-p)

continued...

- (56) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.
- (57) F_{REF} is f_{IN}/N, specification applies when N = 1.
- (58) Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in *Memory Output Clock Jitter Specification for Cyclone V Devices* table.
- (59) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.
- (60) External memory interface clock output jitter specifications use a different measurement method, which are available in *Memory Output Clock Jitter Specification for Cyclone V Devices* table.



High-Speed I/O Specifications

Table 34. High-Speed I/O Specifications for Cyclone V Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The Cyclone V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	-C6			-C7, -I7			-C8, -A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40 ⁽⁶³⁾	5	—	437.5	5	—	420	5	—	320	MHz
f _{HCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40 ⁽⁶³⁾	5	—	320	5	—	320	5	—	275	MHz
f _{HCLK_OUT} (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J = 4 to 10 ⁽⁶⁴⁾	⁽⁶⁵⁾	—	840	⁽⁶⁵⁾	—	740	⁽⁶⁵⁾	—	640	Mbps
<i>continued...</i>												

⁽⁶³⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁶⁴⁾ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁶⁵⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.



HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 41. HPS PLL VCO Frequency Range for Cyclone V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	-C7, -I7, -A7, -C8	320	1,600	MHz
	-C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

[Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 42. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns



Related Information

Quad SPI Flash Controller Chapter, Cyclone V Hard Processor System Technical Reference Manual

Provides more information about R_{delay} .

SPI Timing Characteristics

Table 44. SPI Master Timing Requirements for Cyclone V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 ⁽⁶⁹⁾	—	ns
T_{h}	SPI MISO hold time	1	—	ns
$T_{\text{duty}}_{\text{cycle}}$	SPI_CLK duty cycle	45	55	%
T_{dssfrst}	Output delay SPI_SS valid before first clock edge	8	—	ns
T_{dsslst}	Output delay SPI_SS valid after last clock edge	8	—	ns
T_{dio}	Master-out slave-in (MOSI) output delay	-1	1	ns

⁽⁶⁹⁾ This value is based on $\text{rx_sample_dly} = 1$ and $\text{spi_m_clk} = 120$ MHz. spi_m_clk is the internal clock that is used by SPI Master to derive its SCLK_OUT. These timings are based on rx_sample_dly of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct rx_sample_dly value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about rx_sample_delay , refer to the *SPI Controller* chapter in the *Hard Processor System Technical Reference Manual*.



Figure 7. SPI Master Timing Diagram

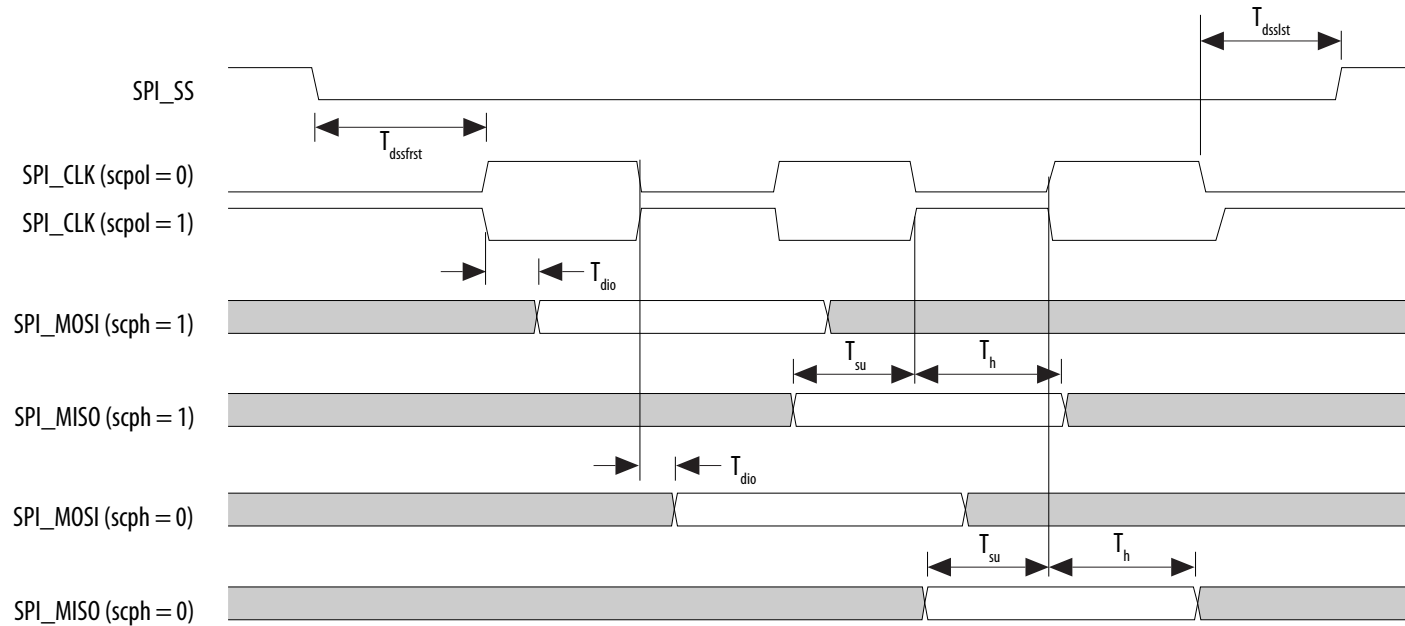


Table 45. SPI Slave Timing Requirements for Cyclone V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	20	—	ns
T_s	MOSI Setup time	5	—	ns
T_h	MOSI Hold time	5	—	ns
T_{suss}	Setup time SPI_SS valid before first clock edge	8	—	ns
T_{hss}	Hold time SPI_SS valid after last clock edge	8	—	ns
T_d	MISO output delay	—	6	ns



POR Specifications

Table 55. Fast and Standard POR Delay Specification for Cyclone V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 ⁽⁷⁴⁾	ms
Standard	100	300	ms

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 56. FPGA JTAG Timing Parameters and Values for Cyclone V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30, 167 ⁽⁷⁵⁾	—	ns
t _{JCH}	TCK clock high time	14	—	ns
t _{JCL}	TCK clock low time	14	—	ns
t _{JPSU (TDI)}	TDI JTAG port setup time	1	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	—	ns
t _{JPH}	JTAG port hold time	5	—	ns

continued...

⁽⁷⁴⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

⁽⁷⁵⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.



Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Cyclone V Devices table.

Table 58. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μs
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁷⁷⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽⁷⁸⁾	μs
t _{CF2CK} ⁽⁷⁹⁾	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽⁷⁹⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	0.45 × 1/f _{MAX}	—	s

continued...

⁽⁷⁷⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

⁽⁷⁸⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽⁷⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.



Active Serial (AS) Configuration Timing

Table 60. AS Timing Parameters for AS x1 and x4 Configurations in Cyclone V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in *PS Timing Parameters for Cyclone V Devices* table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding $nSTATUS$ low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
$t_{DH}^{(86)}$	Data hold time after the falling edge on DCLK	2.5 ⁽⁸⁷⁾ /2.9 ⁽⁸⁸⁾	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

- [Passive Serial \(PS\) Configuration Timing](#) on page 74
- [AS Configuration Timing](#)
Provides the AS configuration timing waveform.
- [AN822: Intel FPGA Configuration Device Migration Guideline](#)

⁽⁸⁶⁾ *Note:* To evaluate the data setup (t_{SU}) and data hold time (t_{DH}) slack on your board in order to ensure you are meeting the t_{SU} and t_{DH} requirement, you are recommended to follow the guideline in the "Evaluating Data Setup and Hold Timing Slack" chapter in *AN822: Intel FPGA Configuration Device Migration Guideline*.

⁽⁸⁷⁾ Specification for -6 speed grade

⁽⁸⁸⁾ Specification for -7 and -8 speed grade



Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device ⁽⁹⁴⁾
	A4	33,958,560	322,072	EPCQ128
	A5	56,057,632	324,888	EPCQ128
	A6	56,057,632	324,888	EPCQ128
Cyclone V SX	C2	33,958,560	322,072	EPCQ128
	C4	33,958,560	322,072	EPCQ128
	C5	56,057,632	324,888	EPCQ128
	C6	56,057,632	324,888	EPCQ128
Cyclone V ST	D5	56,057,632	324,888	EPCQ128
	D6	56,057,632	324,888	EPCQ128

Minimum Configuration Time Estimation

Table 65. Minimum Configuration Time Estimation for Cyclone V Devices

The estimated values are based on the configuration .rbf sizes in *Uncompressed .rbf Sizes for Cyclone V Devices* table.

Variant	Member Code	Active Serial ⁽⁹⁶⁾			Fast Passive Parallel ⁽⁹⁷⁾		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Cyclone V E	A2	4	100	53	16	125	11
	A4	4	100	53	16	125	11
	A5	4	100	85	16	125	17
	A7	4	100	140	16	125	28

continued...

⁽⁹⁴⁾ The recommended EPCQ serial configuration devices are able to store more than one image.

⁽⁹⁶⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽⁹⁷⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Programmable Output Buffer Delay

Table 69. Programmable Output Buffer Delay for Cyclone V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Intel Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Symbol	Parameter	Typical	Unit
D _{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

Table 70. Glossary

Term	Definition
Differential I/O standards	Receiver Input Waveforms

continued...