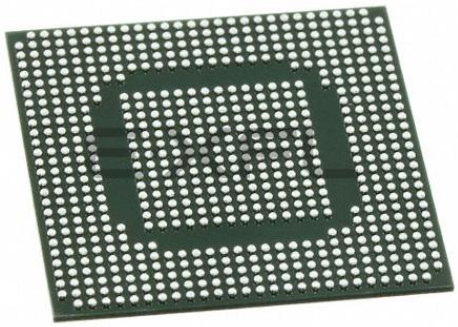

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-FBGA
Supplier Device Package	672-UBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csema5u23c8n

Density	Ordering Part Number (OPN)	Static Power Reduction
110K LE	5CSEBA6U19I7LN	
	5CSEBA6U23I7LN	
	5CSXFC6C6U23I7LN	

To estimate total power consumption for a low-power device, listed in Table 1 on page 3:

1. Multiply the Total Static Power reported by the Early Power Estimator (EPE) by the appropriate scale factor:
   - For 25K LE and 40K LE devices, use 0.7
   - For 85K LE and 110K LE devices, use 0.8
2. Add the result from Step 1 on page 4 to the Total Dynamic Power reported by the EPE.

Related Information

Cyclone V Device Overview
Provides more information about the densities and packages of devices in the Cyclone V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Cyclone V devices.

Operating Conditions

Cyclone V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Cyclone V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Cyclone V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions for Cyclone V Devices

This table lists the steady-state voltage values expected from Cyclone V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum(2)	Typical	Maximum(2)	Unit
V_{CC}	Core voltage, periphery circuitry power supply, transceiver physical coding sublayer (PCS) power supply, and transceiver PCI Express* (PCIe*) hard IP digital power supply	Devices without internal scrubbing feature	1.07	1.1	1.13	V
		Devices with internal scrubbing feature (with SC suffix) (3)	1.12	1.15	1.18	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCPD}(4)	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V

continued...

(2) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(3) The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Intel sales representatives.

(4) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

I/O Pin Leakage Current

Table 7. I/O Pin Leakage Current for Cyclone V Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 8. Bus Hold Parameters for Cyclone V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V <V_{IN} <V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 11. OCT Variation after Power-Up Calibration for Cyclone V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of ±5% and a temperature range of 0°C to 85°C.

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

Differential I/O Standard Specifications

Table 20. Differential I/O Standard Specifications for Cyclone V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[21]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[22]			V_{OCM} (V)[22][23]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to *Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices* table.														
2.5 V LVDS[24]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	D_{MAX} ≤ 700 Mbps	1.80	0.247	—	0.6	1.125	1.25	1.375
							1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS[25][26]	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO)[27]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)[28]	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4

continued...

(21) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(22) R_L range: 90 ≤ R_L ≤ 110 Ω.

(23) This applies to default pre-emphasis setting only.

(24) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rate above 700 Mbps and 0.00 V to 1.85 V for data rate below 700 Mbps.

(25) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

(26) For more information about BLVDS interface support in Intel devices, refer to *AN522: Implementing Bus LVDS Interface in Supported Intel Device Families*.

(27) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

(28) For optimized mini-LVDS receiver performance, the receiver voltage input range must be within 0.300 V to 1.425 V.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Minimum differential eye opening at the receiver serial input pins[40]	—	110	—	—	110	—	—	110	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
V_{ICM} (AC coupled)	2.5 V PCML, LVPECL, and LVDS	V_{CCE_GXBL} supply[34][35]			V_{CCE_GXBL} supply			V_{CCE_GXBL} supply			V
	1.5 V PCML	0.65/0.75/0.8 [41]									V
t_{LTR}[42]	—	—	—	10	—	—	10	—	—	10	µs
t_{LTD}[43]	—	—	—	4	—	—	4	—	—	4	µs
t_{LTD_manual}[44]	—	—	—	4	—	—	4	—	—	4	µs
$t_{LTR\_LTD\_manual}$[45]	—	15	—	—	15	—	—	15	—	—	µs

continued...

(40) The differential eye opening specification at the receiver input pins assumes that you have disabled the Receiver Equalization feature. If you enable the Receiver Equalization feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(41) The AC coupled V_{ICM} = 650 mV for Cyclone V GX and SX in PCIe mode only. The AC coupled V_{ICM} = 750mV for Cyclone V GT and ST in PCIe mode only.

(42) t_{LTR} is the time required for the receive clock data recovery (CDR) to lock to the input reference clock frequency after coming out of reset.

(43) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(44) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable ppm detector[46]	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000									ppm
Run length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to 3 [47] DC gain setting = 0 to 1	Refer to *CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices* and *CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices* diagrams.									dB

Table 24. Transmitter Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML										
Data rate	—	614	—	5000/6144[35]	614	—	3125	614	—	2500	Mbps
V_{OCM} (AC coupled)	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω

continued...

(45) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(46) The rate matcher supports only up to ±300 parts per million (ppm).

(47) The Intel Quartus Prime software allows AC gain setting = 3 for design with data rate between 614 Mbps and 1.25 Gbps only.

- 6.144-Gbps Support Capability in Cyclone V GT Devices
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Cyclone V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Intel Sales Representative.

Table 29. Transceiver Compliance Specification for All Supported Protocol for Cyclone V GX, GT, SX, and ST Devices

Protocol	Sub-protocol	Data Rate (Mbps)
PCIe	PCIe Gen1	2,500
	PCIe Gen2(50)	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
Serial RapidIO® (SRIO)	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
	SRIO 3125 LR	3,125
	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4

continued...

(50) For PCIe Gen2 sub-protocol, Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which ensure full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–C6	–C7, –I7	–C8, –A7	
	ROM, all supported width	0	1	420	350	300	MHz
M10K Block	Single-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port with the **read-during-write** option set to **Old Data**, all supported widths	0	1	275	240	180	MHz
	True dual port, all supported widths	0	1	315	275	240	MHz
	ROM, all supported widths	0	1	315	275	240	MHz

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 34. High-Speed I/O Specifications for Cyclone V Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The Cyclone V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	437.5	5	—	420	5	—	320	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	320	5	—	320	5	—	275	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	840	(65)	—	740	(65)	—	640	Mbps

continued...

(63) Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

(64) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(65) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
	Emulated Differential I/O Standards with Three External Output Resistor Networks- f_{HSDR} (data rate)(67)	SERDES factor J = 4 to 10	(65)	—	640	(65)	—	640	(65)	—	550	Mbps
	Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)	SERDES factor J = 4 to 10	(65)	—	170	(65)	—	170	(65)	—	170	Mbps
	$t_{x\ Jitter}$ -True Differential I/O Standards(67)	Total Jitterfor Data Rate, 600 Mbps – 840 Mbps	—	—	350	—	—	380	—	—	500	ps
		Total Jitter for Data Rate < 600Mbps	—	—	0.21	—	—	0.23	—	—	0.30	UI
	$t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Networks	Total Jitter for Data Rate < 640Mbps	—	—	500	—	—	500	—	—	500	ps
	$t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network	Total Jitter for Data Rate < 640Mbps	—	—	0.15	—	—	0.15	—	—	0.15	UI
	t_{DUTY}	TX output clock duty cycle for both True and	45	50	55	45	50	55	45	50	55	%

continued...

(66) The maximum ideal data rate is the SERDES factor (J) × PLL max output frequency (f_{out}), provided you can close the design timing and the signal integrity simulation is clean. You can estimate the achievable maximum data rate by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(67) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 41. HPS PLL VCO Frequency Range for Cyclone V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C7, –I7, –A7, –C8	320	1,600	MHz
	–C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

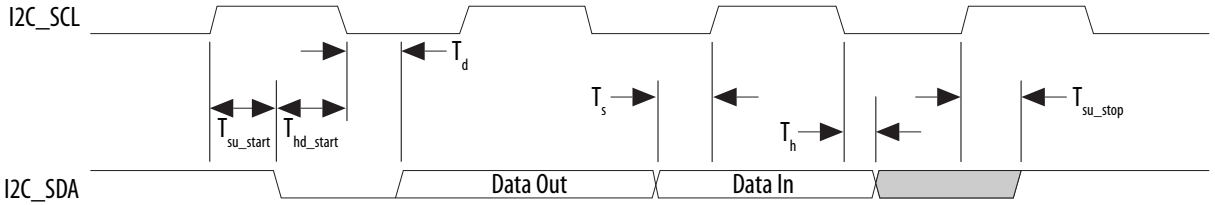
Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 42. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Figure 14. I²C Timing Diagram



NAND Timing Characteristics

Table 52. NAND ONFI 1.0 Timing Requirements for Cyclone V Devices

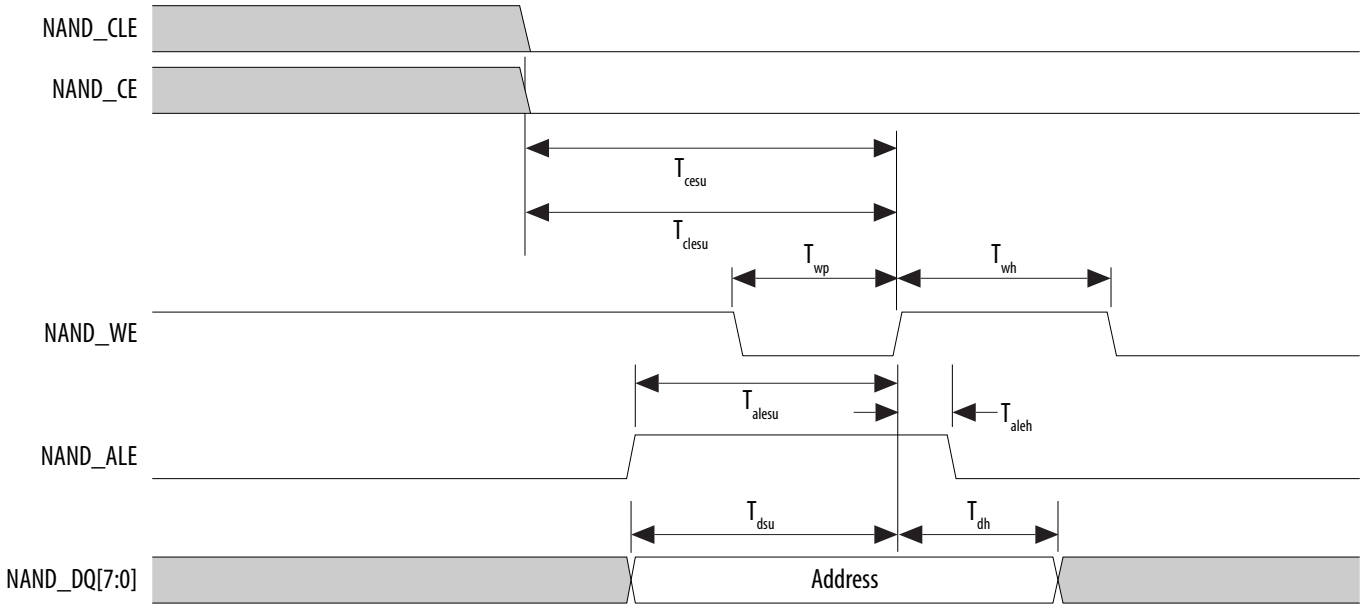
The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T_{wp} (72)	Write enable pulse width	10	—	ns
T_{wh} (72)	Write enable hold time	7	—	ns
T_{rp} (72)	Read enable pulse width	10	—	ns
T_{reh} (72)	Read enable hold time	7	—	ns
T_{clesu} (72)	Command latch enable to write enable setup time	10	—	ns
T_{cleh} (72)	Command latch enable to write enable hold time	5	—	ns
T_{cesu} (72)	Chip enable to write enable setup time	15	—	ns
T_{ceh} (72)	Chip enable to write enable hold time	5	—	ns
T_{alesu} (72)	Address latch enable to write enable setup time	10	—	ns
T_{aleh} (72)	Address latch enable to write enable hold time	5	—	ns
T_{dsu} (72)	Data to write enable setup time	10	—	ns
T_{dh} (72)	Data to write enable hold time	5	—	ns

continued...

(72) Timing of the NAND interface is controlled through the NAND configuration registers.

Figure 16. NAND Address Latch Timing Diagram



Symbol	Description	Min	Max	Unit
t_{JPCO}	JTAG port clock to output	—	11[76]	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14[76]	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14[76]	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Cyclone V devices use additional clock cycles to decrypt and decompress the configuration data. If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Cyclone V device.

Table 57. DCLK-to-DATA[] Ratio for Cyclone V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1

continued...

(76) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK}[83]	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}[83]	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$[84]	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode[85]	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times$ CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(82) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

(83) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(84) *N* is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

(85) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device(94)
	A4	33,958,560	322,072	EPCQ128
	A5	56,057,632	324,888	EPCQ128
	A6	56,057,632	324,888	EPCQ128
Cyclone V SX	C2	33,958,560	322,072	EPCQ128
	C4	33,958,560	322,072	EPCQ128
	C5	56,057,632	324,888	EPCQ128
	C6	56,057,632	324,888	EPCQ128
Cyclone V ST	D5	56,057,632	324,888	EPCQ128
	D6	56,057,632	324,888	EPCQ128

Minimum Configuration Time Estimation

Table 65. Minimum Configuration Time Estimation for Cyclone V Devices

The estimated values are based on the configuration `.rbf` sizes in *Uncompressed .rbf Sizes for Cyclone V Devices* table.

Variant	Member Code	Active Serial(96)			Fast Passive Parallel(97)		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Cyclone V E	A2	4	100	53	16	125	11
	A4	4	100	53	16	125	11
	A5	4	100	85	16	125	17
	A7	4	100	140	16	125	28

continued...

(94) The recommended EPCQ serial configuration devices are able to store more than one image.

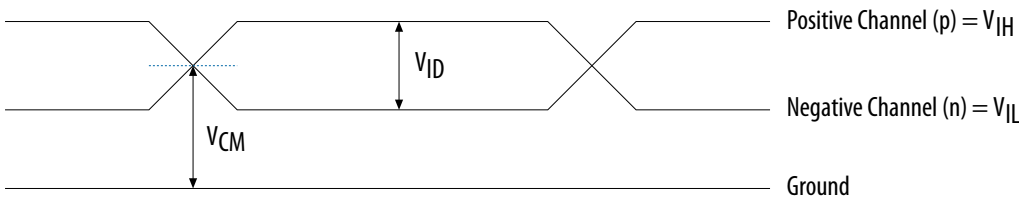
(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Variant	Member Code	Active Serial[96]			Fast Passive Parallel[97]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A9	4	100	257	16	125	51
Cyclone V GX	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms

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