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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 110K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csema6f31c8n



Symbol	Description	Condition	Minimum ⁽²⁾	Typical	Maximum ⁽²⁾	Unit
V _{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V _{CCA_FPLL} ⁽⁵⁾	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CCBAT} ⁽⁶⁾	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V _I	DC input voltage	—	-0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	-40	—	100	°C
		Automotive	-40	—	125	°C
t _{RAMP} ⁽⁷⁾	Power supply ramp time	Standard POR	200μs	—	100ms	—
		Fast POR	200μs	—	4ms	—

⁽²⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁵⁾ PLL digital voltage is regulated from V_{CCA_FPLL}.

⁽⁶⁾ If you do not use the design security feature in Cyclone V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Cyclone V power-on reset (POR) circuitry monitors V_{CCBAT}. Cyclone V devices do not exit POR if V_{CCBAT} is not powered up.

⁽⁷⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.



Pin Capacitance

Table 12. Pin Capacitance for Cyclone V Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on left and right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 13. Hot Socketing Specifications for Cyclone V Devices

Symbol	Description	Maximum	Unit
I _{IOPIN} (DC)	DC current per I/O pin	300	μA
I _{IOPIN} (AC)	AC current per I/O pin	8 ⁽¹⁵⁾	mA
I _{XCVR-TX} (DC)	DC current per transceiver transmitter (TX) pin	100	mA
I _{XCVR-RX} (DC)	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

⁽¹⁵⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C \, dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.



Single-Ended I/O Standards

Table 15. Single-Ended I/O Standards for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁸⁾ (mA)	I _{OH} ⁽¹⁸⁾ (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} - 0.2	2	-2
3.0-V LVTTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} - 0.2	0.1	-0.1
3.0-V PCI*	2.85	3	3.15	—	0.3 × V _{CCIO}	0.5 × V _{CCIO}	V _{CCIO} + 0.3	0.1 × V _{CCIO}	0.9 × V _{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V _{CCIO}	0.5 × V _{CCIO}	V _{CCIO} + 0.3	0.1 × V _{CCIO}	0.9 × V _{CCIO}	1.5	-0.5
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V _{CCIO}	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} - 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	0.35 × V _{CCIO}	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.25 × V _{CCIO}	0.75 × V _{CCIO}	2	-2
1.2 V	1.14	1.2	1.26	-0.3	0.35 × V _{CCIO}	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.25 × V _{CCIO}	0.75 × V _{CCIO}	2	-2

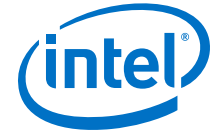
Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V _{CCIO}	0.5 × V _{CCIO}	0.51 × V _{CCIO}	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04

continued...

⁽¹⁸⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	$I_{OL}^{(19)}$ (mA)	$I_{OH}^{(19)}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
SSTL-125	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

⁽¹⁹⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



Differential SSTL I/O Standards

Table 18. Differential SSTL I/O Standards for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.2	—	V _{CCIO} /2 + 0.2	0.62	V _{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.175	—	V _{CCIO} /2 + 0.175	0.5	V _{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	⁽²⁰⁾	V _{CCIO} /2 - 0.15	—	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-135	1.283	1.35	1.45	0.18	⁽²⁰⁾	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})
SSTL-125	1.19	1.25	1.31	0.18	⁽²⁰⁾	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	2(V _{IL(AC)} - V _{REF})

Differential HSTL and HSUL I/O Standards

Table 19. Differential HSTL and HSUL I/O Standards for Cyclone V Devices

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	—	0.5 × V _{CCIO}	—	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V _{CCIO} - 0.12	0.5 × V _{CCIO}	0.5 × V _{CCIO} + 0.12	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44	0.44

⁽²⁰⁾ The maximum value for V_{SWING(DC)} is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V_{IH(DC)} and V_{IL(DC)}).



Transceiver Performance Specifications

Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Table 21. Reference Clock Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5 ⁽³⁰⁾			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽³¹⁾ , HCSSL, and LVDS										
Input frequency from REFCLK input pins ⁽³²⁾	—	27	—	550	27	—	550	27	—	550	MHz
Rise time	Measure at ±60 mV of differential signal ⁽³³⁾	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽³³⁾	—	—	400	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%	—	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω

continued...

- ⁽³⁰⁾ Transceiver Speed Grade 5 covers specifications for Cyclone V GT and ST devices.
- ⁽³¹⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
- ⁽³²⁾ The reference clock frequency must be ≥ 307.2 MHz to be fully compliance to CPRI transmit jitter specification at 6.144 Gbps. For more information about CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.
- ⁽³³⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.



Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting	Intel Quartus Prime V _{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

[SPICE Models for Intel Devices](#)

Provides the Cyclone V HSSI HSPICE models.



- 6.144-Gbps Support Capability in Cyclone V GT Devices
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

Core Performance Specifications

Clock Tree Specifications

Table 30. Clock Tree Specifications for Cyclone V Devices

Parameter	Performance			Unit
	-C6	-C7, -I7	-C8, -A7	
Global clock and Regional clock	550	550	460	MHz
Peripheral clock	155	155	155	MHz

PLL Specifications

Table 31. PLL Specifications for Cyclone V Devices

This table lists the Cyclone V PLL block specifications. Cyclone V PLL block does not include HPS PLL.

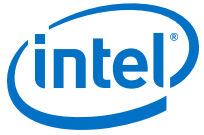
Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	-C6 speed grade	5	—	670 ⁽⁵²⁾	MHz
		-C7, -I7 speed grades	5	—	622 ⁽⁵²⁾	MHz
		-C8, -A7 speed grades	5	—	500 ⁽⁵²⁾	MHz
f_{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	—	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	—	50	—	160	MHz
f_{VCO} ⁽⁵³⁾	PLL voltage-controlled oscillator (VCO) operating range	-C6, -C7, -I7 speed grades	600	—	1600	MHz

continued...

⁽⁵²⁾ This specification is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.



Symbol		Condition	-C6			-C7, -17			-C8, -A7			Unit	
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
		Emulated Differential I/O Standards											
	t _{RISE} and t _{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps	
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps	
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps	
	TCCS	True Differential I/O Standards	—	—	200	—	—	250	—	—	250	ps	
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	300	—	—	300	—	—	300	ps	
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps	
	Receiver	f _{HSDR} (data rate)	SERDES factor J = 4 to 10 ⁽⁶⁴⁾	⁽⁶⁵⁾	—	875 ⁽⁶⁷⁾	⁽⁶⁵⁾	—	840 ⁽⁶⁷⁾	⁽⁶⁵⁾	—	640 ⁽⁶⁷⁾	Mbps
			SERDES factor J = 1 to 2, uses DDR registers	⁽⁶⁵⁾	—	⁽⁶⁶⁾	⁽⁶⁵⁾	—	⁽⁶⁶⁾	⁽⁶⁵⁾	—	⁽⁶⁶⁾	Mbps
Sampling Window			—	—	350	—	—	350	—	—	350	ps	

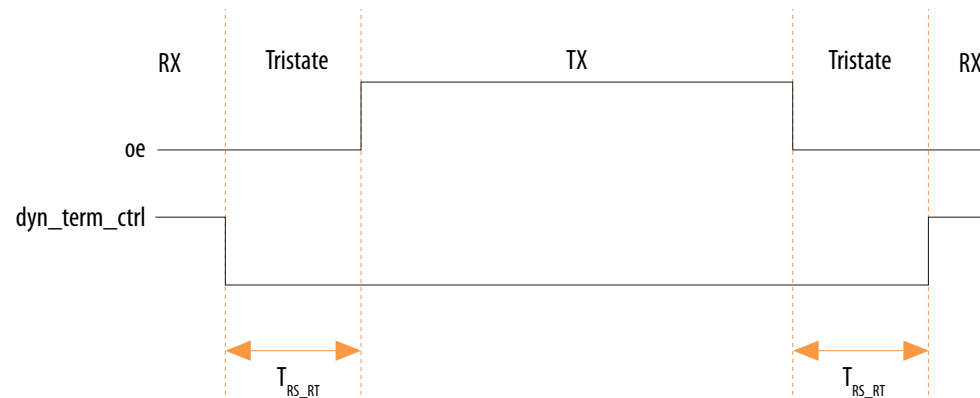


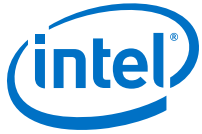
OCT Calibration Block Specifications

Table 38. OCT Calibration Block Specifications for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for R _S OCT/R _T OCT calibration	—	1000	—	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R _S OCT and R _T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for oe and dyn_term_ctrl Signals





HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 41. HPS PLL VCO Frequency Range for Cyclone V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	-C7, -I7, -A7, -C8	320	1,600	MHz
	-C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

[Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

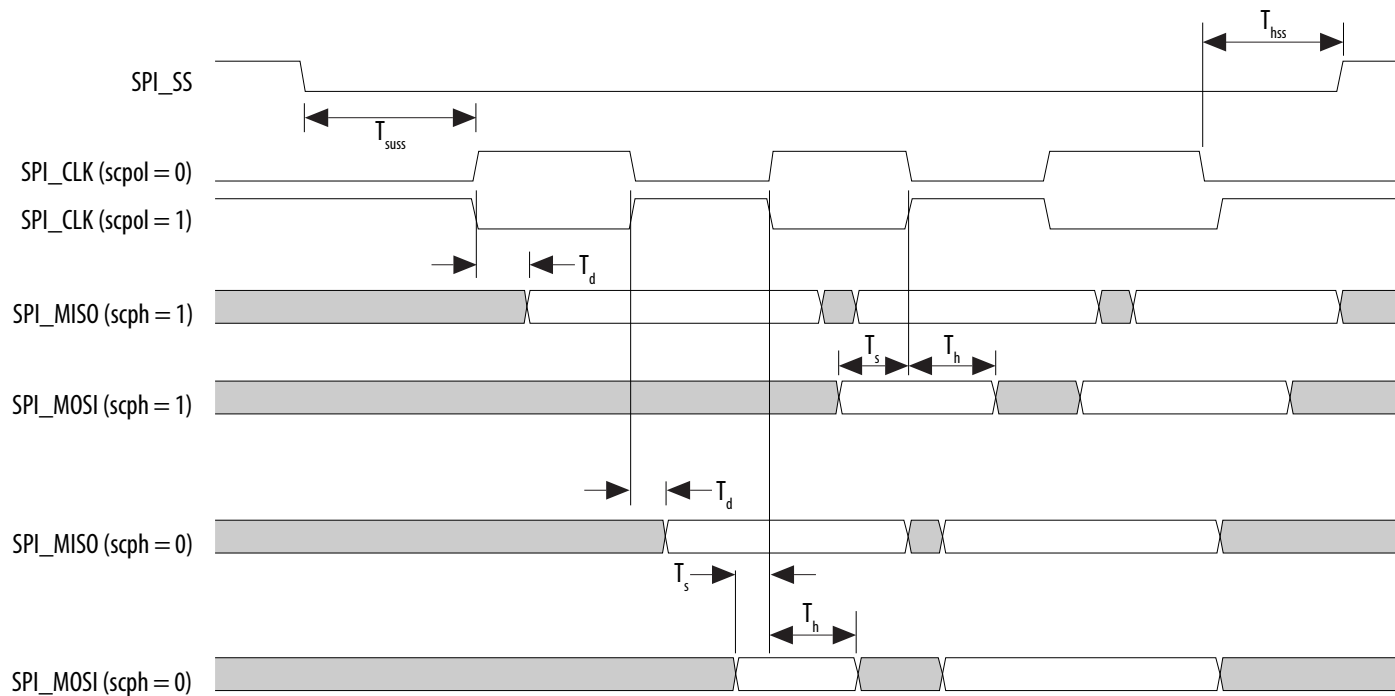
Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 42. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Figure 8. SPI Slave Timing Diagram



Related Information

[SPI Controller, Cyclone V Hard Processor System Technical Reference Manual](#)

Provides more information about `rx_sample_delay`.



SD/MMC Timing Characteristics

Table 46. Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices

After power up or cold reset, the Boot ROM uses $drvsel = 3$ and $smp1sel = 0$ to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock $SDMMC_CLK_OUT$ changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock $SDMMC_CLK$ and the $CSEL$ setting. The value of $SDMMC_CLK$ is based on the external oscillator frequency and has a maximum value of 50 MHz.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of $drvsel$ and $smp1sel$ via the system manager. $drvsel$ can be set from 1 to 7 and $smp1sel$ can be set from 0 to 7. While the preloader is executing, the values for $SDMMC_CLK$ and $SDMMC_CLK_OUT$ increase to a maximum of 200 MHz and 50 MHz respectively.

Symbol	Description	Min	Max	Unit
T_{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{sdmmc_clk_out}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
T_{duty}	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	$(T_{sdmmc_clk} \times drvsel)/2 - 1.23$ ⁽⁷⁰⁾	$(T_{sdmmc_clk} \times drvsel)/2 + 1.69$ ⁽⁷⁰⁾	ns
T_{su}	Input setup time	$1.05 - (T_{sdmmc_clk} \times smp1sel)/2$ ⁽⁷¹⁾	—	ns
T_h	Input hold time	$(T_{sdmmc_clk} \times smp1sel)/2$ ⁽⁷¹⁾	—	ns

⁽⁷⁰⁾ $drvsel$ is the drive clock phase shift select value.

⁽⁷¹⁾ $smp1sel$ is the sample clock phase shift select value.

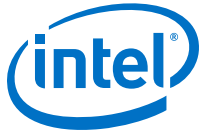
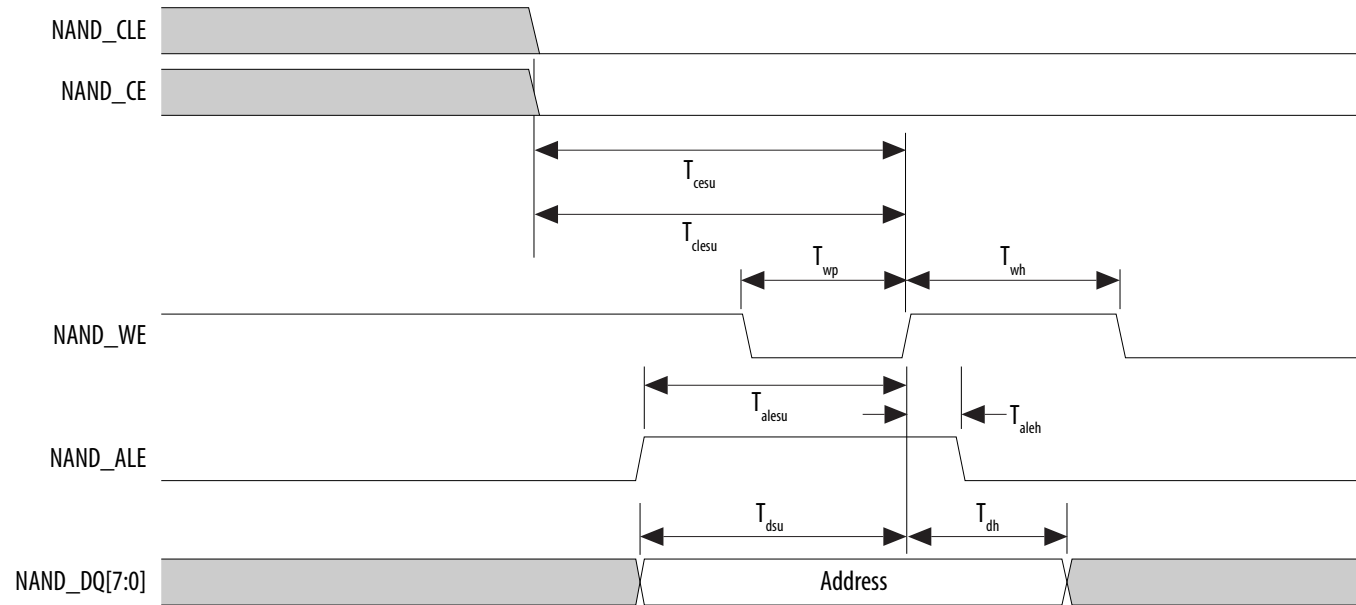


Figure 16. NAND Address Latch Timing Diagram





CAN Interface

The maximum controller area network (CAN) data rate is 1 Mbps.

HPS JTAG Timing Specifications

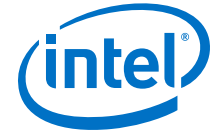
Table 54. HPS JTAG Timing Parameters and Values for Cyclone V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30	—	ns
t _{JCH}	TCK clock high time	14	—	ns
t _{JCL}	TCK clock low time	14	—	ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	—	ns
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	12 ⁽⁷³⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁷³⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁷³⁾	ns

Configuration Specifications

This section provides configuration specifications and timing for Cyclone V devices.

⁽⁷³⁾ A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.



Active Serial (AS) Configuration Timing

Table 60. AS Timing Parameters for AS x1 and x4 Configurations in Cyclone V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in *PS Timing Parameters for Cyclone V Devices* table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding $nSTATUS$ low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
$t_{DH}^{(86)}$	Data hold time after the falling edge on DCLK	$2.5^{(87)}/2.9^{(88)}$	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

- [Passive Serial \(PS\) Configuration Timing](#) on page 74
- [AS Configuration Timing](#)
Provides the AS configuration timing waveform.
- [AN822: Intel FPGA Configuration Device Migration Guideline](#)

⁽⁸⁶⁾ *Note:* To evaluate the data setup (t_{SU}) and data hold time (t_{DH}) slack on your board in order to ensure you are meeting the t_{SU} and t_{DH} requirement, you are recommended to follow the guideline in the "Evaluating Data Setup and Hold Timing Slack" chapter in *AN822: Intel FPGA Configuration Device Migration Guideline*.

⁽⁸⁷⁾ Specification for -6 speed grade

⁽⁸⁸⁾ Specification for -7 and -8 speed grade



Symbol	Parameter	Minimum	Maximum	Unit
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t _{CLK}	DCLK period	$1/f_{MAX}$	—	s
f _{MAX}	DCLK frequency	—	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁹²⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (T _{init} × CLKUSR period)	—	—
T _{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.

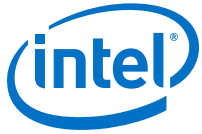
Initialization

Table 63. Initialization Clock Source Option and the Maximum Frequency for Cyclone V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T _{init}
CLKUSR ⁽⁹³⁾	PS and FPP	125	
	AS	100	
DCLK	PS and FPP	125	

⁽⁹²⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽⁹³⁾ To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Intel Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.



Variant	Member Code	Active Serial ⁽⁹⁶⁾			Fast Passive Parallel ⁽⁹⁷⁾		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Cyclone V GX	A9	4	100	257	16	125	51
	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

⁽⁹⁶⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽⁹⁷⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Programmable Output Buffer Delay

Table 69. Programmable Output Buffer Delay for Cyclone V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Intel Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

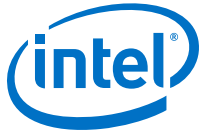
Symbol	Parameter	Typical	Unit
D _{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

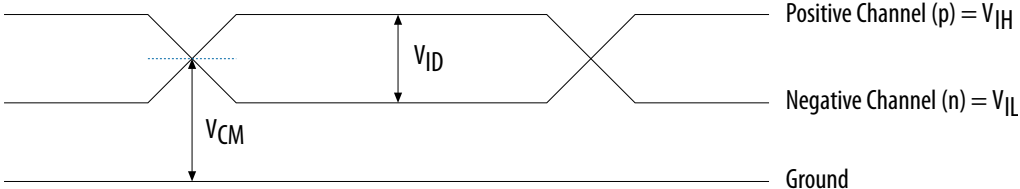
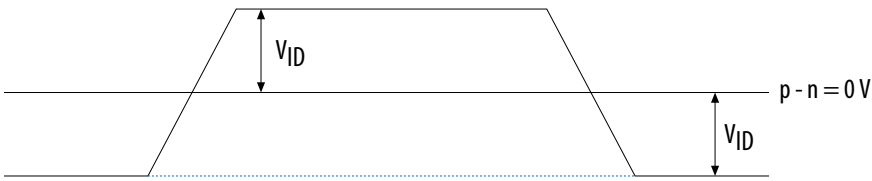
Glossary

Table 70. Glossary

Term	Definition
Differential I/O standards	Receiver Input Waveforms

continued...



Term	Definition
	<p data-bbox="730 316 970 344">Single-Ended Waveform</p>  <p data-bbox="1507 365 1743 393">Positive Channel (p) = V_{IH}</p> <p data-bbox="1507 446 1743 474">Negative Channel (n) = V_{IL}</p> <p data-bbox="1507 527 1575 555">Ground</p> <p data-bbox="730 609 955 636">Differential Waveform</p>  <p data-bbox="1507 730 1596 758">$p - n = 0V$</p> <p data-bbox="592 860 886 888">Transmitter Output Waveforms</p> <p data-bbox="1738 917 1869 945"><i>continued...</i></p>