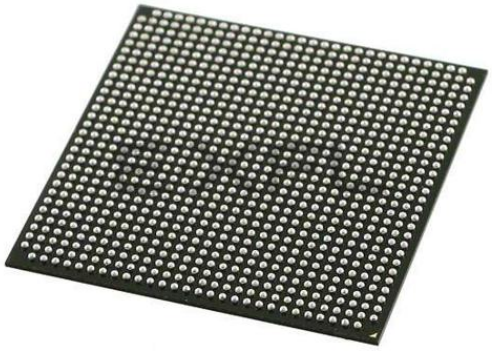

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5cstfd5d5f31i7n

Table 2. Absolute Maximum Ratings for Cyclone V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.5	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO}	I/O power supply	–0.5	3.90	V
V_{CCA_FPLL}	Phase-locked loop (PLL) analog power supply	–0.5	3.25	V
V_{CCH_GXB}	Transceiver high voltage power	–0.5	3.25	V
V_{CCE_GXB}	Transceiver power	–0.5	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.5	1.50	V
V_I	DC input voltage	–0.5	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.5	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.5	3.90	V
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.5	3.25	V
$V_{CC\_AUX\_SHARED}$ (1)	HPS auxiliary power supply	–0.5	3.25	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

(1) $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.

I/O Pin Leakage Current

Table 7. I/O Pin Leakage Current for Cyclone V Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 8. Bus Hold Parameters for Cyclone V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V <V_{IN} <V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Single-Ended I/O Standards

Table 15. Single-Ended I/O Standards for Cyclone V Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL}[18] (mA)	I_{OH}[18] (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
3.0-V PCI*	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Cyclone V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04

continued...

(18) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[21]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[22]			V_{OCM} (V)[22][23]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL[29]	—	—	—	300	—	—	0.60	D_{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D_{MAX} > 700 Mbps	1.60						
SLVS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
Sub-LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
HiSpi	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—

Related Information

- AN522: Implementing Bus LVDS Interface in Supported Intel Device Families
  Provides more information about BLVDS interface support in Intel devices.
- Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices on page 25
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Cyclone V core and periphery blocks.

(21) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(22) R_L range: 90 ≤ R_L ≤ 110 Ω.

(23) This applies to default pre-emphasis setting only.

(29) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{ICM} (AC coupled)	—	V_{CCE_GXBL} supply[34][35]			V_{CCE_GXBL} supply			V_{CCE_GXBL} supply			V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK phase noise[36]	10 Hz	—	—	–50	—	—	–50	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	—	—	–80	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	—	—	–110	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	—	—	–120	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	—	—	–120	—	—	–120	dBc/Hz
	≥1 MHz	—	—	–130	—	—	–130	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

(30) Transceiver Speed Grade 5 covers specifications for Cyclone V GT and ST devices.

(34) Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which require full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

(35) Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144 Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

(36) The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12}.

Symbol	V_{OD} Setting[48]	V_{OD} Value (mV)	V_{OD} Setting[48]	V_{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Cyclone V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

(48) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Cyclone V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Intel Sales Representative.

Table 29. Transceiver Compliance Specification for All Supported Protocol for Cyclone V GX, GT, SX, and ST Devices

Protocol	Sub-protocol	Data Rate (Mbps)
PCIe	PCIe Gen1	2,500
	PCIe Gen2(50)	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
Serial RapidIO® (SRIO)	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
	SRIO 3125 LR	3,125
	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4

continued...

(50) For PCIe Gen2 sub-protocol, Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which ensure full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		–C8, –A7 speed grades	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	–C6, –C7, –I7 speed grades	—	—	550(54)	MHz
		–C8, –A7 speed grades	—	—	460(54)	MHz
f_{OUT_EXT}	Output frequency for external clock output	–C6, –C7, –I7 speed grades	—	—	667(54)	MHz
		–C8, –A7 speed grades	—	—	533(54)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$t_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High(55)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps

continued...

(53) The VCO frequency reported by the Intel Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(54) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

(55) High bandwidth PLL settings are not supported in external feedback mode.

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–C6	–C7, –I7	–C8, –A7	
	ROM, all supported width	0	1	420	350	300	MHz
M10K Block	Single-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port, all supported widths	0	1	315	275	240	MHz
	Simple dual-port with the **read-during-write** option set to **Old Data**, all supported widths	0	1	275	240	180	MHz
	True dual port, all supported widths	0	1	315	275	240	MHz
	ROM, all supported widths	0	1	315	275	240	MHz

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

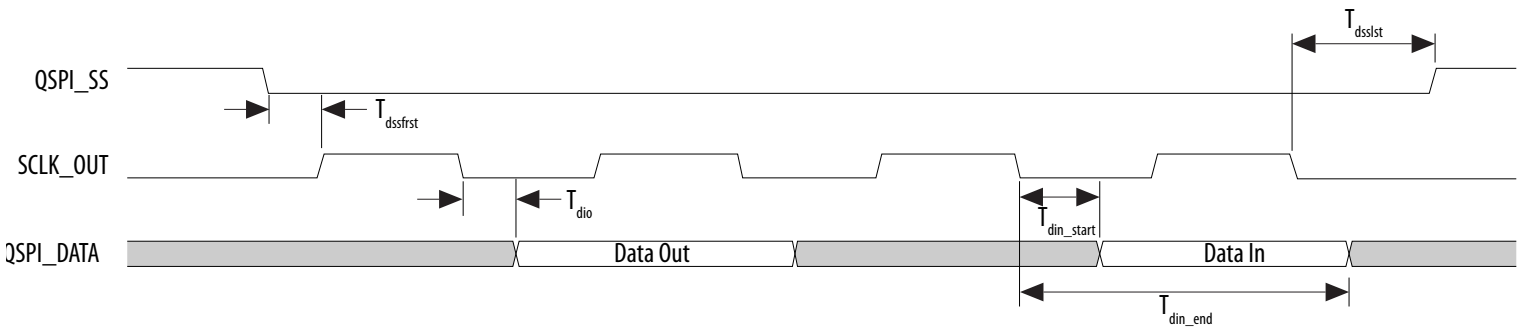
Quad SPI Flash Timing Characteristics

Table 43. Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (68)	ns
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (68)	—	—	ns

Figure 6. Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



(68) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Intel provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the *Quad SPI Flash Controller chapter in the Cyclone V Hard Processor System Technical Reference Manual*.

Related Information

Quad SPI Flash Controller Chapter, Cyclone V Hard Processor System Technical Reference Manual
Provides more information about R_{delay}.

SPI Timing Characteristics

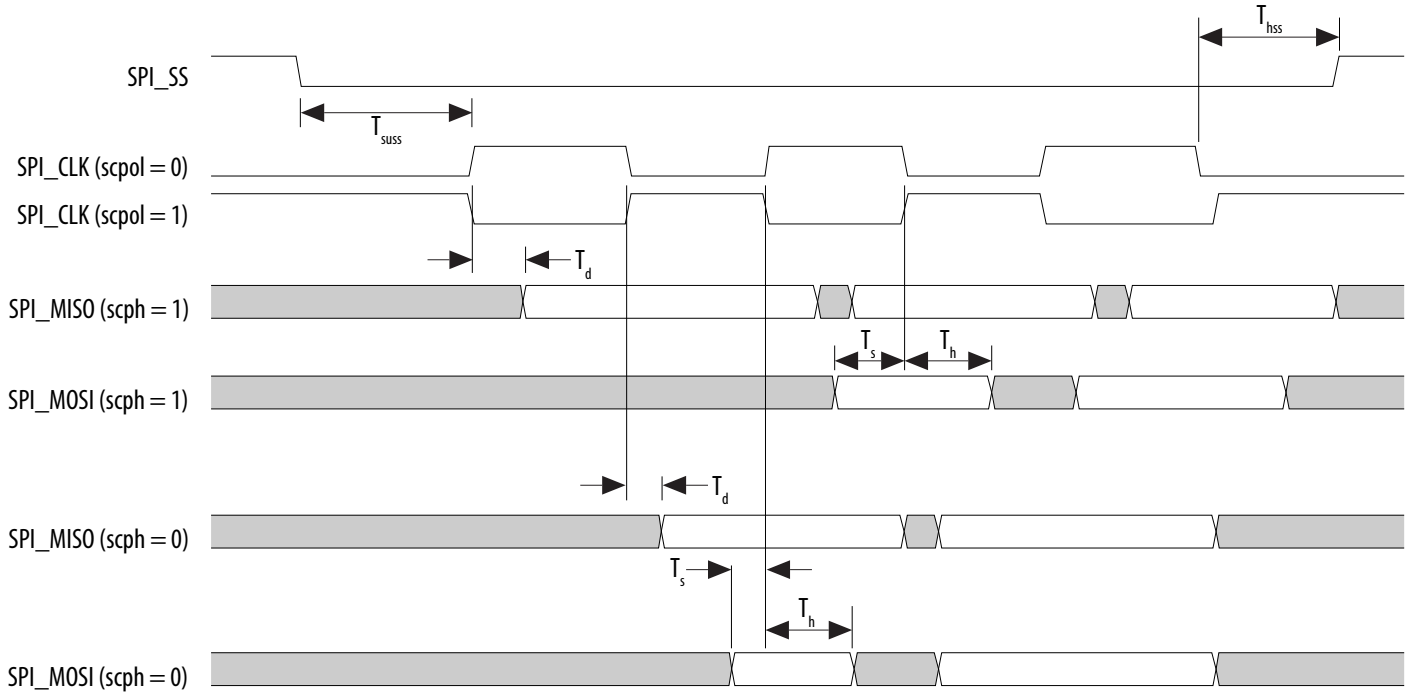
Table 44. SPI Master Timing Requirements for Cyclone V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 (69)	—	ns
T_{h}	SPI MISO hold time	1	—	ns
$T_{dutycycle}$	SPI_CLK duty cycle	45	55	%
$T_{dssfrst}$	Output delay SPI_SS valid before first clock edge	8	—	ns
T_{dsslst}	Output delay SPI_SS valid after last clock edge	8	—	ns
T_{dio}	Master-out slave-in (MOSI) output delay	–1	1	ns

(69) This value is based on `rx_sample_dly` = 1 and `spi_m_clk` = 120 MHz. `spi_m_clk` is the internal clock that is used by SPI Master to derive it's SCLK_OUT. These timings are based on `rx_sample_dly` of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct `rx_sample_dly` value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about `rx_sample_delay`, refer to the *SPI Controller* chapter in the *Hard Processor System Technical Reference Manual*.

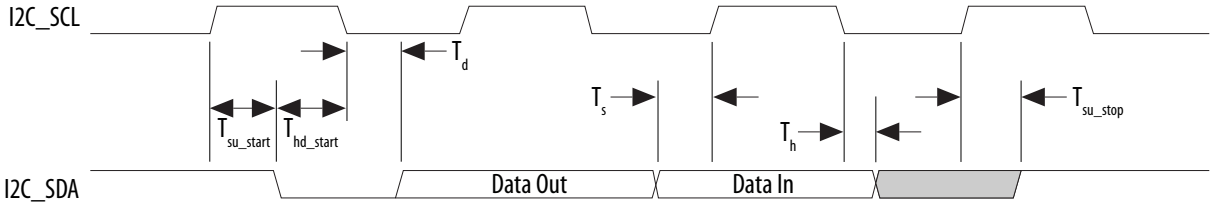
Figure 8. SPI Slave Timing Diagram



Related Information

SPI Controller, Cyclone V Hard Processor System Technical Reference Manual
Provides more information about `rx_sample_delay`.

Figure 14. I²C Timing Diagram



NAND Timing Characteristics

Table 52. NAND ONFI 1.0 Timing Requirements for Cyclone V Devices

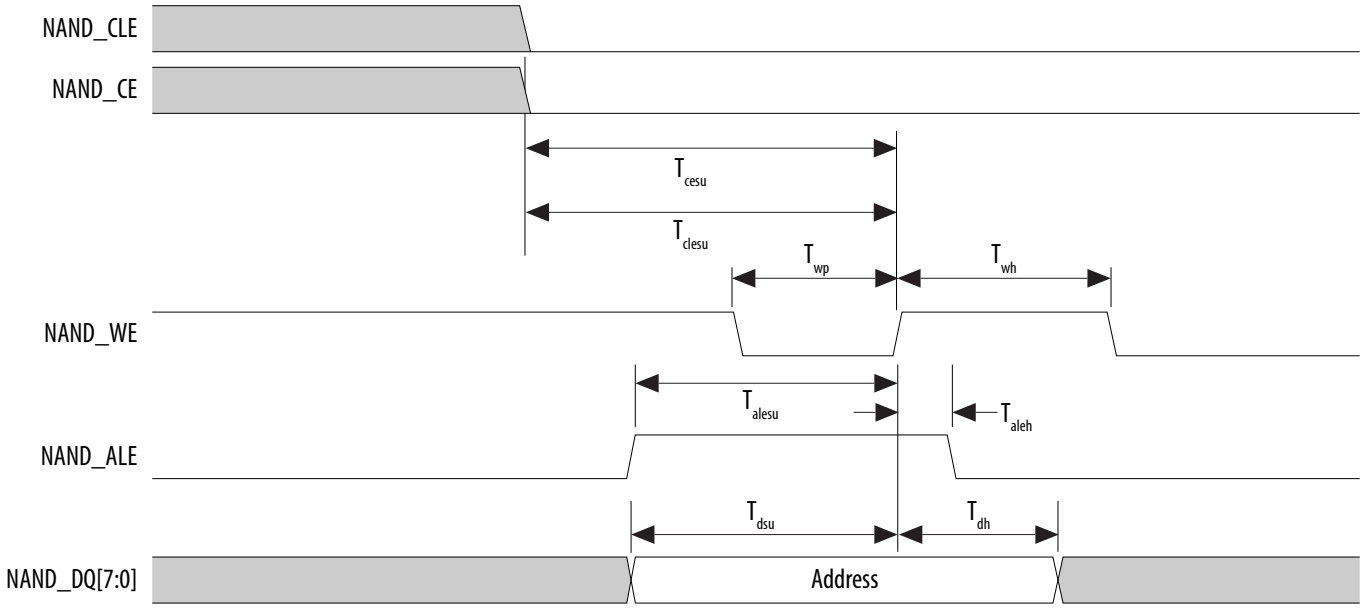
The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T_{wp} (72)	Write enable pulse width	10	—	ns
T_{wh} (72)	Write enable hold time	7	—	ns
T_{rp} (72)	Read enable pulse width	10	—	ns
T_{reh} (72)	Read enable hold time	7	—	ns
T_{clesu} (72)	Command latch enable to write enable setup time	10	—	ns
T_{cleh} (72)	Command latch enable to write enable hold time	5	—	ns
T_{cesu} (72)	Chip enable to write enable setup time	15	—	ns
T_{ceh} (72)	Chip enable to write enable hold time	5	—	ns
T_{alesu} (72)	Address latch enable to write enable setup time	10	—	ns
T_{aleh} (72)	Address latch enable to write enable hold time	5	—	ns
T_{dsu} (72)	Data to write enable setup time	10	—	ns
T_{dh} (72)	Data to write enable hold time	5	—	ns

continued...

(72) Timing of the NAND interface is controlled through the NAND configuration registers.

Figure 16. NAND Address Latch Timing Diagram



Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Cyclone V Devices table.

Table 58. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(77)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(78)	µs
t_{CF2CK}(79)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(79)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × $1/f_{MAX}$	—	s

continued...

(77) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

(78) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(79) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CL}	DCLK low time	0.45 × $1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(80)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

- FPP Configuration Timing
  Provides the FPP configuration timing waveforms.
- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 69

FPP Configuration Timing when DCLK-to-DATA[] >1

Table 59. FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(81)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(82)	µs

continued...

(80) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(81) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Programmable Output Buffer Delay

Table 69. Programmable Output Buffer Delay for Cyclone V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Intel Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

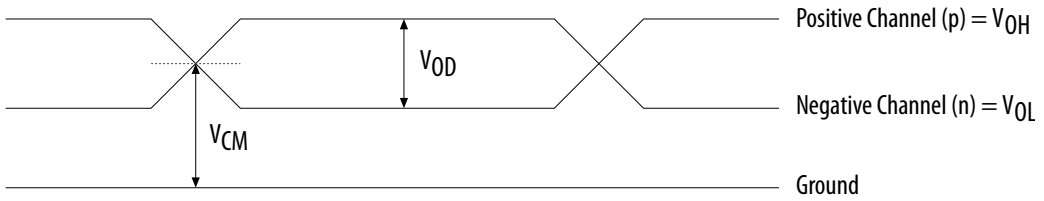
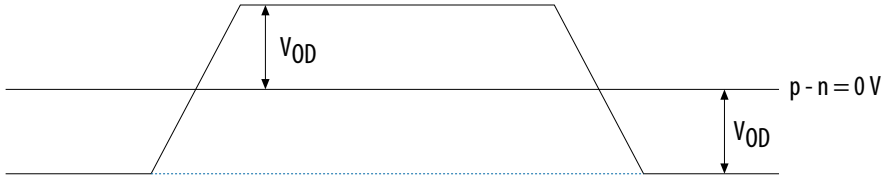
Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

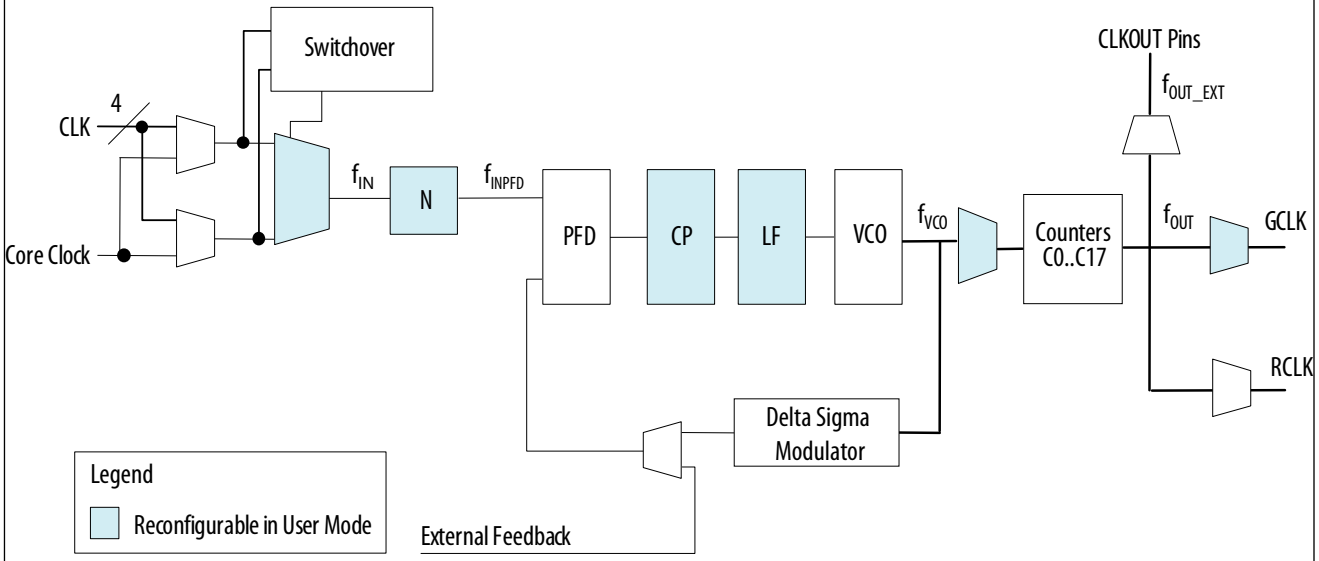
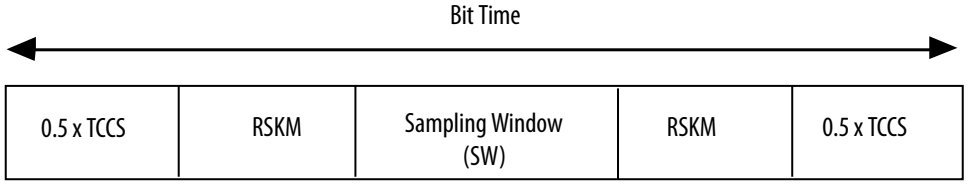
Table 70. Glossary

Term	Definition
Differential I/O standards	Receiver Input Waveforms

continued...

Term	Definition
	Single-Ended Waveform  **Differential Waveform** 
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} =1/TUI).
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG timing specifications	JTAG Timing Specifications

continued...

Term	Definition
	 Note: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.
R_L	Receiver differential input discrete resistor (external to the Cyclone V device).
Sampling window (SW)	Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 

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Document Revision History for Cyclone V Device Datasheet

Document Version	Changes
2018.05.07	• Added description about the low-power option ("L" suffix) for Cyclone V SE and SX devices. • Added the *Cyclone V Devices Overshoot Duration* diagram. • Removed the description on SD/MMC interface calibration support in the *Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices* table. This feature is currently supported in the preloader. • Removed the note to Cyclone V SE A2 and A4 devices, and Cyclone V SX C2 and C4 devices in the *Uncompressed .rbf Sizes for Cyclone V Devices* table. These devices are currently supported in the Intel Quartus Prime software. • Removed PowerPlay text from tool name. • Updated the IP name from ALTREMOTE_UPDATE to Remote Update Intel FPGA IP. • Rebranded as Intel. • Added the Low Power Variants table and the estimating power consumption steps to the "Cyclone V Device Datasheet" Overview section. • Updated the minimum value for t_{DH} to 2.5 for -6 speed grade/2.9 for -7 and -8 speed grade.

Date	Version	Changes
December 2016	2016.12.09	• Updated V_{ICM} (AC coupled) specifications for 1.5 V PCML in Receiver Specifications for Cyclone V GX, GT, SX, and ST Devices table. • Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Cyclone V Devices table. • Updated T_{init} specifications in the following tables: — FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices — FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices — AS Timing Parameters for AS ×1 and ×4 Configurations in Cyclone V Devices — PS Timing Parameters for Cyclone V Devices
June 2016	2016.06.10	• Changed pin capacitance to maximum values. • Updated SPI Master Timing Requirements for Cyclone V Devices table. — Added T_{su} and T_h specifications. — Removed T_{dinmax} specifications. • Updated SPI Master Timing Diagram. • Updated T_{clk} spec from maximum to minimum in I^2C Timing Requirements for Cyclone V Devices table.

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