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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 85K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csxfc5d6f31c8n



Transceiver Power Supply Operating Conditions

Table 5. Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices

Symbol	Description	Minimum ⁽⁸⁾	Typical	Maximum ⁽⁸⁾	Unit
V _{CCH_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V _{CCE_GXBL} ⁽⁹⁾⁽¹⁰⁾	Transmitter and receiver power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V
V _{CCL_GXBL} ⁽⁹⁾⁽¹⁰⁾	Clock network power (left side)	1.07/1.17	1.1/1.2	1.13/1.23	V

Related Information

- [PCIe Supported Configurations and Placement Guidelines](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.
- [6.144-Gbps Support Capability in Cyclone V GT Devices](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

⁽⁸⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁹⁾ Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for Cyclone V GT and ST FPGA systems which require full compliance to the PCIe Gen2 transmit jitter specification. For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices under this condition, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

⁽¹⁰⁾ Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.



Symbol	Description	Condition	Minimum ⁽¹¹⁾	Typical	Maximum ⁽¹¹⁾	Unit
		1.8 V	1.71	1.8	1.89	V
V _{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CC_AUX_SHARED} ⁽¹⁴⁾	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

[Recommended Operating Conditions](#) on page 8

Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based EPE and the Intel® Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- [Early Power Estimator User Guide](#)
Provides more information about power estimation tools.
- [Power Analysis chapter, Intel Quartus Prime Handbook](#)
Provides more information about power estimation tools.

⁽¹¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹⁴⁾ V_{CC_AUX_SHARED} must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.



Pin Capacitance

Table 12. Pin Capacitance for Cyclone V Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on left and right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 13. Hot Socketing Specifications for Cyclone V Devices

Symbol	Description	Maximum	Unit
I _{IOPIN} (DC)	DC current per I/O pin	300	μA
I _{IOPIN} (AC)	AC current per I/O pin	8 ⁽¹⁵⁾	mA
I _{XCVR-TX} (DC)	DC current per transceiver transmitter (TX) pin	100	mA
I _{XCVR-RX} (DC)	DC current per transceiver receiver (RX) pin	50	mA

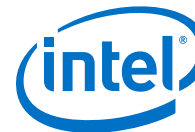
Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

⁽¹⁵⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C \, dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.



- [6.144-Gbps Support Capability in Cyclone V GT Devices](#)
Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.



Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting	Intel Quartus Prime V _{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

[SPICE Models for Intel Devices](#)

Provides the Cyclone V HSSI HSPICE models.



Protocol	Sub-protocol	Data Rate (Mbps)
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII ⁽⁵¹⁾	4,915.2
	CPRI E60LVII ⁽⁵¹⁾	6,144
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970
VbyOne	VbyOne 3750	3,750
HiGig+	HIGIG 3750	3,750

Related Information

- [PCIe Supported Configurations and Placement Guidelines](#)

Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.

⁽⁵¹⁾ For CPRI E48LVII and E60LVII, Intel recommends increasing the V_{CC_GXBL} and V_{CC_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144 Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.



DLL Frequency Range Specifications

Table 35. DLL Frequency Range Specifications for Cyclone V Devices

Parameter	-C6	-C7, -I7	-C8	Unit
DLL operating frequency range	167 – 400	167 – 400	167 – 333	MHz

DQS Logic Block Specifications

Table 36. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Cyclone V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	-C6	-C7, -I7	-C8	Unit
2	40	80	80	ps

Memory Output Clock Jitter Specifications

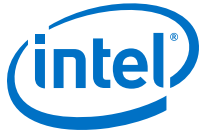
Table 37. Memory Output Clock Jitter Specifications for Cyclone V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma.

Intel recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Parameter	Clock Network	Symbol	-C6		-C7, -I7		-C8		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	-60	60	-70	70	-70	70	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	—	90	—	100	—	100	ps

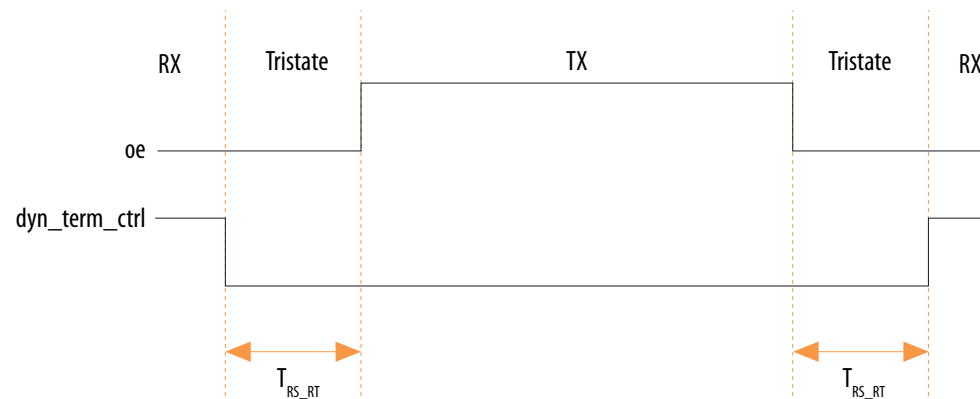


OCT Calibration Block Specifications

Table 38. OCT Calibration Block Specifications for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for R _S OCT/R _T OCT calibration	—	1000	—	Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R _S OCT and R _T OCT	—	2.5	—	ns

Figure 5. Timing Diagram for oe and dyn_term_ctrl Signals





Related Information

Quad SPI Flash Controller Chapter, Cyclone V Hard Processor System Technical Reference Manual

Provides more information about R_{delay} .

SPI Timing Characteristics

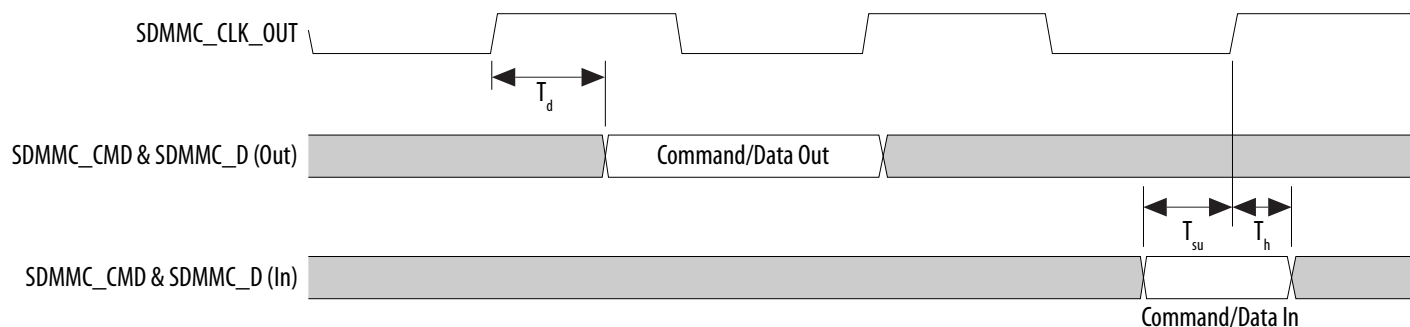
Table 44. SPI Master Timing Requirements for Cyclone V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 ⁽⁶⁹⁾	—	ns
T_{h}	SPI MISO hold time	1	—	ns
$T_{\text{dutycycle}}$	SPI_CLK duty cycle	45	55	%
T_{dssfrst}	Output delay SPI_SS valid before first clock edge	8	—	ns
T_{dsslst}	Output delay SPI_SS valid after last clock edge	8	—	ns
T_{dio}	Master-out slave-in (MOSI) output delay	-1	1	ns

⁽⁶⁹⁾ This value is based on $\text{rx_sample_dly} = 1$ and $\text{spi_m_clk} = 120$ MHz. spi_m_clk is the internal clock that is used by SPI Master to derive its SCLK_OUT. These timings are based on rx_sample_dly of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct rx_sample_dly value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about rx_sample_delay , refer to the *SPI Controller* chapter in the *Hard Processor System Technical Reference Manual*.

Figure 9. SD/MMC Timing Diagram



Related Information

[Booting and Configuration Chapter, Cyclone V Hard Processor System Technical Reference Manual](#)

Provides more information about CSEL pin settings in the *SD/MMC Controller CSEL Pin Settings* table.

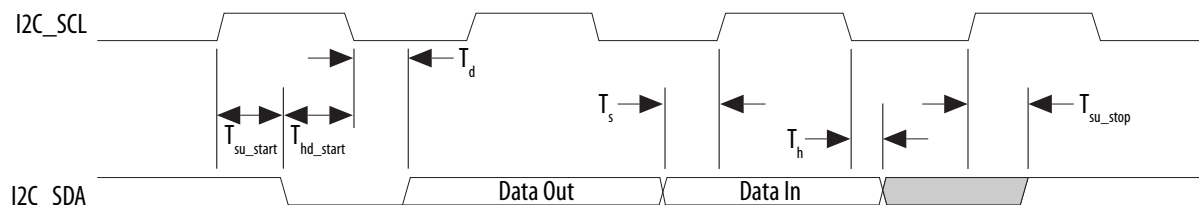
USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 47. USB Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	—	11	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 14. I²C Timing Diagram



NAND Timing Characteristics

Table 52. NAND ONFI 1.0 Timing Requirements for Cyclone V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
$T_{wp}^{(72)}$	Write enable pulse width	10	—	ns
$T_{wh}^{(72)}$	Write enable hold time	7	—	ns
$T_{rp}^{(72)}$	Read enable pulse width	10	—	ns
$T_{reh}^{(72)}$	Read enable hold time	7	—	ns
$T_{clesu}^{(72)}$	Command latch enable to write enable setup time	10	—	ns
$T_{cleh}^{(72)}$	Command latch enable to write enable hold time	5	—	ns
$T_{cesu}^{(72)}$	Chip enable to write enable setup time	15	—	ns
$T_{ceh}^{(72)}$	Chip enable to write enable hold time	5	—	ns
$T_{alesu}^{(72)}$	Address latch enable to write enable setup time	10	—	ns
$T_{aleh}^{(72)}$	Address latch enable to write enable hold time	5	—	ns
$T_{dsu}^{(72)}$	Data to write enable setup time	10	—	ns
$T_{dh}^{(72)}$	Data to write enable hold time	5	—	ns

continued...

(72) Timing of the NAND interface is controlled through the NAND configuration registers.



Symbol	Description	Min	Max	Unit
t _{JPCO}	JTAG port clock to output	—	11 ⁽⁷⁶⁾	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁷⁶⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁷⁶⁾	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP $\times 16$ where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Cyclone V devices use additional clock cycles to decrypt and decompress the configuration data. If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio - 1) clock cycles after the last data is latched into the Cyclone V device.

Table 57. DCLK-to-DATA[] Ratio for Cyclone V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1

continued...

⁽⁷⁶⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.



Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Cyclone V Devices table.

Table 58. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μs
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁷⁷⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽⁷⁸⁾	μs
t _{CF2CK} ⁽⁷⁹⁾	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽⁷⁹⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	0.45 × 1/f _{MAX}	—	s

continued...

⁽⁷⁷⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

⁽⁷⁸⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽⁷⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.



Configuration Files

Table 64. Uncompressed .rbf Sizes for Cyclone V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.tbf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (.rbf) size is specifically for the Configuration via Protocol (CvP) feature.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device ⁽⁹⁴⁾
Cyclone V E ⁽⁹⁵⁾	A2	21,061,280	275,608	EPCQ64
	A4	21,061,280	275,608	EPCQ64
	A5	33,958,560	322,072	EPCQ128
	A7	56,167,552	435,288	EPCQ128
	A9	102,871,776	400,408	EPCQ256
Cyclone V GX	C3	14,510,912	320,280	EPCQ32
	C4	33,958,560	322,072	EPCQ128
	C5	33,958,560	322,072	EPCQ128
	C7	56,167,552	435,288	EPCQ128
	C9	102,871,776	400,408	EPCQ256
Cyclone V GT	D5	33,958,560	322,072	EPCQ128
	D7	56,167,552	435,288	EPCQ128
	D9	102,871,776	400,408	EPCQ256
Cyclone V SE ⁽⁹⁵⁾	A2	33,958,560	322,072	EPCQ128

continued...

⁽⁹⁴⁾ The recommended EPCQ serial configuration devices are able to store more than one image.

⁽⁹⁵⁾ No PCIe hard IP, configuration via protocol (CvP) is not supported in this family.



Variant	Member Code	Active Serial ⁽⁹⁶⁾			Fast Passive Parallel ⁽⁹⁷⁾		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Cyclone V GX	A9	4	100	257	16	125	51
	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
Cyclone V GT	C9	4	100	257	16	125	51
	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
Cyclone V SE	D9	4	100	257	16	125	51
	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
Cyclone V SX	A6	4	100	140	16	125	28
	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
Cyclone V ST	C6	4	100	140	16	125	28
	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

⁽⁹⁶⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽⁹⁷⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Cyclone V I/O Timing Spreadsheet](#)

Provides the Cyclone V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Table 68. I/O element (IOE) Programmable Delay for Cyclone V Devices

Parameter ⁽¹⁰⁰⁾	Available Settings	Minimum Offset ⁽¹⁰¹⁾	Fast Model		Slow Model					Unit
			Industrial	Commercial	-C6	-C7	-C8	-I7	-A7	
D1	32	0	0.508	0.517	0.971	1.187	1.194	1.179	1.160	ns
D3	8	0	1.761	1.793	3.291	4.022	3.961	3.999	3.929	ns
D4	32	0	0.510	0.519	1.180	1.187	1.195	1.180	1.160	ns
D5	32	0	0.508	0.517	0.970	1.186	1.194	1.179	1.179	ns

⁽¹⁰⁰⁾ You can set this value in the Intel Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹⁰¹⁾ Minimum offset does not include the intrinsic delay.



Term	Definition
Single-ended voltage referenced I/O standard	<p>The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.</p> <p>Single-Ended Voltage Referenced I/O Standard</p>
t_c	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input

continued...



Document Revision History for Cyclone V Device Datasheet

Document Version	Changes
2018.05.07	<ul style="list-style-type: none"> Added description about the low-power option ("L" suffix) for Cyclone V SE and SX devices. Added the <i>Cyclone V Devices Overshoot Duration</i> diagram. Removed the description on SD/MMC interface calibration support in the <i>Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices</i> table. This feature is currently supported in the preloader. Removed the note to Cyclone V SE A2 and A4 devices, and Cyclone V SX C2 and C4 devices in the <i>Uncompressed .rbf Sizes for Cyclone V Devices</i> table. These devices are currently supported in the Intel Quartus Prime software. Removed PowerPlay text from tool name. Updated the IP name from ALTREMOTE_UPDATE to Remote Update Intel FPGA IP. Rebranded as Intel. Added the Low Power Variants table and the estimating power consumption steps to the "Cyclone V Device Datasheet" Overview section. Updated the minimum value for t_{DH} to 2.5 for -6 speed grade/2.9 for -7 and -8 speed grade.

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December 2016	2016.12.09	<ul style="list-style-type: none"> Updated V_{ICM} (AC coupled) specifications for 1.5 V PCML in Receiver Specifications for Cyclone V GX, GT, SX, and ST Devices table. Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Cyclone V Devices table. Updated T_{init} specifications in the following tables: <ul style="list-style-type: none"> FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices AS Timing Parameters for AS $\times 1$ and $\times 4$ Configurations in Cyclone V Devices PS Timing Parameters for Cyclone V Devices
June 2016	2016.06.10	<ul style="list-style-type: none"> Changed pin capacitance to maximum values. Updated SPI Master Timing Requirements for Cyclone V Devices table. <ul style="list-style-type: none"> Added T_{su} and T_h specifications. Removed T_{dinmax} specifications. Updated SPI Master Timing Diagram. Updated T_{clk} spec from maximum to minimum in I²C Timing Requirements for Cyclone V Devices table.

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January 2015	2015.01.23	<ul style="list-style-type: none"> • Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps. Updated the note in the following tables: <ul style="list-style-type: none"> – Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices – Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices – Transceiver Compliance Specification for All Supported Protocol for Cyclone V Devices • Updated the description for $V_{CC_AUX_SHARED}$ to "HPS auxiliary power supply". Added a note to state that $V_{CC_AUX_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices. Updated in the following tables: <ul style="list-style-type: none"> – Absolute Maximum Ratings for Cyclone V Devices – HPS Power Supply Operating Conditions for Cyclone V SE, SX, and ST Devices • Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. • Updated the conditions for transceiver reference clock rise time and fall time: Measure at ± 60 mV of differential signal. Added a note to the conditions: $REFCLK$ performance requires to meet transmitter $REFCLK$ phase noise specification. • Updated f_{VCO} maximum value from 1400 MHz to 1600 MHz for -C7 and -I7 speed grades in the PLL specifications table. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Added the following notes in the High-Speed I/O Specifications for Cyclone V Devices table: <ul style="list-style-type: none"> – The Cyclone V devices support true RSDS output standard with data rates of up to 230 Mbps using true LVDS output buffer types on all I/O banks. – The Cyclone V devices support true mini-LVDS output standard with data rates of up to 340 Mbps using true LVDS output buffer types on all I/O banks. • Updated HPS Clock Performance <code>main_base_clk</code> specifications from 462 MHz to 400 MHz for -C6 speed grade. • Updated HPS PLL VCO maximum frequency to 1,600 MHz (for -C7, -I7, -A7, and -C8 speed grades) and 1,850 MHz (for -C6 speed grade). • Changed the symbol for HPS PLL input jitter divide value from NR to N. • Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables: <ul style="list-style-type: none"> – SPI Master Timing Requirements for Cyclone V Devices – SPI Slave Timing Requirements for Cyclone V Devices • Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board. • Added HPS JTAG timing specifications. • Updated the configuration <code>.rbf</code> size (bits) for Cyclone V devices. • Added a note to Uncompressed <code>.rbf</code> Sizes for Cyclone V Devices table: The recommended EPCQ serial configuration devices are able to store more than one image.
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June 2013	3.4	<ul style="list-style-type: none"> • Updated Table 20, Table 27, and Table 34. • Updated "UART Interface" and "CAN Interface" sections. • Removed the following tables: <ul style="list-style-type: none"> — Table 45: UART Baud Rate for Cyclone V Devices — Table 47: CAN Pulse Width for Cyclone V Devices
May 2013	3.3	<ul style="list-style-type: none"> • Added Table 33. • Updated Figure 5, Figure 6, Figure 17, Figure 19, and Figure 20. • Updated Table 1, Table 4, Table 5, Table 10, Table 13, Table 19, Table 20, Table 26, Table 32, Table 35, Table 36, Table 43, Table 53, Table 54, Table 57, and Table 61.
March 2013	3.2	<ul style="list-style-type: none"> • Added HPS reset information in the "HPS Specifications" section. • Added Table 57. • Updated Table 1, Table 2, Table 17, Table 20, Table 52, and Table 56. • Updated Figure 18.
January 2013	3.1	Updated Table 4, Table 20, and Table 56.
November 2012	3.0	<ul style="list-style-type: none"> • Updated Table 1, Table 4, Table 5, Table 9, Table 14, Table 16, Table 17, Table 19, Table 20, Table 25, Table 28, Table 52, Table 55, Table 56, and Table 59. • Removed table: Transceiver Block Jitter Specifications for Cyclone V GX Devices. • Added HPS information: <ul style="list-style-type: none"> — Added "HPS Specifications" section. — Added Table 33, Table 34, Table 35, Table 36, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, and Table 46. — Added Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, and Figure 16. — Updated Table 3.
June 2012	2.0	<p>Updated for the Quartus Prime software v12.0 release:</p> <ul style="list-style-type: none"> • Restructured document. • Removed "Power Consumption" section. • Updated Table 1, Table 3, Table 19, Table 20, Table 25, Table 27, Table 28, Table 30, Table 31, Table 34, Table 36, Table 37, Table 38, Table 39, Table 41, Table 43, and Table 46. • Added Table 22, Table 23, and Table 29. • Added Figure 1 and Figure 2. • Added "Initialization" and "Configuration Files" sections.

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