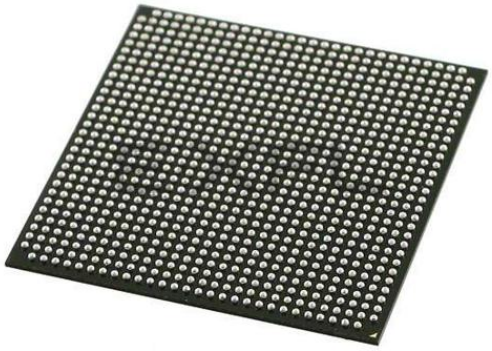


Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	925MHz
Primary Attributes	FPGA - 110K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csxfc6d6f31c6n

Density	Ordering Part Number (OPN)	Static Power Reduction
110K LE	5CSEBA6U19I7LN	
	5CSEBA6U23I7LN	
	5CSXFC6C6U23I7LN	

To estimate total power consumption for a low-power device, listed in Table 1 on page 3:

1. Multiply the Total Static Power reported by the Early Power Estimator (EPE) by the appropriate scale factor:
   - For 25K LE and 40K LE devices, use 0.7
   - For 85K LE and 110K LE devices, use 0.8
2. Add the result from Step 1 on page 4 to the Total Dynamic Power reported by the EPE.

Related Information

Cyclone V Device Overview
Provides more information about the densities and packages of devices in the Cyclone V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Cyclone V devices.

Operating Conditions

Cyclone V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Cyclone V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Cyclone V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2. Absolute Maximum Ratings for Cyclone V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.5	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO}	I/O power supply	–0.5	3.90	V
V_{CCA_FPLL}	Phase-locked loop (PLL) analog power supply	–0.5	3.25	V
V_{CCH_GXB}	Transceiver high voltage power	–0.5	3.25	V
V_{CCE_GXB}	Transceiver power	–0.5	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.5	1.50	V
V_I	DC input voltage	–0.5	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.5	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.5	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.5	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.5	3.90	V
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.5	3.25	V
$V_{CC\_AUX\_SHARED}$ (1)	HPS auxiliary power supply	–0.5	3.25	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

(1) $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[19] (mA)	I_{OH}[19] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO}+ 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

(19) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[21]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[22]			V_{OCM} (V)[22][23]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL[29]	—	—	—	300	—	—	0.60	D_{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D_{MAX} > 700 Mbps	1.60						
SLVS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
Sub-LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
HiSpi	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—

Related Information

- AN522: Implementing Bus LVDS Interface in Supported Intel Device Families
  Provides more information about BLVDS interface support in Intel devices.
- Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices on page 25
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Cyclone V core and periphery blocks.

(21) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(22) R_L range: 90 ≤ R_L ≤ 110 Ω.

(23) This applies to default pre-emphasis setting only.

(29) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Transceiver Performance Specifications

Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Table 21. Reference Clock Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL[31], HCSL, and LVDS										
Input frequency from REFCLK input pins[32]	—	27	—	550	27	—	550	27	—	550	MHz
Rise time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal[33]	—	—	400	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCIe	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω

continued...

(30) Transceiver Speed Grade 5 covers specifications for Cyclone V GT and ST devices.

(31) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(32) The reference clock frequency must be ≥ 307.2 MHz to be fully compliance to CPRI transmit jitter specification at 6.144 Gbps. For more information about CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

(33) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

Table 22. Transceiver Clocks Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	100/125[37]	75	—	100/125[37]	75	—	100/125[37]	MHz

Table 23. Receiver Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS										
Data rate[38]	—	614	—	5000/6144[35]	614	—	3125	614	—	2500	Mbps
Absolute V_{MAX} for a receiver pin[39]	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	—	—	2.2	V

continued...

(37) The maximum supported clock frequency is 100 MHz if the PCIe hard IP block is enabled or 125 MHz if the PCIe hard IP block is not enabled.

(38) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

(39) The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Intra-differential pair skew	TX V_{CM} = 0.65 V and slew rate of 15 ps	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode	—	—	180	—	—	180	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew	×*N* PMA bonded mode	—	—	500	—	—	500	—	—	500	ps

Table 25. CMU PLL Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported data range	—	614	—	5000/6144[35]	614	—	3125	614	—	2500	Mbps
fPLL supported data range	—	614	—	3125	614	—	3125	614	—	2500	Mbps

Table 26. Transceiver-FPGA Fabric Interface Specifications for Cyclone V GX, GT, SX, and ST Devices

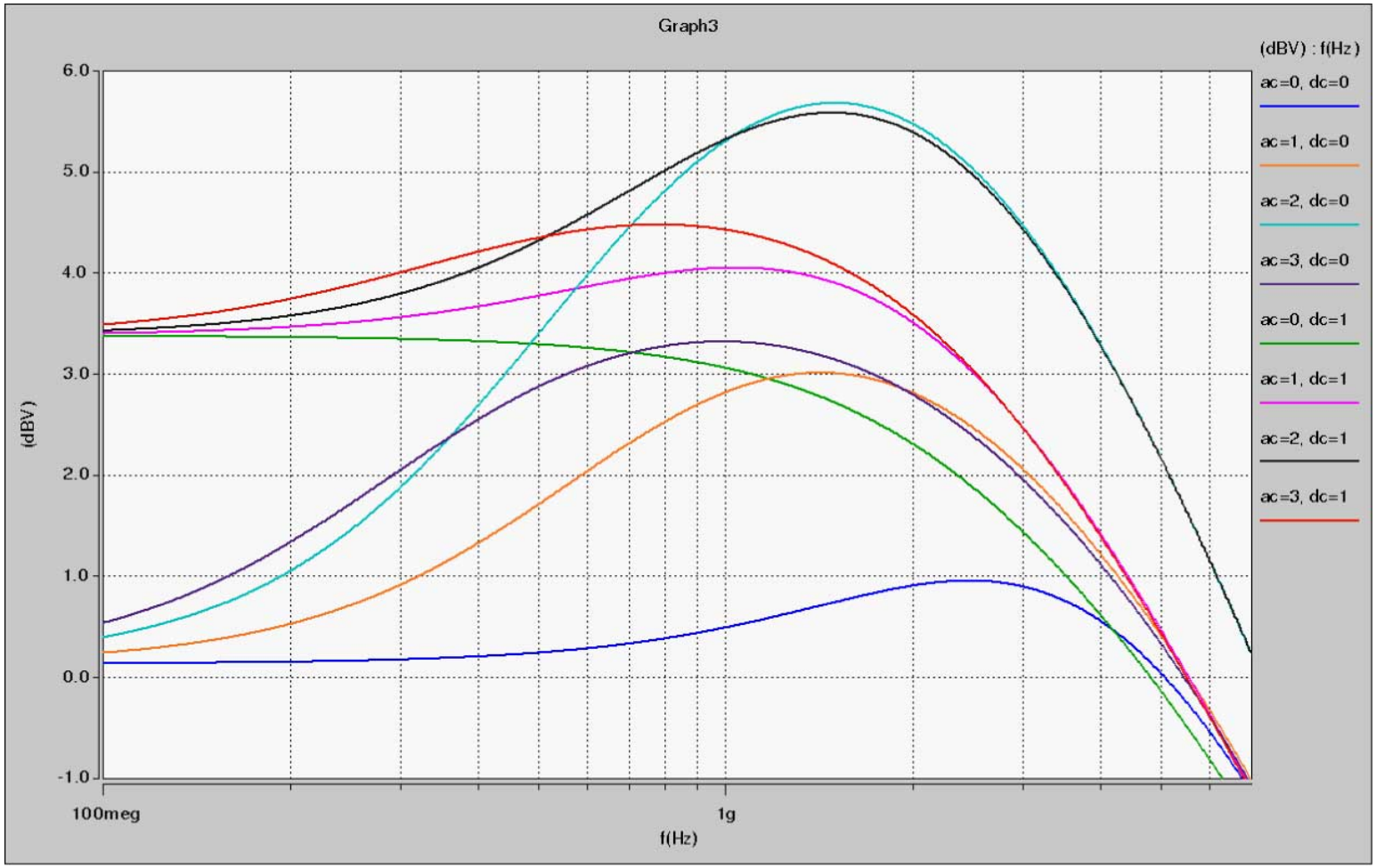
Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Interface speed (single-width mode)	—	25	—	187.5	25	—	187.5	25	—	163.84	MHz
Interface speed (double-width mode)	—	25	—	163.84	25	—	163.84	25	—	156.25	MHz

Related Information

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 32
- CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain on page 33
- PCIe Supported Configurations and Placement Guidelines
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 4. CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices



Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

Table 27. Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting[48]	V_{OD} Value (mV)	V_{OD} Setting[48]	V_{OD} Value (mV)
V_{OD} differential peak-to-peak typical	6[49]	120	34	680
	7[49]	140	35	700
	8[49]	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

continued...

(48) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

(49) Only valid for data rates ≤ 5 Gbps.

- 6.144-Gbps Support Capability in Cyclone V GT Devices
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps.

Core Performance Specifications

Clock Tree Specifications

Table 30. Clock Tree Specifications for Cyclone V Devices

Parameter	Performance			Unit
	–C6	–C7, –I7	–C8, –A7	
Global clock and Regional clock	550	550	460	MHz
Peripheral clock	155	155	155	MHz

PLL Specifications

Table 31. PLL Specifications for Cyclone V Devices

This table lists the Cyclone V PLL block specifications. Cyclone V PLL block does not include HPS PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–C6 speed grade	5	—	670(52)	MHz
		–C7, –I7 speed grades	5	—	622(52)	MHz
		–C8, –A7 speed grades	5	—	500(52)	MHz
f_{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	—	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	—	50	—	160	MHz
f_{VCO}(53)	PLL voltage-controlled oscillator (VCO) operating range	–C6, –C7, –I7 speed grades	600	—	1600	MHz

continued...

(52) This specification is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		Emulated Differential I/O Standards										
	t_{RISE} and t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
	TCCS	True Differential I/O Standards	—	—	200	—	—	250	—	—	250	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	300	—	—	300	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
Receiver	f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	875(67)	(65)	—	840(67)	(65)	—	640(67)	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
Sampling Window		—	—	—	350	—	—	350	—	—	350	ps

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 41. HPS PLL VCO Frequency Range for Cyclone V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C7, –I7, –A7, –C8	320	1,600	MHz
	–C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 42. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

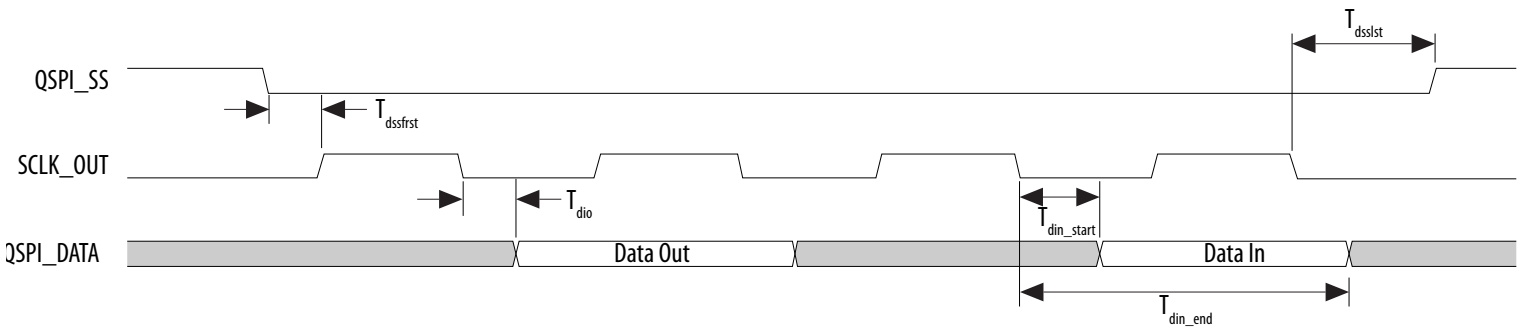
Quad SPI Flash Timing Characteristics

Table 43. Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (68)	ns
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (68)	—	—	ns

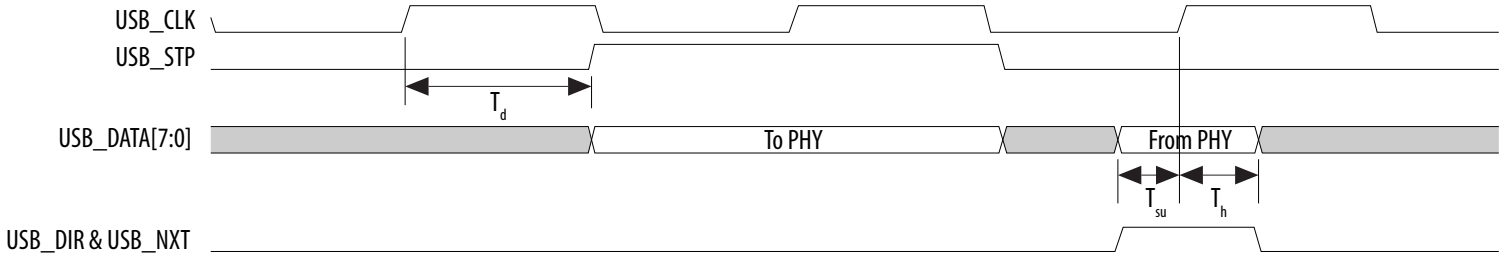
Figure 6. Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



(68) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Intel provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the *Quad SPI Flash Controller chapter in the Cyclone V Hard Processor System Technical Reference Manual*.

Figure 10. USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 48. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$	TX_CLK duty cycle	45	—	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	–0.85	—	0.15	ns

Figure 11. RGMII TX Timing Diagram

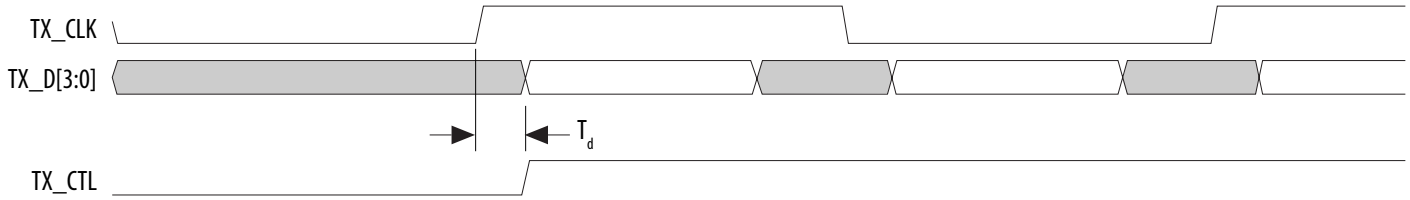
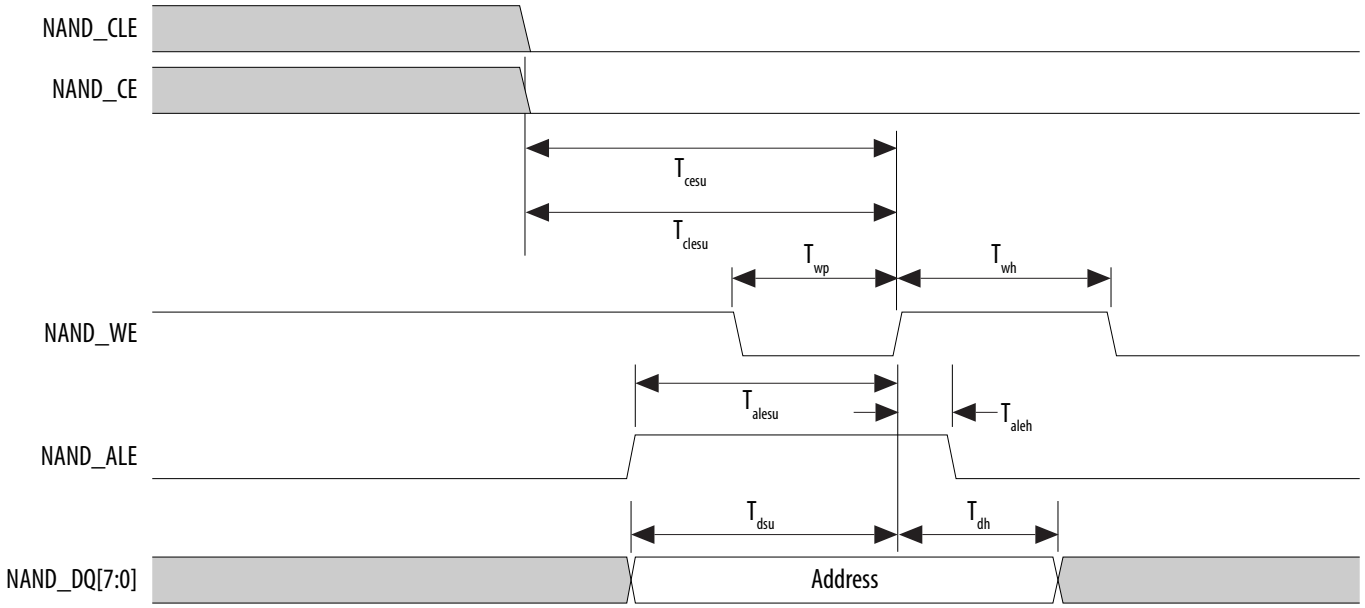


Figure 16. NAND Address Latch Timing Diagram



CAN Interface

The maximum controller area network (CAN) data rate is 1 Mbps.

HPS JTAG Timing Specifications

Table 54. HPS JTAG Timing Parameters and Values for Cyclone V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12(73)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14(73)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14(73)	ns

Configuration Specifications

This section provides configuration specifications and timing for Cyclone V devices.

(73) A 1-ns adder is required for each $V_{CCIO\ \_HPS}$ voltage step down from 3.0 V. For example, t_{JPCO}= 13 ns if $V_{CCIO\ \_HPS}$ of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

Symbol	Parameter	Minimum	Maximum	Unit
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × 1/f_{MAX}	—	s
t_{CL}	DCLK low time	0.45 × 1/f_{MAX}	—	s
t_{CLK}	DCLK period	1/f_{MAX}	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(92)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

Initialization

Table 63. Initialization Clock Source Option and the Maximum Frequency for Cyclone V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T_{init}
CLKUSR(93)	PS and FPP	125	
	AS	100	
DCLK	PS and FPP	125	

(92) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(93) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Intel Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Configuration Files

Table 64. Uncompressed .rbf Sizes for Cyclone V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (`.rbf`) size is specifically for the Configuration via Protocol (CvP) feature.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device(94)
Cyclone V E (95)	A2	21,061,280	275,608	EPCQ64
	A4	21,061,280	275,608	EPCQ64
	A5	33,958,560	322,072	EPCQ128
	A7	56,167,552	435,288	EPCQ128
	A9	102,871,776	400,408	EPCQ256
Cyclone V GX	C3	14,510,912	320,280	EPCQ32
	C4	33,958,560	322,072	EPCQ128
	C5	33,958,560	322,072	EPCQ128
	C7	56,167,552	435,288	EPCQ128
	C9	102,871,776	400,408	EPCQ256
Cyclone V GT	D5	33,958,560	322,072	EPCQ128
	D7	56,167,552	435,288	EPCQ128
	D9	102,871,776	400,408	EPCQ256
Cyclone V SE (95)	A2	33,958,560	322,072	EPCQ128

continued...

(94) The recommended EPCQ serial configuration devices are able to store more than one image.

(95) No PCIe hard IP, configuration via protocol (CvP) is not supported in this family.

Variant	Member Code	Active Serial[96]			Fast Passive Parallel[97]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A9	4	100	257	16	125	51
Cyclone V GX	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
June 2013	3.4	• Updated Table 20, Table 27, and Table 34. • Updated "UART Interface" and "CAN Interface" sections. • Removed the following tables: — Table 45: UART Baud Rate for Cyclone V Devices — Table 47: CAN Pulse Width for Cyclone V Devices
May 2013	3.3	• Added Table 33. • Updated Figure 5, Figure 6, Figure 17, Figure 19, and Figure 20. • Updated Table 1, Table 4, Table 5, Table 10, Table 13, Table 19, Table 20, Table 26, Table 32, Table 35, Table 36, Table 43, Table 53, Table 54, Table 57, and Table 61.
March 2013	3.2	• Added HPS reset information in the "HPS Specifications" section. • Added Table 57. • Updated Table 1, Table 2, Table 17, Table 20, Table 52, and Table 56. • Updated Figure 18.
January 2013	3.1	Updated Table 4, Table 20, and Table 56.
November 2012	3.0	• Updated Table 1, Table 4, Table 5, Table 9, Table 14, Table 16, Table 17, Table 19, Table 20, Table 25, Table 28, Table 52, Table 55, Table 56, and Table 59. • Removed table: Transceiver Block Jitter Specifications for Cyclone V GX Devices. • Added HPS information: — Added "HPS Specifications" section. — Added Table 33, Table 34, Table 35, Table 36, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, and Table 46. — Added Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, and Figure 16. — Updated Table 3.
June 2012	2.0	Updated for the Quartus Prime software v12.0 release: • Restructured document. • Removed "Power Consumption" section. • Updated Table 1,Table 3, Table 19, Table 20, Table 25, Table 27, Table 28, Table 30, Table 31, Table 34, Table 36, Table 37, Table 38, Table 39, Table 41, Table 43, and Table 46. • Added Table 22, Table 23, and Table 29. • Added Figure 1 and Figure 2. • Added "Initialization" and "Configuration Files" sections.

continued...