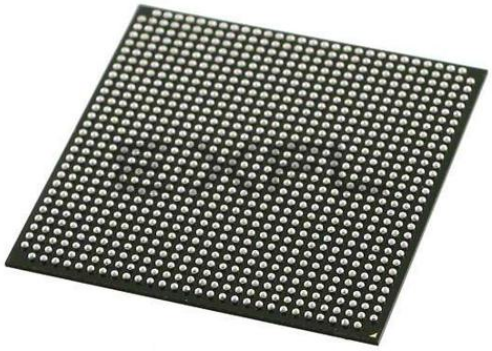


Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	600MHz
Primary Attributes	FPGA - 110K Logic Elements
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csxfc6d6f31c8n

Contents

Cyclone V Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Cyclone® V devices.

Cyclone V devices are offered in commercial and industrial grades. Commercial devices are offered in –C6 (fastest), –C7, and –C8 speed grades. Industrial grade devices are offered in the –I7 speed grade. Automotive devices are offered in the –A7 speed grade.

Cyclone V SoC devices are also offered in a low-power variant, as indicated by the L power option in the device part number. These devices have 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE. Note that the L power option devices are only available in –I7 speed grade, and have the equivalent operating conditions and timing specifications as the standard –I7 speed grade devices.

Table 1. Low Power Variants

Density	Ordering Part Number (OPN)	Static Power Reduction
25K LE	5CSEBA2U19I7LN	30%
	5CSEBA2U23I7LN	
	5CSXFC2C6U23I7LN	
40K LE	5CSEBA4U19I7LN	
	5CSEBA4U23I7LN	
	5CSXFC4C6U23I7LN	
85K LE	5CSEBA5U19I7LN	20%
	5CSEBA5U23I7LN	
	5CSXC5C6U23I7LN	

continued...

Symbol	Description	Condition	Minimum(11)	Typical	Maximum(11)	Unit
		1.8 V	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
$V_{CC\_AUX\_SHARED}$(14)	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

Recommended Operating Conditions on page 8
Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based EPE and the Intel® Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Handbook
  Provides more information about power estimation tools.

(11) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(14) $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.

Pin Capacitance

Table 12. Pin Capacitance for Cyclone V Devices

Symbol	Description	Maximum	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on left and right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 13. Hot Socketing Specifications for Cyclone V Devices

Symbol	Description	Maximum	Unit
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300	µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8(15)	mA
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter (TX) pin	100	mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

(15) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Differential I/O Standard Specifications

Table 20. Differential I/O Standard Specifications for Cyclone V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[21]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[22]			V_{OCM} (V)[22][23]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to *Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices* table.														
2.5 V LVDS[24]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	D_{MAX} ≤ 700 Mbps	1.80	0.247	—	0.6	1.125	1.25	1.375
							1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS[25][26]	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO)[27]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)[28]	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4

continued...

(21) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(22) R_L range: 90 ≤ R_L ≤ 110 Ω.

(23) This applies to default pre-emphasis setting only.

(24) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rate above 700 Mbps and 0.00 V to 1.85 V for data rate below 700 Mbps.

(25) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

(26) For more information about BLVDS interface support in Intel devices, refer to *AN522: Implementing Bus LVDS Interface in Supported Intel Device Families*.

(27) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

(28) For optimized mini-LVDS receiver performance, the receiver voltage input range must be within 0.300 V to 1.425 V.

Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

Table 27. Typical TX V_{OD} Setting for Cyclone V Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting[48]	V_{OD} Value (mV)	V_{OD} Setting[48]	V_{OD} Value (mV)
V_{OD} differential peak-to-peak typical	6[49]	120	34	680
	7[49]	140	35	700
	8[49]	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

continued...

(48) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

(49) Only valid for data rates ≤ 5 Gbps.

Protocol	Sub-protocol	Data Rate (Mbps)
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII(51)	4,915.2
	CPRI E60LVII(51)	6,144
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970
VbyOne	VbyOne 3750	3,750
HiGig+	HIGIG 3750	3,750

Related Information

- PCIe Supported Configurations and Placement Guidelines
  Provides more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices which require full compliance to the PCIe Gen2 transmit jitter specification.

(51) For CPRI E48LVII and E60LVII, Intel recommends increasing the V_{CCE_GXBL} and V_{CCL_GXBL} typical value from 1.1 V to 1.2 V for full compliance to CPRI transmit jitter specification at 4.9152 Gbps (Cyclone V GT and ST devices) and 6.144 Gbps (Cyclone V GT and ST devices only). For more information about the maximum full duplex channels recommended in Cyclone V GT and ST devices for CPRI 6.144 Gbps, refer to the *Transceiver Protocol Configurations in Cyclone V Devices* chapter.

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		Emulated Differential I/O Standards										
	t_{RISE} and t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
	TCCS	True Differential I/O Standards	—	—	200	—	—	250	—	—	250	ps
		Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	300	—	—	300	—	—	300	ps
		Emulated Differential I/O Standards with One External Output Resistor Network	—	—	300	—	—	300	—	—	300	ps
Receiver	f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	875(67)	(65)	—	840(67)	(65)	—	640(67)	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	(65)	—	(66)	(65)	—	(66)	(65)	—	(66)	Mbps
Sampling Window		—	—	—	350	—	—	350	—	—	350	ps

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 41. HPS PLL VCO Frequency Range for Cyclone V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C7, –I7, –A7, –C8	320	1,600	MHz
	–C6	320	1,850	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 42. Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

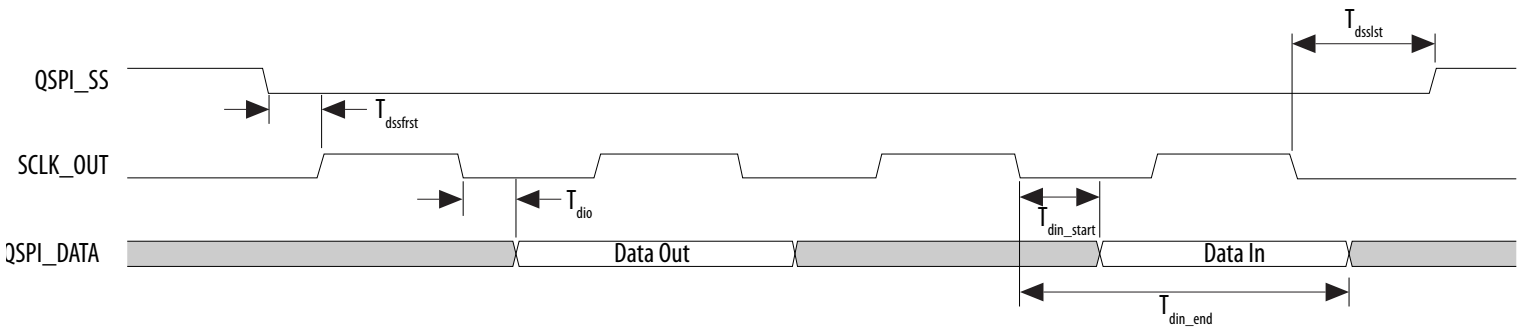
Quad SPI Flash Timing Characteristics

Table 43. Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (68)	ns
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (68)	—	—	ns

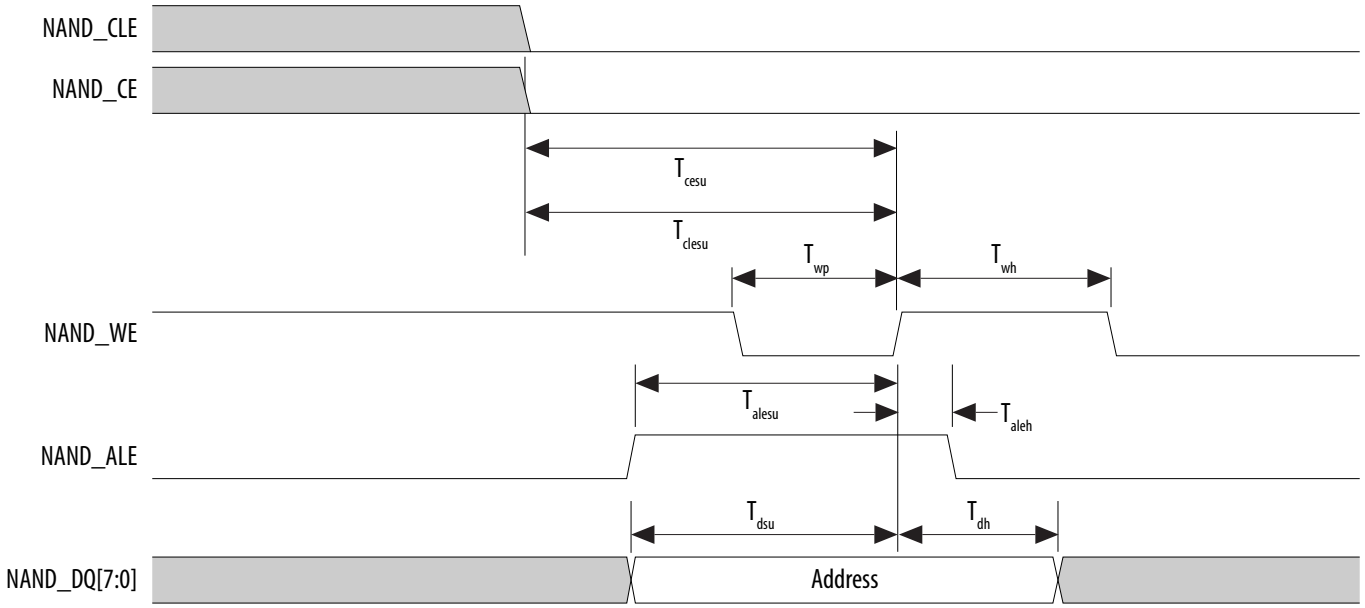
Figure 6. Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



(68) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Intel provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the *Quad SPI Flash Controller chapter in the Cyclone V Hard Processor System Technical Reference Manual*.

Figure 16. NAND Address Latch Timing Diagram



Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Cyclone V Devices table.

Table 58. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(77)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(78)	µs
t_{CF2CK}(79)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(79)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × $1/f_{MAX}$	—	s

continued...

(77) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

(78) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(79) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Configuration Files

Table 64. Uncompressed .rbf Sizes for Cyclone V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (`.rbf`) size is specifically for the Configuration via Protocol (CvP) feature.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device(94)
Cyclone V E (95)	A2	21,061,280	275,608	EPCQ64
	A4	21,061,280	275,608	EPCQ64
	A5	33,958,560	322,072	EPCQ128
	A7	56,167,552	435,288	EPCQ128
	A9	102,871,776	400,408	EPCQ256
Cyclone V GX	C3	14,510,912	320,280	EPCQ32
	C4	33,958,560	322,072	EPCQ128
	C5	33,958,560	322,072	EPCQ128
	C7	56,167,552	435,288	EPCQ128
	C9	102,871,776	400,408	EPCQ256
Cyclone V GT	D5	33,958,560	322,072	EPCQ128
	D7	56,167,552	435,288	EPCQ128
	D9	102,871,776	400,408	EPCQ256
Cyclone V SE (95)	A2	33,958,560	322,072	EPCQ128

continued...

(94) The recommended EPCQ serial configuration devices are able to store more than one image.

(95) No PCIe hard IP, configuration via protocol (CvP) is not supported in this family.

Variant	Member Code	Active Serial[96]			Fast Passive Parallel[97]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A9	4	100	257	16	125	51
Cyclone V GX	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Cyclone V I/O Timing Spreadsheet
Provides the Cyclone V Excel-based I/O timing spreadsheet.

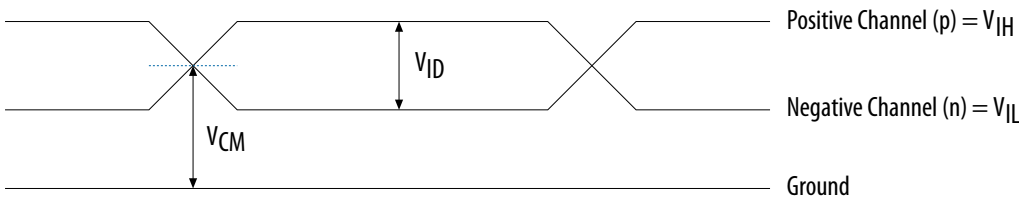
Programmable IOE Delay

Table 68. I/O element (IOE) Programmable Delay for Cyclone V Devices

Parameter[100]	Available Settings	Minimum Offset[101]	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C6	–C7	–C8	–I7	–A7	
D1	32	0	0.508	0.517	0.971	1.187	1.194	1.179	1.160	ns
D3	8	0	1.761	1.793	3.291	4.022	3.961	3.999	3.929	ns
D4	32	0	0.510	0.519	1.180	1.187	1.195	1.180	1.160	ns
D5	32	0	0.508	0.517	0.970	1.186	1.194	1.179	1.179	ns

(100) You can set this value in the Intel Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

(101) Minimum offset does not include the intrinsic delay.

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms

continued...

Date	Version	Changes
December 2015	2015.12.04	• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices table. — Updated F_{clk}, $T_{dutycycle}$, and $T_{dssfrst}$ specifications. — Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications. — Removed T_{dinmax} specifications. • Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Cyclone V Devices table. • Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices table. — Updated T_{clk} to $T_{sdmmc\_clk\_out}$ symbol. — Updated $T_{sdmmc\_clk\_out}$ and T_d specifications. — Added T_{sdmmc_clk}, T_{su}, and T_h specifications. — Removed T_{dinmax} specifications. • Updated the following diagrams: — Quad SPI Flash Timing Diagram — SD/MMC Timing Diagram • Updated configuration .rbf sizes for Cyclone V devices. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Updated the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Cyclone V Devices table: — True RSDS output standard: data rates of up to 360 Mbps — True mini-LVDS output standard: data rates of up to 400 Mbps • Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash. • Updated T_h location in I^2C Timing Diagram. • Updated T_{wp} location in NAND Address Latch Timing Diagram. • Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Cyclone V Devices table. • Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Cyclone V Devices chapter. — FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1 — FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1 — AS Configuration Timing Waveform — PS Configuration Timing Waveform
March 2015	2015.03.31	• Added V_{CC} specifications for devices with internal scrubbing feature (with SC suffix) in Recommended Operating Conditions table. • Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices table.

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Date	Version	Changes
January 2015	2015.01.23	• Updated the transceiver specification for Cyclone V ST from 5 Gbps to 6.144 Gbps. Updated the note in the following tables: — Transceiver Power Supply Operating Conditions for Cyclone V GX, GT, SX, and ST Devices — Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices — Transceiver Compliance Specification for All Supported Protocol for Cyclone V Devices • Updated the description for $V_{CC\_AUX\_SHARED}$ to "HPS auxiliary power supply". Added a note to state that $V_{CC\_AUX\_SHARED}$ must be powered by the same source as VCC_AUX for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices. Updated in the following tables: — Absolute Maximum Ratings for Cyclone V Devices — HPS Power Supply Operating Conditions for Cyclone V SE, SX, and ST Devices • Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. • Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification. • Updated f_{VCO} maximum value from 1400 MHz to 1600 MHz for –C7 and –I7 speed grades in the PLL specifications table. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Added the following notes in the High-Speed I/O Specifications for Cyclone V Devices table: — The Cyclone V devices support true RSDS output standard with data rates of up to 230 Mbps using true LVDS output buffer types on all I/O banks. — The Cyclone V devices support true mini-LVDS output standard with data rates of up to 340 Mbps using true LVDS output buffer types on all I/O banks. • Updated HPS Clock Performance main_base_clk specifications from 462 MHz to 400 MHz for –C6 speed grade. • Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C7, –I7, –A7, and –C8 speed grades) and 1,850 MHz (for –C6 speed grade). • Changed the symbol for HPS PLL input jitter divide value from NR to N. • Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables: — SPI Master Timing Requirements for Cyclone V Devices — SPI Slave Timing Requirements for Cyclone V Devices • Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board. • Added HPS JTAG timing specifications. • Updated the configuration `.rbf` size (bits) for Cyclone V devices. • Added a note to Uncompressed .rbf Sizes for Cyclone V Devices table: The recommended EPCQ serial configuration devices are able to store more than one image.

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Date	Version	Changes
July 2014	3.9	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20. • Updated h2f_user2_clk specification for –C6, –C7, and –I7 speed grades in Table 34. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 35. • Updated T_d and T_h specifications in Table 41. • Added T_h specification in Table 43 and Figure 10. • Updated a note in Figure 17, Figure 18, and Figure 20 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 54. • Added DCLK device initialization clock source specification in Table 56. • Added description in "Configuration Files" section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature. • Added "Recommended EPCQ Serial Configuration Device" values in Table 57. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 59.
February 2014	3.8	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.7	• Updated Table 1, Table 3, Table 19, Table 20, Table 23, Table 25, Table 27, Table 34, Table 44, Table 51, Table 52, Table 55, and Table 61. • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 24, Table 25, Table 26, Table 27, Table 28, Table 32, Table 33, Table 49, Table 50, Table 51, Table 52, Table 53, Table 54, Table 55, Table 57, Table 58, Table 59, Table 60, and Table 62.
November 2013	3.6	Updated Table 23, Table 30, and Table 31.
October 2013	3.5	• Added "HPS PLL Specifications". • Added Table 23, Table 35, and Table 36. • Updated Table 1, Table 5, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, Table 28, Table 34, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, and Table 53. • Updated Figure 1, Figure 2, Figure 4, Figure 10, Figure 12, Figure 13, and Figure 16. • Removed table: GPIO Pulse Width for Cyclone V Devices.

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Date	Version	Changes
June 2013	3.4	• Updated Table 20, Table 27, and Table 34. • Updated "UART Interface" and "CAN Interface" sections. • Removed the following tables: — Table 45: UART Baud Rate for Cyclone V Devices — Table 47: CAN Pulse Width for Cyclone V Devices
May 2013	3.3	• Added Table 33. • Updated Figure 5, Figure 6, Figure 17, Figure 19, and Figure 20. • Updated Table 1, Table 4, Table 5, Table 10, Table 13, Table 19, Table 20, Table 26, Table 32, Table 35, Table 36, Table 43, Table 53, Table 54, Table 57, and Table 61.
March 2013	3.2	• Added HPS reset information in the "HPS Specifications" section. • Added Table 57. • Updated Table 1, Table 2, Table 17, Table 20, Table 52, and Table 56. • Updated Figure 18.
January 2013	3.1	Updated Table 4, Table 20, and Table 56.
November 2012	3.0	• Updated Table 1, Table 4, Table 5, Table 9, Table 14, Table 16, Table 17, Table 19, Table 20, Table 25, Table 28, Table 52, Table 55, Table 56, and Table 59. • Removed table: Transceiver Block Jitter Specifications for Cyclone V GX Devices. • Added HPS information: — Added "HPS Specifications" section. — Added Table 33, Table 34, Table 35, Table 36, Table 37, Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, and Table 46. — Added Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, and Figure 16. — Updated Table 3.
June 2012	2.0	Updated for the Quartus Prime software v12.0 release: • Restructured document. • Removed "Power Consumption" section. • Updated Table 1,Table 3, Table 19, Table 20, Table 25, Table 27, Table 28, Table 30, Table 31, Table 34, Table 36, Table 37, Table 38, Table 39, Table 41, Table 43, and Table 46. • Added Table 22, Table 23, and Table 29. • Added Figure 1 and Figure 2. • Added "Initialization" and "Configuration Files" sections.

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