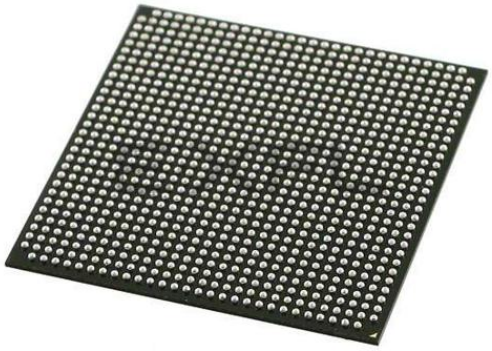

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	64KB
Peripherals	DMA, POR, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	800MHz
Primary Attributes	FPGA - 110K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5csxfc6d6f31i7n

Contents

Cyclone V Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Cyclone® V devices.

Cyclone V devices are offered in commercial and industrial grades. Commercial devices are offered in –C6 (fastest), –C7, and –C8 speed grades. Industrial grade devices are offered in the –I7 speed grade. Automotive devices are offered in the –A7 speed grade.

Cyclone V SoC devices are also offered in a low-power variant, as indicated by the L power option in the device part number. These devices have 30% static power reduction for devices with 25K LE and 40K LE, and 20% static power reduction for devices with 85K LE and 110K LE. Note that the L power option devices are only available in –I7 speed grade, and have the equivalent operating conditions and timing specifications as the standard –I7 speed grade devices.

Table 1. Low Power Variants

Density	Ordering Part Number (OPN)	Static Power Reduction
25K LE	5CSEBA2U19I7LN	30%
	5CSEBA2U23I7LN	
	5CSXFC2C6U23I7LN	
40K LE	5CSEBA4U19I7LN	
	5CSEBA4U23I7LN	
	5CSXFC4C6U23I7LN	
85K LE	5CSEBA5U19I7LN	20%
	5CSEBA5U23I7LN	
	5CSXC5C6U23I7LN	

continued...

Symbol	Description	Condition	Minimum(11)	Typical	Maximum(11)	Unit
		1.8 V	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
$V_{CC\_AUX\_SHARED}$(14)	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

Recommended Operating Conditions on page 8
Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based EPE and the Intel® Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Handbook
  Provides more information about power estimation tools.

(11) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(14) $V_{CC\_AUX\_SHARED}$ must be powered by the same source as V_{CC_AUX} for Cyclone V SX C5, C6, D5, and D6 devices, and Cyclone V SE A5 and A6 devices.

- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 11. OCT Variation after Power-Up Calibration for Cyclone V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of ±5% and a temperature range of 0°C to 85°C.

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

Single-Ended I/O Standards

Table 15. Single-Ended I/O Standards for Cyclone V Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL}[18] (mA)	I_{OH}[18] (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
3.0-V PCI*	2.85	3	3.15	—	0.3 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 × V_{CCIO}	0.5 × V_{CCIO}	V_{CCIO} + 0.3	0.1 × V_{CCIO}	0.9 × V_{CCIO}	1.5	–0.5
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Cyclone V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04

continued...

(18) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[21]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[22]			V_{OCM} (V)[22][23]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL[29]	—	—	—	300	—	—	0.60	D_{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D_{MAX} > 700 Mbps	1.60						
SLVS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
Sub-LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—
HiSpi	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	—	1.80	—	—	—	—	—	—

Related Information

- AN522: Implementing Bus LVDS Interface in Supported Intel Device Families
  Provides more information about BLVDS interface support in Intel devices.
- Transceiver Specifications for Cyclone V GX, GT, SX, and ST Devices on page 25
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Cyclone V core and periphery blocks.

(21) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(22) R_L range: 90 ≤ R_L ≤ 110 Ω.

(23) This applies to default pre-emphasis setting only.

(29) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable ppm detector[46]	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000									ppm
Run length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to 3 [47] DC gain setting = 0 to 1	Refer to *CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices* and *CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Cyclone V GX, GT, SX, and ST Devices* diagrams.									dB

Table 24. Transmitter Specifications for Cyclone V GX, GT, SX, and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 5[30]			Transceiver Speed Grade 6			Transceiver Speed Grade 7			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML										
Data rate	—	614	—	5000/6144[35]	614	—	3125	614	—	2500	Mbps
V_{OCM} (AC coupled)	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω

continued...

(45) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(46) The rate matcher supports only up to ±300 parts per million (ppm).

(47) The Intel Quartus Prime software allows AC gain setting = 3 for design with data rate between 614 Mbps and 1.25 Gbps only.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ}[56][57]	Input clock cycle-to-cycle jitter	F_{REF} ≥ 100 MHz	—	—	0.15	UI (p-p)
		F_{REF} < 100 MHz	—	—	±750	ps (p-p)
t_{OUTPJ_DC}[58]	Period jitter for dedicated clock output in integer PLL	F_{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F_{OUT} < 100 MHz	—	—	30	mUI (p-p)
t_{FOUTPJ_DC}[58]	Period jitter for dedicated clock output in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	425[61], 300[59]	ps (p-p)
		F_{OUT} < 100 MHz	—	—	42.5[61], 30[59]	mUI (p-p)
t_{OUTCCJ_DC}[58]	Cycle-to-cycle jitter for dedicated clock output in integer PLL	F_{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F_{OUT} < 100 MHz	—	—	30	mUI (p-p)
$t_{FOUTCCJ\_DC}$[58]	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	425[61], 300[59]	ps (p-p)
		F_{OUT} < 100 MHz	—	—	42.5[61], 30[59]	mUI (p-p)
t_{OUTPJ_IO}[58][60]	Period jitter for clock output on a regular I/O in integer PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
t_{FOUTPJ_IO}[58][60][61]	Period jitter for clock output on a regular I/O in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)

continued...

(56) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(57) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(58) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in *Memory Output Clock Jitter Specification for Cyclone V Devices* table.

(59) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

(60) External memory interface clock output jitter specifications use a different measurement method, which are available in *Memory Output Clock Jitter Specification for Cyclone V Devices* table.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
t_{OUTCCJ_IO}(58)(60)	Cycle-to-cycle jitter for clock output on regular I/O in integer PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
$t_{FOUTCCJ\_IO}$(58)(60)(61)	Cycle-to-cycle jitter for clock output on regular I/O in fractional PLL	F_{OUT} ≥ 100 MHz	—	—	650	ps (p-p)
		F_{OUT} < 100 MHz	—	—	65	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$(58)(62)	Period jitter for dedicated clock output in cascaded PLLs	F_{OUT} ≥ 100 MHz	—	—	300	ps (p-p)
		F_{OUT} < 100 MHz	—	—	30	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	Bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	f_{INPFD} = 100 MHz	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 49
Provides more information about the external memory interface clock output jitter specifications.

(61) This specification only covers fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(62) The cascaded PLL specification is only applicable with the following conditions:
- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

High-Speed I/O Specifications

Table 34. High-Speed I/O Specifications for Cyclone V Devices

When J = 1 or 2, bypass the serializer/deserializer (SERDES) block.

For LVDS applications, you must use the PLLs in integer PLL mode. This is achieved by using the LVDS clock network.

The Cyclone V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–C6			–C7, –I7			–C8, –A7			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	437.5	5	—	420	5	—	320	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40(63)	5	—	320	5	—	320	5	—	275	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	420	5	—	370	5	—	320	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =4 to 10(64)	(65)	—	840	(65)	—	740	(65)	—	640	Mbps

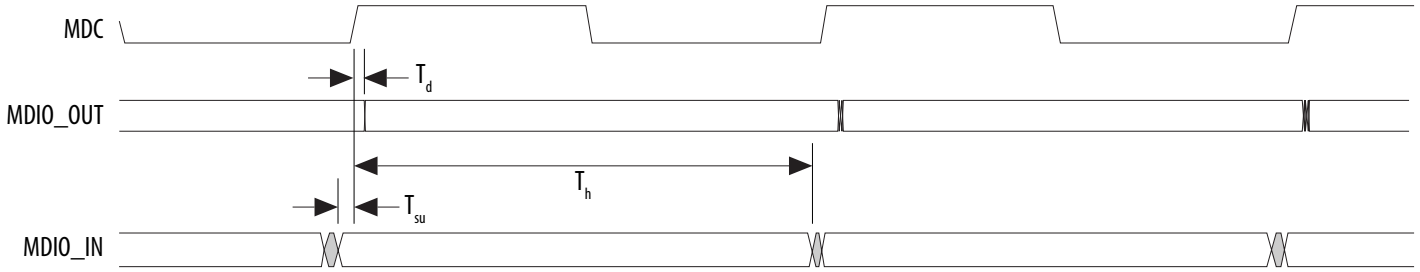
continued...

(63) Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

(64) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(65) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Figure 13. MDIO Timing Diagram



I²C Timing Characteristics

Table 51. I²C Timing Requirements for Cyclone V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

Symbol	Description	Min	Max	Unit
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Figure 15. NAND Command Latch Timing Diagram

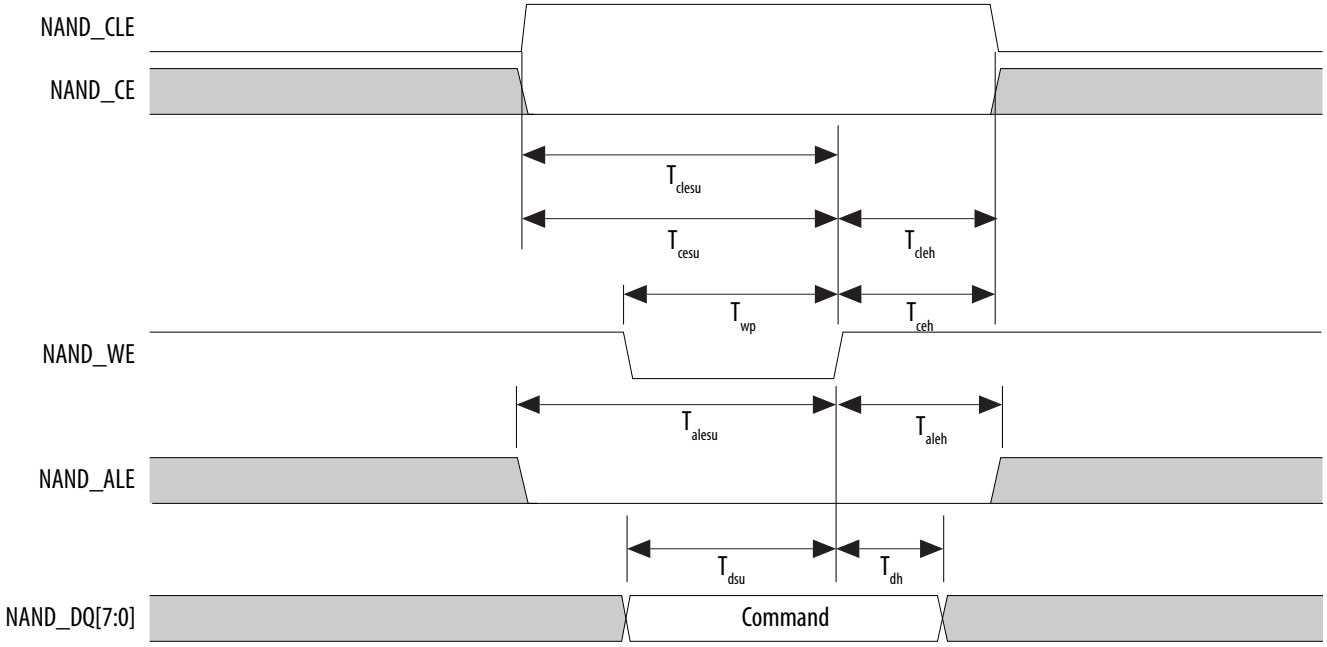
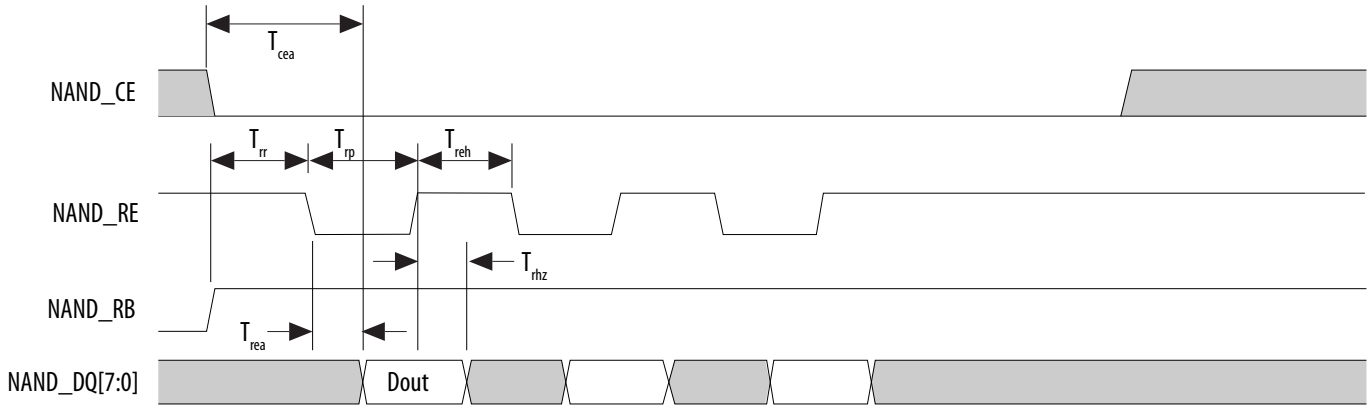


Figure 18. NAND Data Read Timing Diagram



Arm Trace Timing Characteristics

Table 53. Arm Trace Timing Requirements for Cyclone V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Cyclone V Devices table.

Table 58. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Cyclone V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(77)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(78)	µs
t_{CF2CK}(79)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(79)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 × $1/f_{MAX}$	—	s

continued...

(77) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

(78) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(79) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK}[83]	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}[83]	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$[84]	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode[85]	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times$ CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(82) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

(83) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(84) *N* is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

(85) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Configuration Files

Table 64. Uncompressed .rbf Sizes for Cyclone V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (`.rbf`) size is specifically for the Configuration via Protocol (CvP) feature.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)	Recommended EPCQ Serial Configuration Device(94)
Cyclone V E (95)	A2	21,061,280	275,608	EPCQ64
	A4	21,061,280	275,608	EPCQ64
	A5	33,958,560	322,072	EPCQ128
	A7	56,167,552	435,288	EPCQ128
	A9	102,871,776	400,408	EPCQ256
Cyclone V GX	C3	14,510,912	320,280	EPCQ32
	C4	33,958,560	322,072	EPCQ128
	C5	33,958,560	322,072	EPCQ128
	C7	56,167,552	435,288	EPCQ128
	C9	102,871,776	400,408	EPCQ256
Cyclone V GT	D5	33,958,560	322,072	EPCQ128
	D7	56,167,552	435,288	EPCQ128
	D9	102,871,776	400,408	EPCQ256
Cyclone V SE (95)	A2	33,958,560	322,072	EPCQ128

continued...

(94) The recommended EPCQ serial configuration devices are able to store more than one image.

(95) No PCIe hard IP, configuration via protocol (CvP) is not supported in this family.

Variant	Member Code	Active Serial[96]			Fast Passive Parallel[97]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A9	4	100	257	16	125	51
Cyclone V GX	C3	4	100	36	16	125	7
	C4	4	100	85	16	125	17
	C5	4	100	85	16	125	17
	C7	4	100	140	16	125	28
	C9	4	100	257	16	125	51
Cyclone V GT	D5	4	100	85	16	125	17
	D7	4	100	140	16	125	28
	D9	4	100	257	16	125	51
Cyclone V SE	A2	4	100	85	16	125	17
	A4	4	100	85	16	125	17
	A5	4	100	140	16	125	28
	A6	4	100	140	16	125	28
Cyclone V SX	C2	4	100	85	16	125	17
	C4	4	100	85	16	125	17
	C5	4	100	140	16	125	28
	C6	4	100	140	16	125	28
Cyclone V ST	D5	4	100	140	16	125	28
	D6	4	100	140	16	125	28

(96) DCLK frequency of 100 MHz using external CLKUSR.

(97) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Related Information

Configuration Files on page 76

Remote System Upgrades

Table 66. Remote System Upgrade Circuitry Timing Specifications for Cyclone V Devices

Parameter	Minimum	Unit
$t_{RU\_nCONFIG}$ (98)	250	ns
$t_{RU\_nRSTIMER}$ (99)	250	ns

Related Information

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about `reset_timer` (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 67. User Watchdog Internal Oscillator Frequency Specifications for Cyclone V Devices

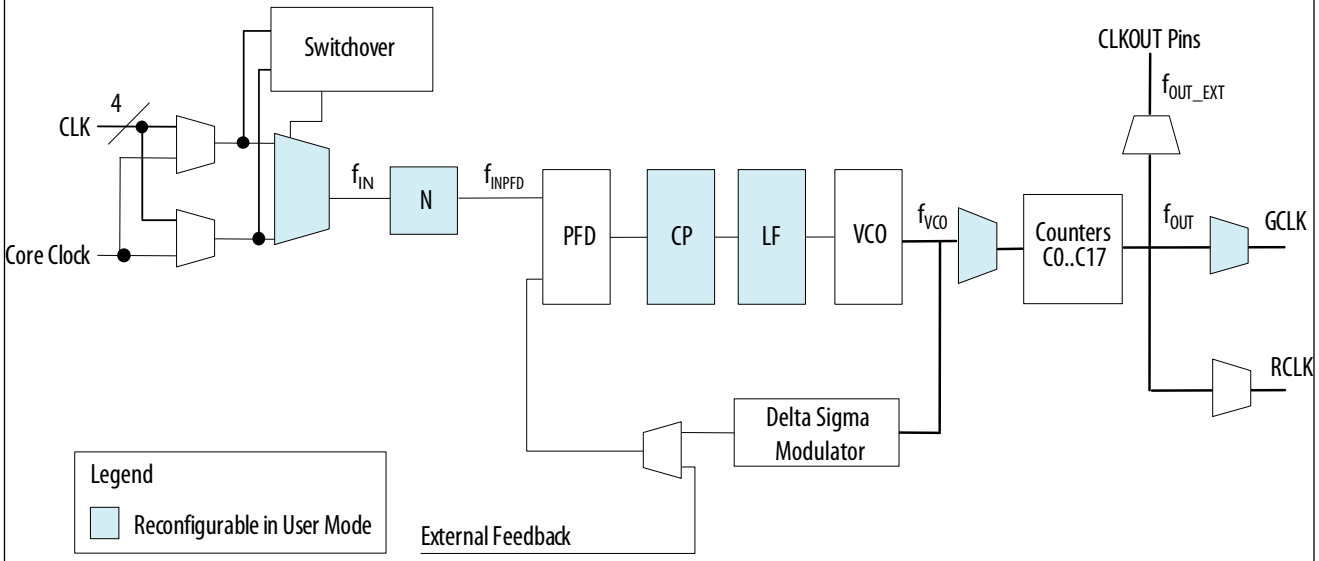
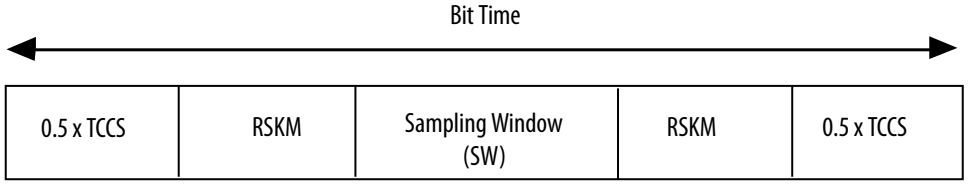
Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

Intel offers two ways to determine I/O timing—the Excel-based I/O timing and the Intel Quartus Prime Timing Analyzer.

(98) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(99) This is equivalent to strobing the reset timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

Term	Definition
	 Note: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.
R_L	Receiver differential input discrete resistor (external to the Cyclone V device).
Sampling window (SW)	Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 

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Date	Version	Changes
December 2015	2015.12.04	• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Cyclone V Devices table. — Updated F_{clk}, $T_{dutycycle}$, and $T_{dssfrst}$ specifications. — Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications. — Removed T_{dinmax} specifications. • Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Cyclone V Devices table. • Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Cyclone V Devices table. — Updated T_{clk} to $T_{sdmmc\_clk\_out}$ symbol. — Updated $T_{sdmmc\_clk\_out}$ and T_d specifications. — Added T_{sdmmc_clk}, T_{su}, and T_h specifications. — Removed T_{dinmax} specifications. • Updated the following diagrams: — Quad SPI Flash Timing Diagram — SD/MMC Timing Diagram • Updated configuration .rbf sizes for Cyclone V devices. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.12	• Updated the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Cyclone V Devices table: — True RSDS output standard: data rates of up to 360 Mbps — True mini-LVDS output standard: data rates of up to 400 Mbps • Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash. • Updated T_h location in I^2C Timing Diagram. • Updated T_{wp} location in NAND Address Latch Timing Diagram. • Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Cyclone V Devices table. • Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Cyclone V Devices chapter. — FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1 — FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1 — AS Configuration Timing Waveform — PS Configuration Timing Waveform
March 2015	2015.03.31	• Added V_{CC} specifications for devices with internal scrubbing feature (with SC suffix) in Recommended Operating Conditions table. • Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Cyclone V Devices table.

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