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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-LQFP-64-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc2237m-104f40l

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Summary of Features

The XC223xM types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the lower address
- DSRAM allocation starts from the higher address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.



Figure 1 SRAM Allocation



General Device Information

2.1 Pin Configuration and Definition

The pins of the XC223xM are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.



Figure 3 XC223xM Pin Configuration (top view)



General Device Information

Key to Pin Definitions

Ctrl.: The output signal for a port pin is selected by bit field PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bit field PC to 1x00_B, output O1 is selected by 1x01_B, etc.
 Output signal OH is controlled by hardware

Output signal OH is controlled by hardware.

- Type: Indicates the pad type and its power supply domain (A, B, M, 1).
 - St: Standard pad
 - Sp: Special pad e.g. XTALx
 - DP: Double pad can be used as standard or high speed pad
 - In: Input only pad
 - PS: Power supply pad

Pin	Symbol	Ctrl.	Туре	Function
3	TESTM	1	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.
4	TRST	1	In/B	Test-System Reset Input For normal system operation, pin TRST should be held low. A high level at this pin at the rising edge of PORST activates the XC223xM's debug system. In this case, pin TRST must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.
5	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input

Table 6 Pin Definitions and Functions



XC2238M, XC2237M XC2000 Family / Base Line

General Device Information

Table	Fable 6 Pin Definitions and Functions (cont'd)							
Pin	Symbol	Ctrl.	Туре	Function				
31	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output				
	U0C0_SELO 0	01	St/B	USIC0 Channel 0 Select/Control 0 Output				
	U0C1_SELO 1	02	St/B	USIC0 Channel 1 Select/Control 1 Output				
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.				
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input				
	RxDC0D	1	St/B	CAN Node 0 Receive Data Input				
	ESR2_6	1	St/B	ESR2 Trigger Input 6				
35	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output				
	U0C1_SELO 0	01	St/B	USIC0 Channel 1 Select/Control 0 Output				
	U0C0_SELO 1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output				
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.				
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input				
	RxDC1C	1	St/B	CAN Node 1 Receive Data Input				
	ESR2_7	1	St/B	ESR2 Trigger Input 7				
36	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output				
	U0C1_SCLK OUT	01	DP/B	USIC0 Channel 1 Shift Clock Output				
	EXTCLK	O2	DP/B	Programmable Clock Signal Output				
	CC2_CC21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.				
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input				



Functional Description

3.2 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instructionfetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.



Figure 5 CPU Block Diagram



Functional Description

3.5 Interrupt System

The architecture of the XC223xM supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC223xM has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11¹⁾ CPU clocks, the XC223xM can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XC223xM provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

¹⁾ Depending if the jump cache is used or not.



Functional Description

3.18 Instruction Set Summary

Table 11 lists the instructions of the XC223xM.

The addressing modes that can be used with a specific instruction, the function of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the "**Instruction Set Manual**".

This document also provides a detailed description of each instruction.

Mnemonic	Description	Bytes		
ADD(B)	Add word (byte) operands			
ADDC(B)	Add word (byte) operands with Carry			
SUB(B)	Subtract word (byte) operands			
SUBC(B)	Subtract word (byte) operands with Carry	2/4		
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- \times 16-bit)			
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2		
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2		
CPL(B)	Complement direct word (byte) GPR	2		
NEG(B)	Negate direct word (byte) GPR	2		
AND(B)	Bitwise AND, (word/byte operands)	2/4		
OR(B)	Bitwise OR, (word/byte operands)	2/4		
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2/4		
BCLR/BSET	Clear/Set direct bit	2		
BMOV(N)	Move (negated) direct bit to direct bit	4		
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4		
BCMP	Compare direct bit to direct bit	4		
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4		
CMP(B)	Compare word (byte) operands	2/4		
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2/4		
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2/4		
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2		
SHL/SHR	Shift left/right direct word GPR	2		

Table 11 Instruction Set Summary



4.2.1 DC Parameters

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Note: Operating Conditions apply.

 Table 14 is valid under the following conditions:

 $V_{\text{DDP}} \ge 4.5 \text{ V}; V_{\text{DDPtvp}} = 5 \text{ V}; V_{\text{DDP}} \le 5.5 \text{ V}$

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	1	Test Condition
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	C _{IO} CC	_	-	10	pF	not subject to production test
Input Hysteresis ²⁾	HYS CC	0.11 x V _{DDP}	-	-	V	$R_{\rm S} = 0$ Ohm
Absolute input leakage current on pins of analog ports ³⁾	I _{OZ1} CC	-	10	200	nA	$V_{\rm IN}$ > 0 V; $V_{\rm IN}$ < $V_{\rm DDP}$
Absolute input leakage current for all other pins. To be double	I _{OZ2} CC	-	0.2	5	μΑ	$\begin{array}{l} T_{\rm J} \leq {\rm 110~^\circ C}; \\ V_{\rm IN} < V_{\rm DDP}; \\ V_{\rm IN} > V_{\rm SS} \end{array}$
bond pins. ³⁾¹⁾⁴⁾		_	0.2	15	μΑ	$T_{ m J} \leq$ 150 °C; $V_{ m IN} < V_{ m DDP}$; $V_{ m IN} > V_{ m SS}$
Pull Level Force Current ⁵⁾	$ I_{PLF} $ SR	250	-	-	μΑ	6)
Pull Level Keep Current ⁷⁾	$ I_{PLK} $ SR	-	-	30	μA	6)
Input high voltage (all except XTAL1)	$V_{\rm IH}{ m SR}$	0.7 x V_{DDP}	-	V _{DDP} + 0.3	V	
Input low voltage (all except XTAL1)	$V_{\rm IL}{\rm SR}$	-0.3	-	$0.3 ext{ x}$ $V_{ ext{DDP}}$	V	
Output High voltage ⁸⁾	V _{OH} CC	V _{DDP} - 1.0	-	-	V	$I_{\rm OH} \ge I_{\rm OHmax}$
		V _{DDP} - 0.4	-	-	V	$I_{OH} \ge I_{OHnom}^{(9)}$

Table 14 DC Characteristics for Upper Voltage Range



XC2238M, XC2237M XC2000 Family / Base Line

Electrical Parameters



Figure 14Supply Current in Active Mode as a Function of FrequencyNote: Operating Conditions apply.



Table 18ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Broken wire detection delay against VAGND ²⁾	t _{BWG} CC	-	-	50	3)	
Broken wire detection delay against VAREF ²⁾	t _{BWR} CC	-	-	50	4)	
Conversion time for 8-bit result ²⁾	t _{c8} CC	(11 + S ⁻ + 2 x t _S	TC) x t _{AD} YS	ICI		
Conversion time for 10-bit result ²⁾	<i>t</i> _{c10} CC	(13 + S ⁻ + 2 x t _S	TC) x t _{AD} YS	ICI		
Total Unadjusted Error	TUE CC	-	1	2	LSB	5)
Wakeup time from analog powerdown, fast mode ²⁾	t _{WAF} CC	-	-	4	μS	
Wakeup time from analog powerdown, slow mode ²⁾	t _{WAS} CC	-	-	15	μS	
Analog reference ground	$V_{ m AGND}$ SR	V _{SS} - 0.05	-	1.5	V	
Analog input voltage range	$V_{\rm AIN}{ m SR}$	$V_{\rm AGND}$	-	V_{AREF}	V	6)
Analog reference voltage	V_{AREF} SR	V _{AGND} + 1.0	-	V _{DDPA} + 0.05	V	5)

 These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

- The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 μs. Result below 10% (66_H).
- 4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 μs. This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H).
- 5) TUE is tested at V_{AREF} = V_{DDPA} = 5.0 V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.
- V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be X000_H or X3FF_H, respectively.





Figure 16 Equivalent Circuitry for Analog Inputs



Table 21	Coding of bit fields LEVxV in Register SWDCON0 (cont'd)							
Code	Default Voltage Level	Notes ¹⁾						
1001 _B	4.5 V	LEV2V: no request						
1010 _B	4.6 V							
1011 _B	4.7 V							
1100 _B	4.8 V							
1101 _B	4.9 V							
1110 _B	5.0 V							
1111 _B	5.5 V							

1) The indicated default levels are selected automatically after a power reset.

Table 22 Coding of Bitfields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes ¹⁾
000 _B	0.95 V	
001 _B	1.05 V	
010 _B	1.15 V	
011 _B	1.25 V	
100 _B	1.35 V	LEV1V: reset request
101 _B	1.45 V	LEV2V: interrupt request ²⁾
110 _B	1.55 V	
111 _B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use the this warning level.



4.6 AC Parameters

These parameters describe the dynamic behavior of the XC223xM.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).



Figure 17 Input Output Waveforms







The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.

The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and Figure 20).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS} . The number of VCO cycles is K2 × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

 D_{Tmax} [ns] = ±(220 / (K2 × f_{SYS}) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of $\mathbf{T} \times TCS$ the accumulated jitter D_T is determined by:

 D_{T} [ns] = $D_{Tmax} \times [(1 - 0.058 \times K2) \times (T - 1) / (0.83 \times f_{SYS} - 1) + 0.058 \times K2]$

 f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

 $D_{max} = \pm (220 / (4 \times 33) + 4.3) = 5.97$ ns (Not applicable directly in this case!)

 $D_3 = 5.97 \times [(1 - 0.058 \times 4) \times (3 - 1) / (0.83 \times 33 - 1) + 0.058 \times 4]$

= 5.97 × [0.768 × 2 / 26.39 + 0.232]

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

 $D_{max} = \pm (220 / (2 \times 33) + 4.3) = 7.63$ ns (Not applicable directly in this case!)

 $\begin{array}{l} \mathsf{D}_3 = 7.63 \times [(1 - 0.058 \times 2) \times (3 - 1) \ / \ (0.83 \times 33 - 1) + 0.058 \times 2] \\ = 7.63 \times [0.884 \times 2 \ / \ 26.39 + 0.116] \end{array}$



PLL frequency band selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
VCO output frequency	$f_{\rm VCO} {\rm CC}$	50	-	110	MHz	$VCOSEL = 00_B$
(VCO controlled)		100	-	160	MHz	$VCOSEL = 01_B$
VCO output frequency	$f_{\rm VCO} {\rm CC}$	10	-	40	MHz	$VCOSEL = 00_B$
(VCO free-running)		20	-	80	MHz	$VCOSEL = 01_B$

Table 24 System PLL Parameters

4.6.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

 $f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.6.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system. Please refer to the Programmer's Guide.



- 1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF} . This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1} .
- 2) Overload conditions must not occur on pin XTAL1.
- Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.

The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.



Figure 21 External Clock Drive XTAL1



Table 29 USIC SSC Master Mode Timing for Lower Voltage Range	(cont'd)
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Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Receive data input setup time to SCLKOUT receive edge	t ₄ SR	40	-	-	ns	
Data input DX0 hold time from SCLKOUT receive edge	t ₅ SR	-5	-	-	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 30 USIC SSC Slave Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.	1	Test Condition
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	<i>t</i> ₁₀ SR	7	-	-	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	<i>t</i> ₁₁ SR	7	-	-	ns	
Receive data input setup time to shift clock receive edge ¹⁾	<i>t</i> ₁₂ SR	7	_	-	ns	
Data input DX0 hold time from clock input DX1 receive edge ¹⁾	<i>t</i> ₁₃ SR	5	-	-	ns	
Data output DOUT valid time	<i>t</i> ₁₄ CC	7	-	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).



Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; C_L = 20 pF.

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
TCK clock period	t ₁ SR	50 ¹⁾	-	-	ns	2)
TCK high time	t_2 SR	16	-	-	ns	
TCK low time	t ₃ SR	16	-	-	ns	
TCK clock rise time	t_4 SR	-	-	8	ns	
TCK clock fall time	t ₅ SR	-	-	8	ns	
TDI/TMS setup to TCK rising edge	t ₆ SR	6	-	-	ns	
TDI/TMS hold after TCK rising edge	t ₇ SR	6	-	-	ns	
TDO valid from TCK falling edge (propagation delay) ³⁾	t ₈ CC	-	25	29	ns	
TDO high impedance to valid output from TCK falling edge ⁴⁾³⁾	t ₉ CC	-	25	29	ns	
TDO valid output to high impedance from TCK falling edge ³⁾	<i>t</i> ₁₀ CC	-	25	29	ns	
TDO hold after TCK falling edge ³⁾	<i>t</i> ₁₈ CC	5	-	_	ns	

Table 34JTAG Interface Timing for Upper Voltage Range

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \ge t_{SYS}$.

2) Under typical conditions, the interface can operate at transfer rates up to 20 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.

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