Welcome to <u>E-XFL.COM</u>

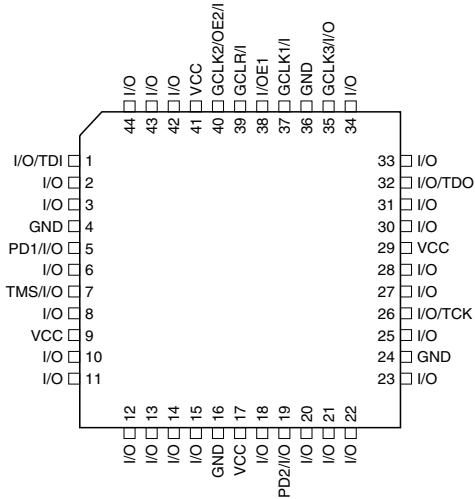**Understanding <u>Embedded - CPLDs (Complex Programmable Logic Devices)</u>**

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.
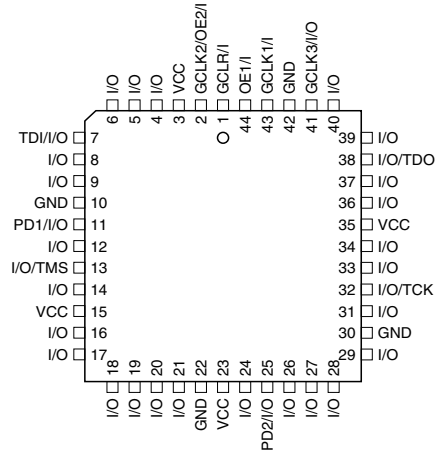
Applications of Embedded - CPLDs

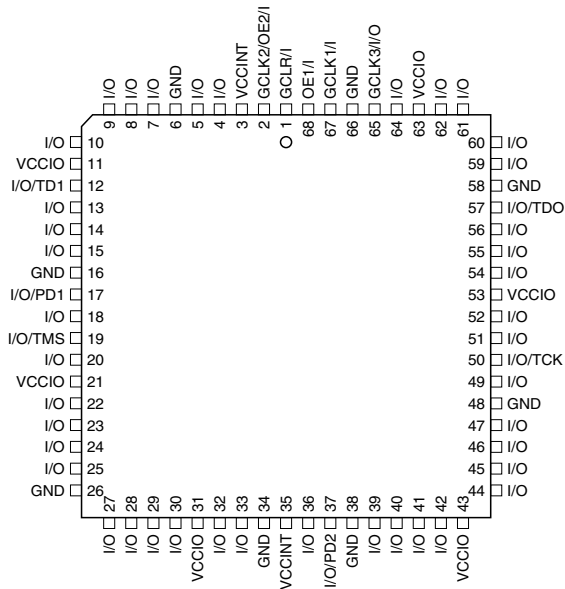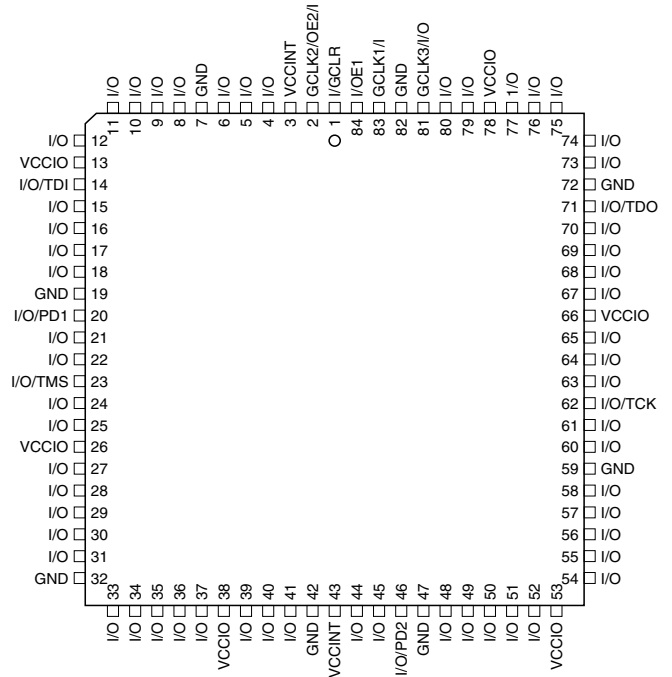| Details	
Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atf1504asv-15ji84

44-lead TQFP
Top View

```
                44 43 42 41 40 39 38 37 36 35 34
                │  │  │  │  │  │  │  │  │  │  │
               I/O I/O I/O VCC     I/OE1  GND  I/O
                         GCLK2/OE2/I  GCLK1/I  GCLK3/I/O
                           GCLKR/I

I/O/TDI ☐ 1                                33 ☐ I/O
I/O     ☐ 2                                32 ☐ I/O/TDO
I/O     ☐ 3                                31 ☐ I/O
GND     ☐ 4                                30 ☐ I/O
PD1/I/O ☐ 5                                29 ☐ VCC
I/O     ☐ 6                                28 ☐ I/O
TMS/I/O ☐ 7                                27 ☐ I/O
I/O     ☐ 8                                26 ☐ I/O/TCK
VCC     ☐ 9                                25 ☐ I/O
I/O     ☐ 10                               24 ☐ GND
I/O     ☐ 11                               23 ☐ I/O

                12 13 14 15 16 17 18 19 20 21 22
                │  │  │  │  │  │  │  │  │  │  │
               I/O I/O I/O GND VCC I/O    I/O I/O
                              PD2/I/O
```

44-lead PLCC
Top View

```
                6  5  4  3  2  1  44 43 42 41 40
                │  │  │  │  │  │  │  │  │  │  │
               I/O I/O I/O VCC  GCLKR/I GCLK1/I GND I/O
                         GCLK2/OE2/I  OE1/I  GCLK3/I/O

TDI/I/O ☐ 7                                39 ☐ I/O
I/O     ☐ 8                                38 ☐ I/O/TDO
I/O     ☐ 9                                37 ☐ I/O
GND     ☐ 10                               36 ☐ I/O
PD1/I/O ☐ 11                               35 ☐ VCC
I/O     ☐ 12                               34 ☐ I/O
I/O/TMS ☐ 13                               33 ☐ I/O
I/O     ☐ 14                               32 ☐ I/O/TCK
VCC     ☐ 15                               31 ☐ I/O
I/O     ☐ 16                               30 ☐ GND
I/O     ☐ 17                               29 ☐ I/O

                18 19 20 21 22 23 24 25 26 27 28
                │  │  │  │  │  │  │  │  │  │  │
               I/O I/O I/O I/O GND VCC    I/O I/O I/O
                                    PD2/I/O
```

68-lead PLCC
Top View

```
            9  8  7  6  5  4  3  2  1  68 67 66 65 64 63 62 61
            │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │
           I/O I/O I/O GND I/O VCCINT  GCLKR/I GCLK1/I GND GCLK3/I/O I/O VCCIO I/O
                           GCLK2/OE2/I  OE1/I

I/O     ☐ 10                                            60 ☐ I/O
VCCIO   ☐ 11                                            59 ☐ I/O
I/O/TD1 ☐ 12                                            58 ☐ GND
I/O     ☐ 13                                            57 ☐ I/O/TDO
I/O     ☐ 14                                            56 ☐ I/O
I/O     ☐ 15                                            55 ☐ I/O
GND     ☐ 16                                            54 ☐ I/O
I/O/PD1 ☐ 17                                            53 ☐ VCCIO
I/O     ☐ 18                                            52 ☐ I/O
I/O/TMS ☐ 19                                            51 ☐ I/O
I/O     ☐ 20                                            50 ☐ I/O/TCK
VCCIO   ☐ 21                                            49 ☐ I/O
I/O     ☐ 22                                            48 ☐ GND
I/O     ☐ 23                                            47 ☐ I/O
I/O     ☐ 24                                            46 ☐ I/O
I/O     ☐ 25                                            45 ☐ I/O
GND     ☐ 26                                            44 ☐ I/O

            27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43
            │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │
           I/O I/O I/O VCCIO I/O I/O GND VCCINT I/O I/O/PD2 GND I/O I/O I/O I/O VCCIO
```

84-lead PLCC
Top View

```
            11 10 9  8  7  6  5  4  3  2  1  84 83 82 81 80 79 78 77 76 75
            │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │
           I/O I/O I/O I/O GND I/O I/O VCCINT  GCLKR GCLK1/I GND GCLK3/I/O I/O I/O VCCIO I/O I/O I/O
                              GCLK2/OE2/I I/GCLR  I/OE1

I/O     ☐ 12                                            74 ☐ I/O
VCCIO   ☐ 13                                            73 ☐ I/O
I/O/TDI ☐ 14                                            72 ☐ GND
I/O     ☐ 15                                            71 ☐ I/O/TDO
I/O     ☐ 16                                            70 ☐ I/O
I/O     ☐ 17                                            69 ☐ I/O
I/O     ☐ 18                                            68 ☐ I/O
GND     ☐ 19                                            67 ☐ I/O
I/O/PD1 ☐ 20                                            66 ☐ VCCIO
I/O     ☐ 21                                            65 ☐ I/O
I/O     ☐ 22                                            64 ☐ I/O
I/O/TMS ☐ 23                                            63 ☐ I/O
I/O     ☐ 24                                            62 ☐ I/O/TCK
I/O     ☐ 25                                            61 ☐ I/O
VCCIO   ☐ 26                                            60 ☐ I/O
I/O     ☐ 27                                            59 ☐ GND
I/O     ☐ 28                                            58 ☐ I/O
I/O     ☐ 29                                            57 ☐ I/O
I/O     ☐ 30                                            56 ☐ I/O
I/O     ☐ 31                                            55 ☐ I/O
GND     ☐ 32                                            54 ☐ I/O

            33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
            │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │
           I/O I/O I/O I/O VCCIO I/O I/O I/O I/O GND VCCINT I/O I/O/PD2 GND I/O I/O I/O I/O I/O VCCIO
```

ATF1504ASV(L)

100-lead PQFP
Top View

Top pins (left to right, 100–81): I/O, I/O, I/O, GND, I/O, I/O, I/O, VCCINT, INPUT/OE2/GCLK2, INPUT/GCLR, INPUT/OE1, INPUT/GCLK1, GND, I/O/GCLK3, I/O, I/O, VCCIO, I/O, I/O, I/O

Left pins (top to bottom, 1–30):
- NC 1
- NC 2
- I/O 3
- I/O 4
- VCCIO 5
- I/O/TDI 6
- NC 7
- I/O 8
- NC 9
- I/O 10
- I/O 11
- I/O 12
- GND 13
- I/O/PD1 14
- I/O 15
- I/O 16
- I/O/TMS 17
- I/O 18
- I/O 19
- VCCIO 20
- I/O 21
- I/O 22
- I/O 23
- NC 24
- I/O 25
- NC 26
- I/O 27
- GND 28
- NC 29
- NC 30

Right pins (top to bottom, 80–51):
- NC 80
- NC 79
- I/O 78
- I/O 77
- GND 76
- I/O/TDO 75
- NC 74
- I/O 73
- NC 72
- I/O 71
- I/O 70
- I/O 69
- VCCIO 68
- I/O 67
- I/O 66
- I/O 65
- I/O/TCK 64
- I/O 63
- I/O 62
- GND 61
- I/O 60
- I/O 59
- I/O 58
- NC 57
- I/O 56
- NC 55
- I/O 54
- VCCIO 53
- NC 52
- NC 51

Bottom pins (left to right, 31–50): I/O, I/O, I/O, I/O, VCCIO, I/O, I/O, I/O, GND, I/O, VCCINT, I/O, I/O, I/O/PD2, GND, I/O, I/O, I/O, I/O, I/O

100-lead TQFP
Top View

Top pins (left to right, 100–76): I/O, I/O, I/O, I/O, GND, I/O, I/O, VCCINT, INPUT/OE2/GCLK2, INPUT/GCLR, INPUT/OE1, INPUT/GCLK1, GND, I/O/GCLK3, I/O, VCCIO, I/O, I/O, NC, NC, I/O

Left pins (top to bottom, 1–25):
- NC 1
- NC 2
- VCCIO 3
- I/O/TDI 4
- NC 5
- I/O 6
- NC 7
- I/O 8
- I/O 9
- I/O 10
- GND 11
- I/O/PD1 12
- I/O 13
- I/O 14
- I/O/TMS 15
- I/O 16
- I/O 17
- VCCIO 18
- I/O 19
- I/O 20
- I/O 21
- NC 22
- I/O 23
- NC 24
- I/O 25

Right pins (top to bottom, 75–51):
- I/O 75
- GND 74
- I/O/TDO 73
- NC 72
- I/O 71
- NC 70
- I/O 69
- I/O 68
- I/O 67
- VCCIO 66
- I/O 65
- I/O 64
- I/O/TCK 62
- I/O 61
- I/O 60
- GND 59
- I/O 58
- I/O 57
- NC 55
- I/O 54
- NC 53
- I/O 52
- VCCIO 51

Bottom pins (left to right, 26–50): GND, NC, NC, I/O, I/O, I/O, I/O, VCCIO, I/O, I/O, I/O, VCCINT, I/O, I/O, I/O/PD2, GND, I/O, I/O, I/O, I/O, I/O, NC, NC, I/O

AMEL

Description

The ATF1504ASV(L) is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504ASV(L)'s enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504ASV(L) has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504ASV(L) allows fast, efficient generation of complex logic functions. The ATF1504ASV(L) contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504ASV(L) macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

Block Diagram
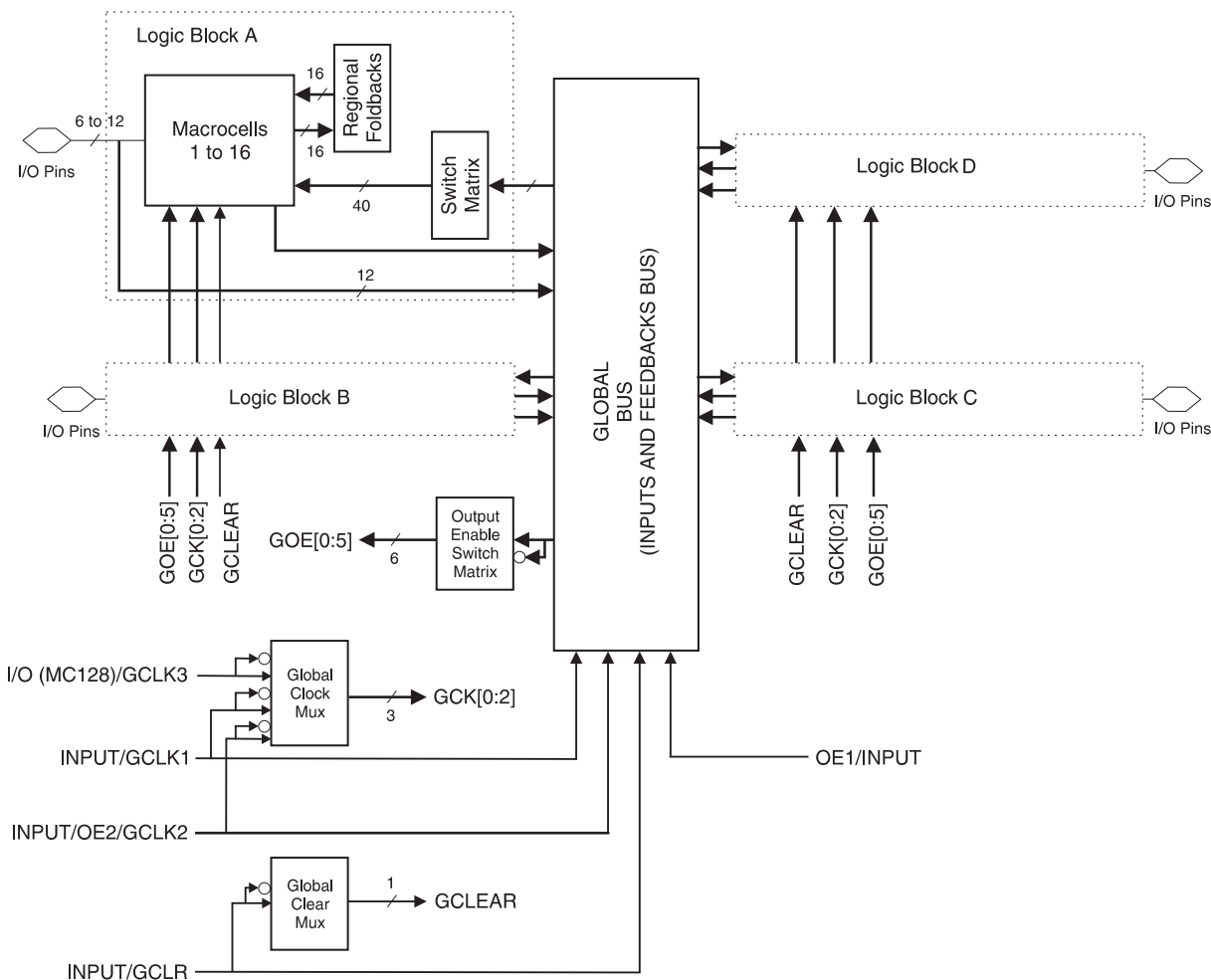
Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1504ASV(L). Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1504ASV(L) device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

Product Terms and Select Mux

Each ATF1504ASV(L) macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

Figure 1. ATF1504ASV(L) Macrocell
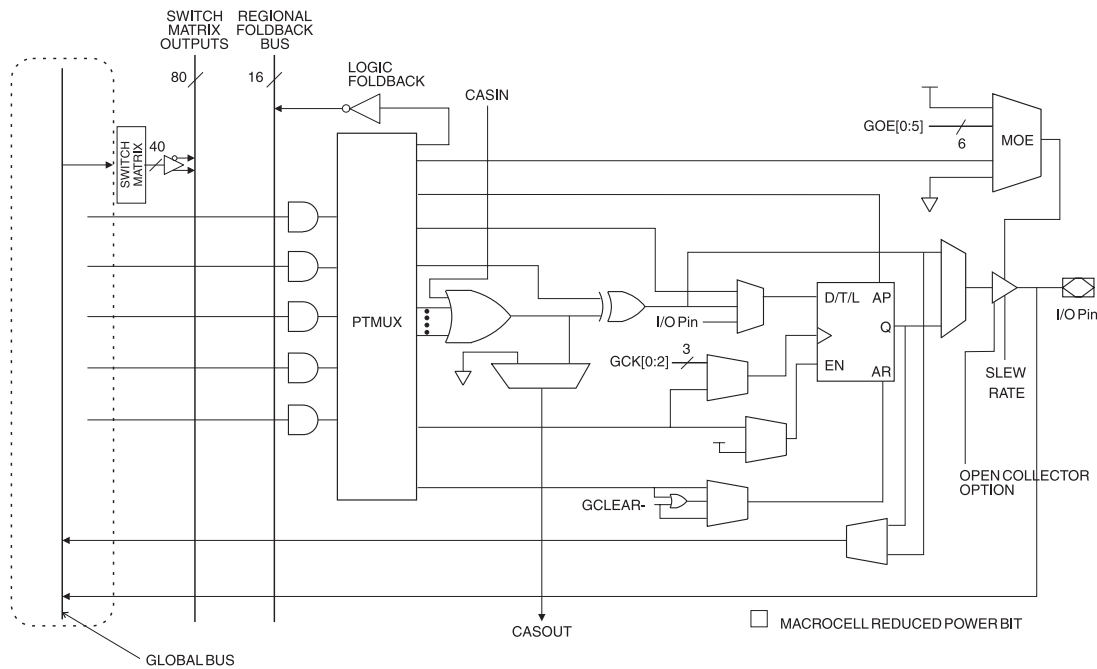
Programmable Pin-keeper Option for Inputs and I/Os

The ATF1504ASV(L) offers the option of programming all input and I/O pins so that pin keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high- or low-level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram
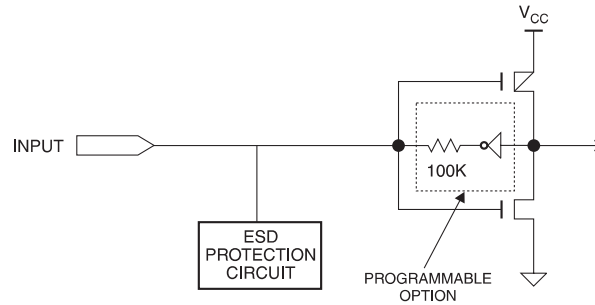
I/O Diagram
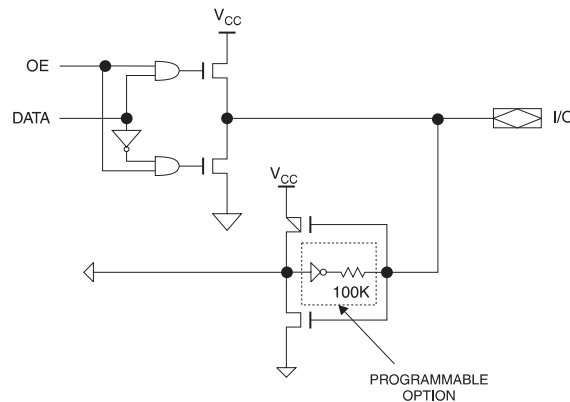
Speed/Power Management

The ATF1504ASV(L) has several built-in speed and power management features. The ATF1504ASV(L) contains circuitry that automatically puts the device into a low power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5 MHz. This feature may be selected as a device option.

To further reduce power, each ATF1504ASV(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504ASV(L) also have an optional power-down mode. In this mode, current drops to below 5 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

Programming

ATF1504ASV(L) devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504ASV(L) via the PC. ISP is performed by using either a download cable, a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504ASV(L) devices can also be programmed using standard third-party programmers. With third-party programmer the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

ISP Programming Protection

The ATF1504ASV(L) has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin keeper option preserves the former state during device programming, if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504ASV(L) is being programmed via ISP.

All ATF1504ASV(L) devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient))	0°C - 70°C	-40°C - 85°C
V_{CC} (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	
I_{OZ}	Tri-State Output Off-State Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Mode	Com.		60		mA
				Ind.		75		mA
			"L" Mode	Com.		5		µA
				Ind.		5		µA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CC} = Max V_{IN} = 0, V_{CC}	"PD" Mode			0.1	5	mA
I_{CC3}[2]	Reduced-power Mode Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Power	Com		40		ma
				Ind		55		
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				1.7		V_{CCIO} + 0.3	V
V_{OL}	Output Low Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = Min, I_{OL} = 8 mA		Com.			0.45	V
				Ind.			0.45	
	Output Low Voltage (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = Min, I_{OL} = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
V_{OH}	Output High Voltage - 3.3V (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = Min, I_{OH} = -2.0 mA			2.4			V
	Output High Voltage - 3.3V (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} V_{CCIO} = Min, I_{OH} = -0.1 mA			V_{CCIO} - 0.2			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. When microcell reduced-power feature is enabled.

Pin Capacitance

	Typ	Max	Units	Conditions
C_{IN}		8	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$		8	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.
The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

AC Characteristics

|		-15		-20		
Symbol	Parameter	Min	Max	Min	Max	Units
t_{PD1}	Input or Feedback to Non-Registered Output	3	15		20	ns
t_{PD2}	I/O Input or Feedback to Non-Registered Feedback	3	12		16	ns
t_{SU}	Global Clock Setup Time	11		13.5		ns
t_H	Global Clock Hold Time	0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		ns
t_{FH}	Global Clock Hold Time of Fast Input	1.0		2		MHz
t_{COP}	Global Clock to Output Delay		9		12	ns
t_{CH}	Global Clock High Time	5		6		ns
t_{CL}	Global Clock Low Time	5		6		ns
t_{ASU}	Array Clock Setup Time	5		7		ns
t_{AH}	Array Clock Hold Time	4		4		ns
t_{ACOP}	Array Clock Output Delay		15		18.5	ns
t_{ACH}	Array Clock High Time	6		8		ns
t_{ACL}	Array Clock Low Time	6		8		ns
t_{CNT}	Minimum Clock Global Period		13		17	ns
f_{CNT}	Maximum Internal Global Clock Frequency	76.9		66		MHz
t_{ACNT}	Minimum Array Clock Period		13		17	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	76.9		58.8		MHz
f_{MAX}	Maximum Clock Frequency	100		83.3		MHz
t_{IN}	Input Pad and Buffer Delay		2		2.5	ns
t_{IO}	I/O Input Pad and Buffer Delay		2		2.5	ns
t_{FIN}	Fast Input Delay		2		2	ns
t_{SEXP}	Foldback Term Delay		8		10	ns
t_{PEXP}	Cascade Logic Delay		1		1	ns
t_{LAD}	Logic Array Delay		6		8	ns
t_{LAC}	Logic Control Delay		3.5		4.5	ns
t_{IOE}	Internal Output Enable Delay		3		3	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 5V; C_L = 35 pF)		3		4	ns
t_{OD2}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		3		4	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 5V or 3.3V; C_L = 35 pF)		5		6	ns
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		7		9	ns

JTAG-BST/ISP Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504ASV(L). The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing. The ATF1504ASV(L) does not currently include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504ASV(L)'s ISP can be fully described using JTAG's BSDL as described in IEEE Standard 1149.1b. This allows ATF1504ASV(L) programming to be described and implemented using any one of the third-party development tools supporting this standard.

The ATF1504ASV(L) has the option of using four JTAG-standard I/O pins for boundary-scan testing (BST) and in-system programming (ISP) purposes. The ATF1504ASV(L) is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 5V TTL-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-scan Cell (BSC) Testing

The ATF1504ASV(L) contains up to 68 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers. There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown below.

BSC Configuration for Input and I/O Pins (Except JTAG TAP Pins)
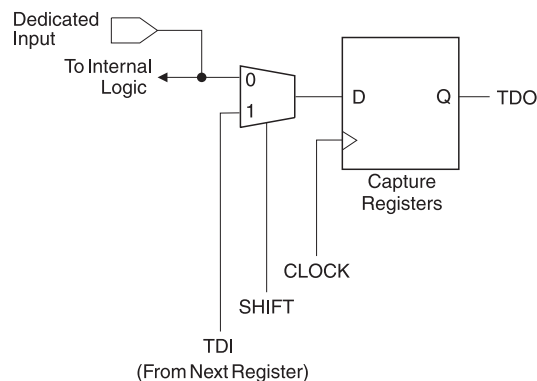
Note: The ATF1504ASV(L) has pull-up option on TMS and TDI pins. This feature is selected as a design option.

BSC Configuration for Macrocell

Pin BSC

Macrocell BSC
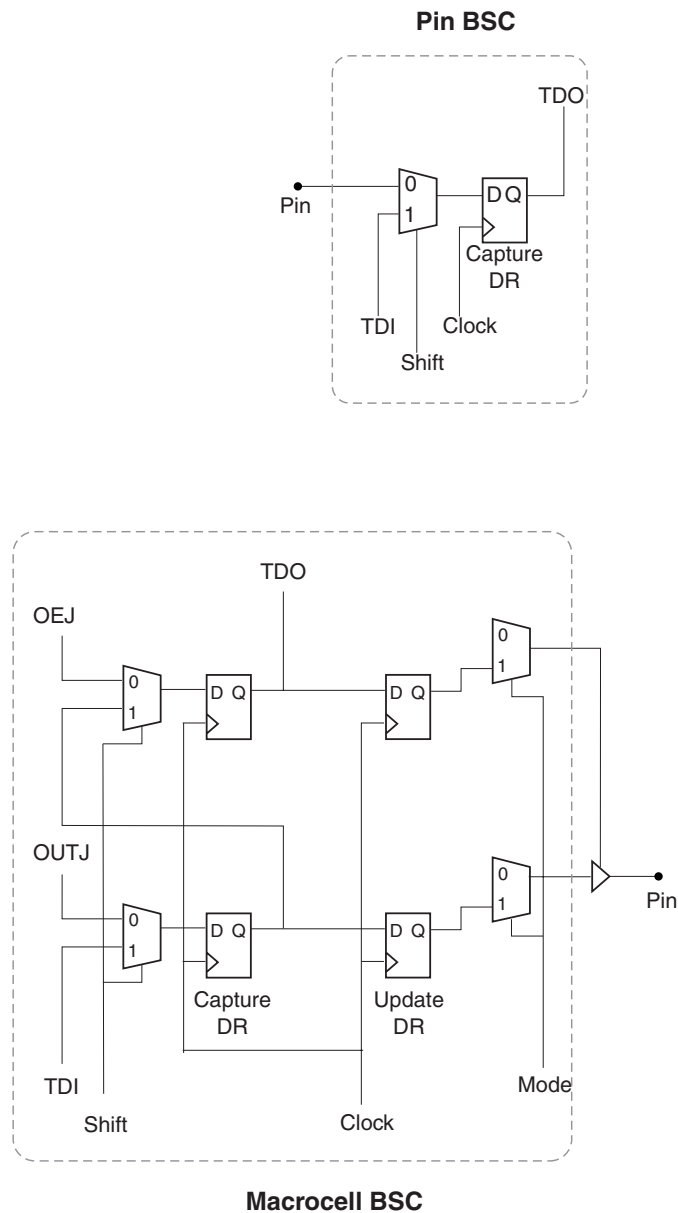
ATF1504ASV I/O Pinouts

| MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP	MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100-lead PQFP	100-lead TQFP
1	A	12	6	18	22	16	14	33	C	24	18	36	44	42	40
2	A	-	-	-	21	15	13	34	C	-	-	-	45	43	41
3	A/ PD1	11	5	17	20	14	12	35	C/ PD2	25	19	37	46	44	42
4	A	9	3	15	18	12	10	36	C	26	20	39	48	46	44
5	A	8	2	14	17	11	9	37	C	27	21	40	49	47	45
6	A	-	-	13	16	10	8	38	C	-	-	41	50	48	46
7	A	-	-	-	15	8	6	39	C	-	-	-	51	49	47
8/ TDI	A	7	1	12	14	6	4	40	C	28	22	42	52	50	48
9	A	-	-	10	12	4	100	41	C	29	23	44	54	54	52
10	A	-	-	-	11	3	99	42	C	-	-	-	55	56	54
11	A	6	44	9	10	100	98	43	C	-	-	45	56	58	56
12	A	-	-	8	9	99	97	44	C	-	-	46	57	59	57
13	A	-	-	7	8	98	96	45	C	-	-	47	58	60	58
14	A	5	43	5	6	96	94	46	C	31	25	49	60	62	60
15	A	-	-	-	5	95	93	47	C	-	-	-	61	63	61
16	A	4	42	4	4	94	92	48/ TCK	C	32	26	50	62	64	62
17	B	21	15	33	41	39	37	49	D	33	27	51	63	65	63
18	B	-	-	-	40	38	36	50	D	-	-	-	64	66	64
19	B	20	14	32	39	37	35	51	D	34	28	52	65	67	65
20	B	19	13	30	37	35	33	52	D	36	30	54	67	69	67
21	B	18	12	29	36	34	32	53	D	37	31	55	68	70	68
22	B	-	-	28	35	33	31	54	D	-	-	56	69	71	69
23	B	-	-	-	34	32	30	55	D	-	-	-	70	73	71
24	B	17	11	27	33	31	29	56/ TDO	D	38	32	57	71	75	73
25	B	16	10	25	31	27	25	57	D	39	33	59	73	77	75
26	B	-	-	-	30	25	23	58	D	-	-	-	74	78	76
27	B	-	-	24	29	23	21	59	D	-	-	60	75	81	79
28	B	-	-	23	28	22	20	60	D	-	-	61	76	82	80
29	B	-	-	22	27	21	19	61	D	-	-	62	77	83	81
30	B	14	8	20	25	19	17	62	D	40	34	64	79	85	83
31	B	-	-	-	24	18	16	63	D	-	-	-	80	86	84
32/ TMS	B	13	7	19	23	17	15	64	D/ GCLK3	41	35	65	81	87	85

OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)
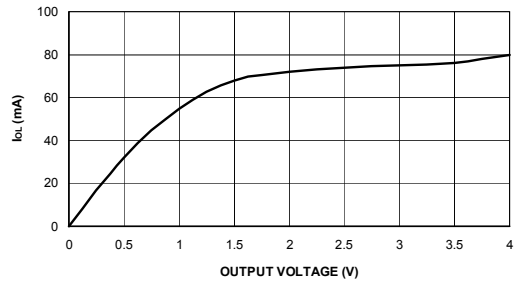
INPUT CURRENT VS. INPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)
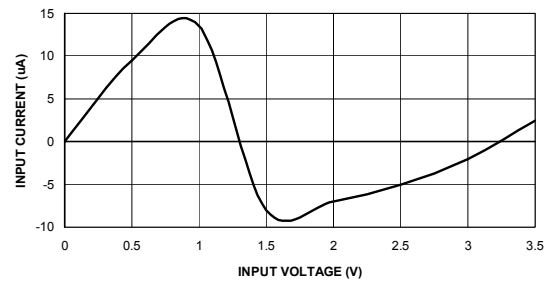
INPUT CLAMP CURRENT VS. INPUT VOLTAGE
(V_{CC} = 3.3V, T_A = 25°C)
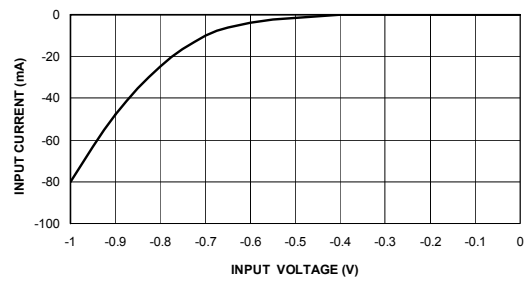
Ordering Information

ATF1504ASV(L) Standard Package Options

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1504ASV-15 AC44	44A	Commercial (0°C to 70°C)
			ATF1504ASV-15 JC44	44J	
			ATF1504ASV-15 JC68[2]	68J	
			ATF1504ASV-15 JC84[3]	84J	
			ATF1504ASV-15 QC100[2]	100Q1	
			ATF1500ASV-15 AC100	100A	
15	8	100	ATF1504ASV-15 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504ASV-15 JI44	44J	
			ATF1504ASV-15 JI68	68J	
			ATF1504ASV-15 JI84	84J	
			ATF1504ASV-15 QI100	100Q1	
			ATF1504ASV-15 AI100	100A	
20	12	83.3	ATF1504ASVL-20 AC44	44A	Commercial (0°C to 70°C)
			ATF1504ASVL-20 JC44	44J	
			ATF1504ASVL-20 JC68[2]	68J	
			ATF1504ASVL-20 JC84[3]	84J	
			ATF1504ASVL-20 QC100[2]	100Q1	
			ATF1504ASVL-20 AC100	100A	
20	12	83.3	ATF1504ASVL-20 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504ASVL-20 JI44	44J	
			ATF1504ASVL-20 JI68	68J	
			ATF1504ASVL-20 JI84	84J	
			ATF1504ASVL-20 QI100	100Q1	
			ATF1504ASVL-20 AI100	100A	

Note:
1. The last time buy is Sept. 30, 2005 for shaded parts.
2. The recommended migration for QC100 or JC68 packages is the AU100 or the smaller JU44 packages.
3. The recommended migration for the JC84 package is the ATF1508ASV-15JU84
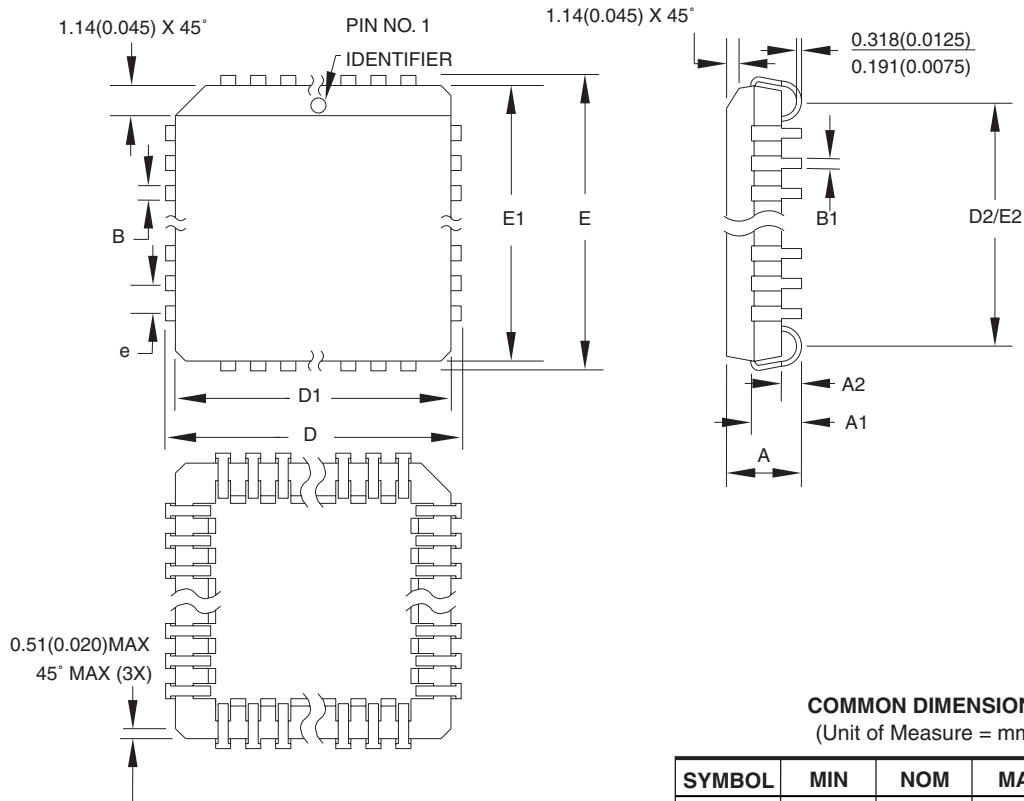
Using "C" Product for Industrial

There is very little risk in using "C" devices for industrial applications because the V_{CC} conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate I_{CC} by 15%.

ATF1504ASV(L) Green Package Options (Pb/Halide-free/RoHS Compliant)

t$_{PD}$ (ns)	t$_{CO1}$ (ns)	f$_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1504ASV-15 AU44	44A	Industrial (-40°C to +85°C)
			ATF1504ASV-15 JU44	44J	
			ATF1504ASV-15 AU100	100A	
20	12	83.3	ATF1504ASVL-20 AU44	44A	Industrial (-40°C to +85°C)
			ATF1504ASVL-20 JU44	44J	
			ATF1504ASVL-20 AU100	100A	

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
68J	68-lead, Plastic J-leaded Chip Carrier (PLCC)
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100Q1	100-lead, 14 x 20 mm Body, Plastic Quad Flat Package (PQFP)
100A	100-lead, 14 x 14 mm Body, Thin Profile Plastic Quad Flat Package (TQFP)

44J – PLCC

1.14(0.045) X 45˚   PIN NO. 1   1.14(0.045) X 45˚

IDENTIFIER

0.318(0.0125)
0.191(0.0075)

E1   E

B1   D2/E2

B

e

A2

A1

D1

A

D

0.51(0.020)MAX
45˚ MAX (3X)

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes: 1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion.
Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
and E1 include mold mismatch and are measured at the extreme
material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J	B

68J – PLCC

1.14(0.045) X 45°

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45°

0.318(0.0125)
0.191(0.0075)

B

E1 E

e

D1

D

B1

D2/E2

A2
A1

A

0.51(0.020)MAX
45° MAX (3X)
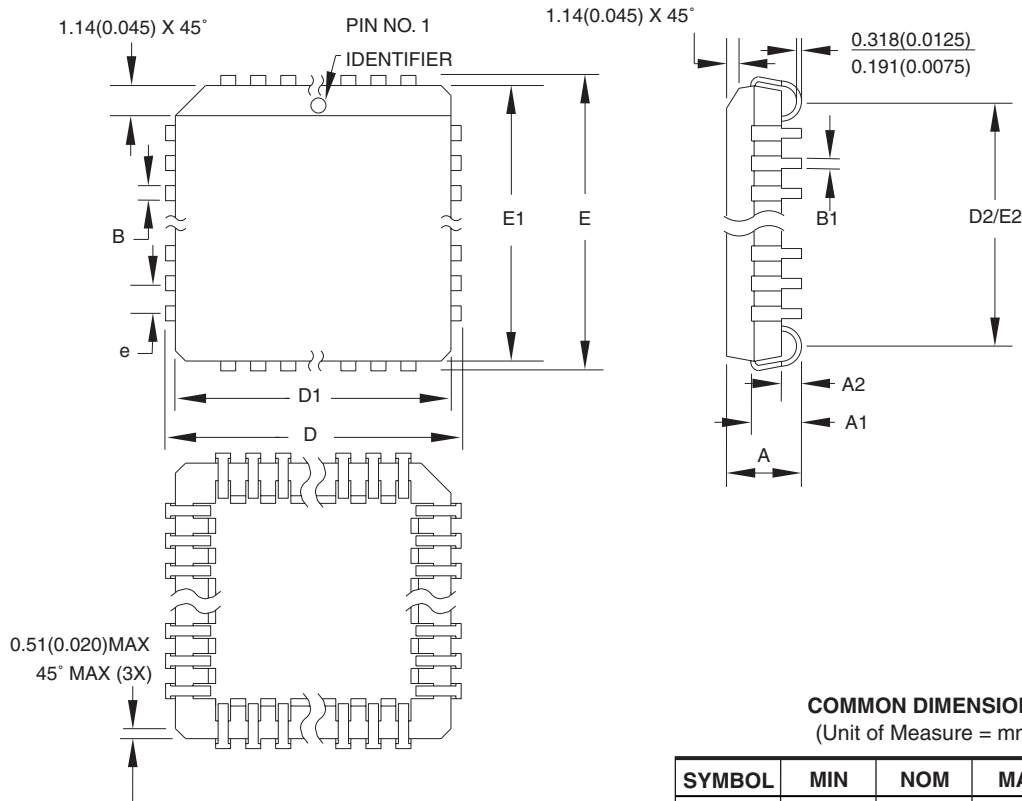
COMMON DIMENSIONS
(Unit of Measure = mm)

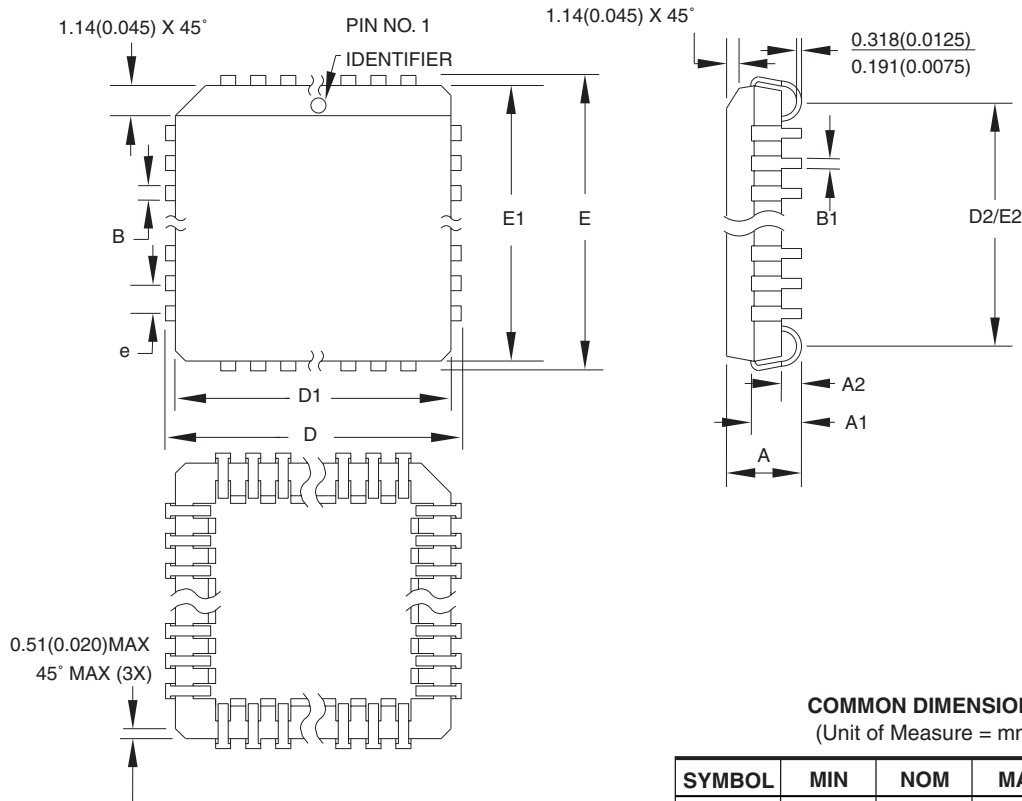| SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	25.019	–	25.273	
D1	24.130	–	24.333	Note 2
E	25.019	–	25.273	
E1	24.130	–	24.333	Note 2
D2/E2	22.606	–	23.622	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes: 1. This package conforms to JEDEC reference MS-018, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion.
Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
and E1 include mold mismatch and are measured at the extreme
material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**68J**, 68-lead, Plastic J-leaded Chip Carrier (PLCC)	68J	B

84J – PLCC

1.14(0.045) X 45˚

PIN NO. 1
IDENTIFIER

1.14(0.045) X 45˚

0.318(0.0125)
0.191(0.0075)

E1   E

B

e

B1

D2/E2

D1

A2

D

A1

A

0.51(0.020)MAX
45˚ MAX (3X)

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes: 1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion.
Allowable protrusion is .010"(0.254 mm) per side. Dimension D1
and E1 include mold mismatch and are measured at the extreme
material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
AMEL 2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

100Q1 – PQFP

PIN 1 ID

PIN 1

E

e

B

D1

D

E1

0º~7º

C

A

L

A1
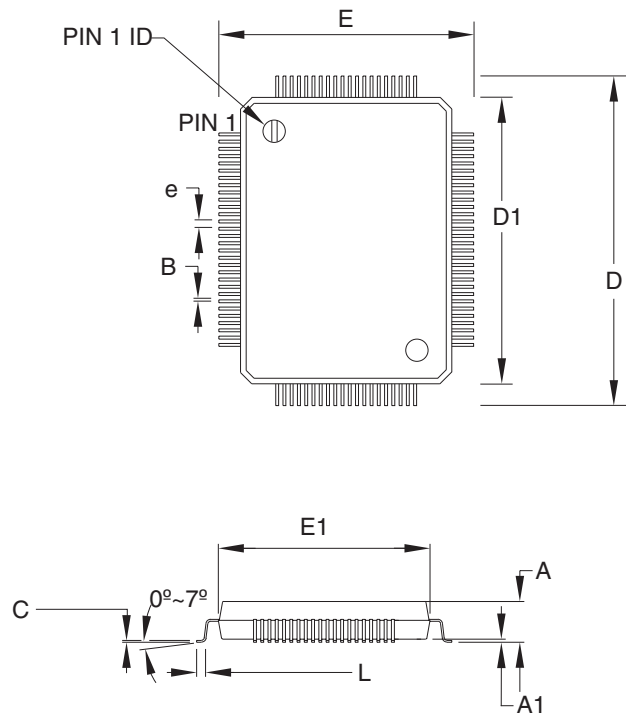
COMMON DIMENSIONS
(Unit of Measure = mm)
JEDEC STANDARD MS-022, GC-1

SYMBOL	MIN	NOM	MAX	NOTE
A	–	3.04	3.4	
A1	0.25	0.33	0.5	
D	23.20 BSC			
E	17.20 BSC			
E1	14.00 BSC			
B	0.22	–	0.40	
D1	20 BSC			
L	0.73	–	1.03	
e	0.65 BSC			

09/10/2002

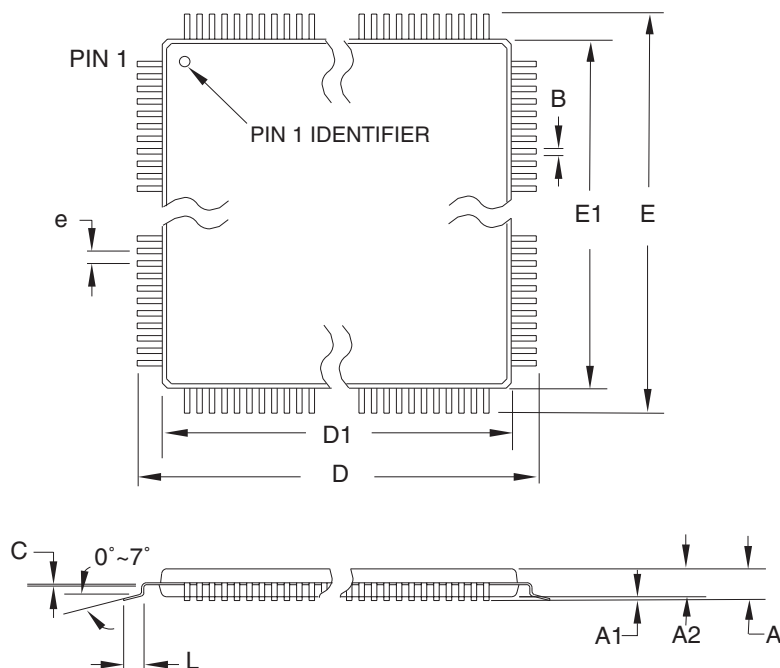|	TITLE	DRAWING NO.	REV.
AMEL 2325 Orchard Parkway San Jose, CA 95131	**100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch, Plastic Quad Flat Package (PQFP)	100Q1	B

ATF1504ASV(L)

100A – TQFP

PIN 1

PIN 1 IDENTIFIER

B

E1 E

e

D1

D

C

0˚~7˚

A1 A2 A

L

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes: 1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable
protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum
plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
AMEL 2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	C