



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

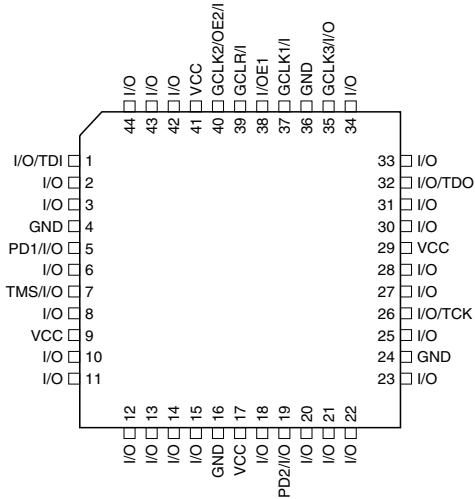
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

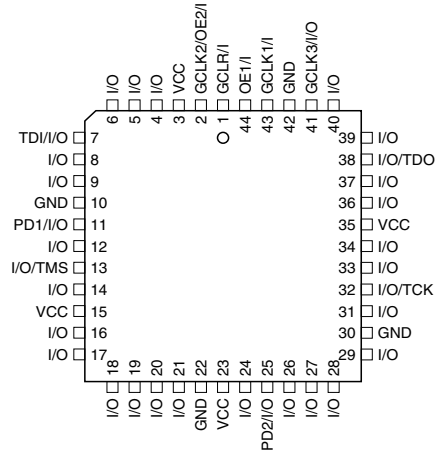
#### Details

Product Status	Obsolete
Programmable Type	In System Programmable (min 10K program/erase cycles)
Delay Time tpd(1) Max	20 ns
Voltage Supply - Internal	3V ~ 3.6V
Number of Logic Elements/Blocks	-
Number of Macrocells	64
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (14x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atf1504asvl-20qi100">https://www.e-xfl.com/product-detail/microchip-technology/atf1504asvl-20qi100</a>

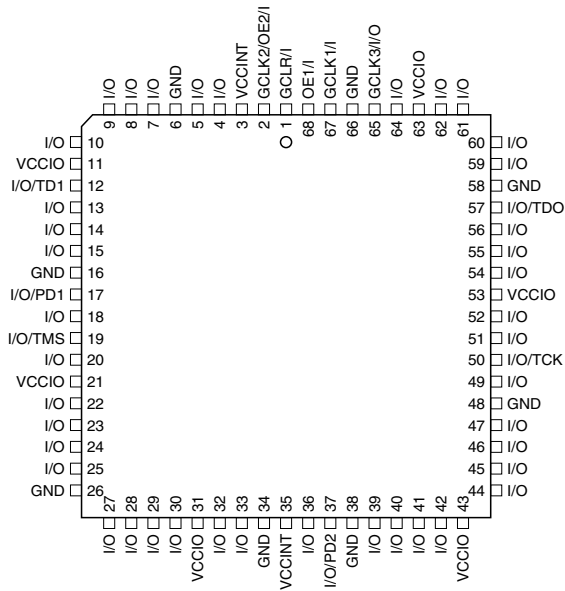
**44-lead TQFP  
Top View**



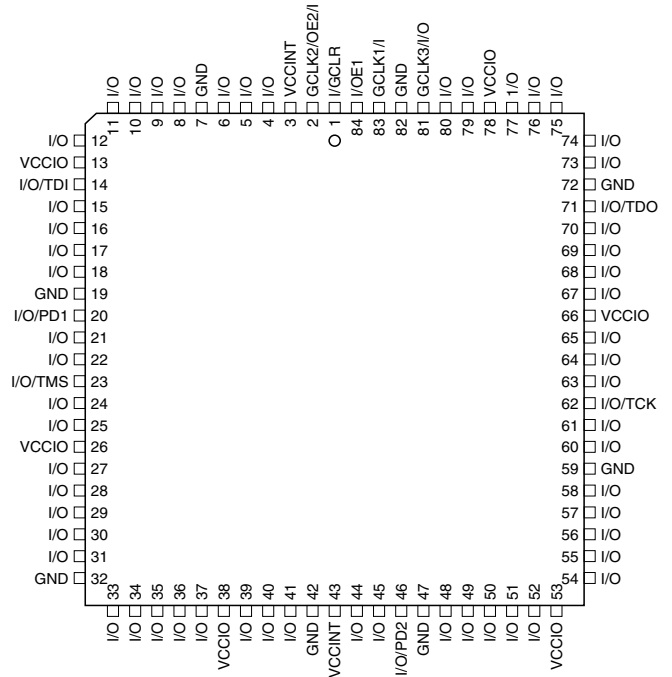
**44-lead PLCC  
Top View**



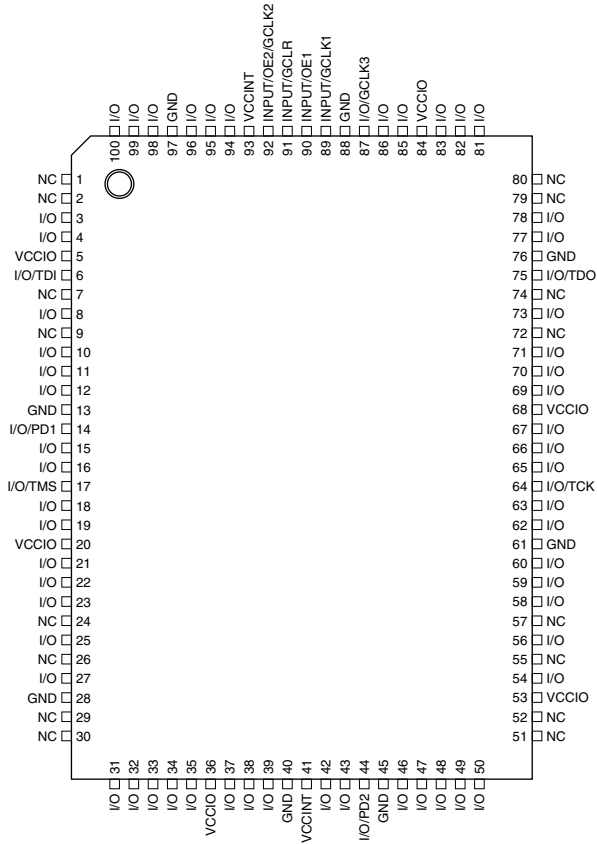
**68-lead PLCC  
Top View**



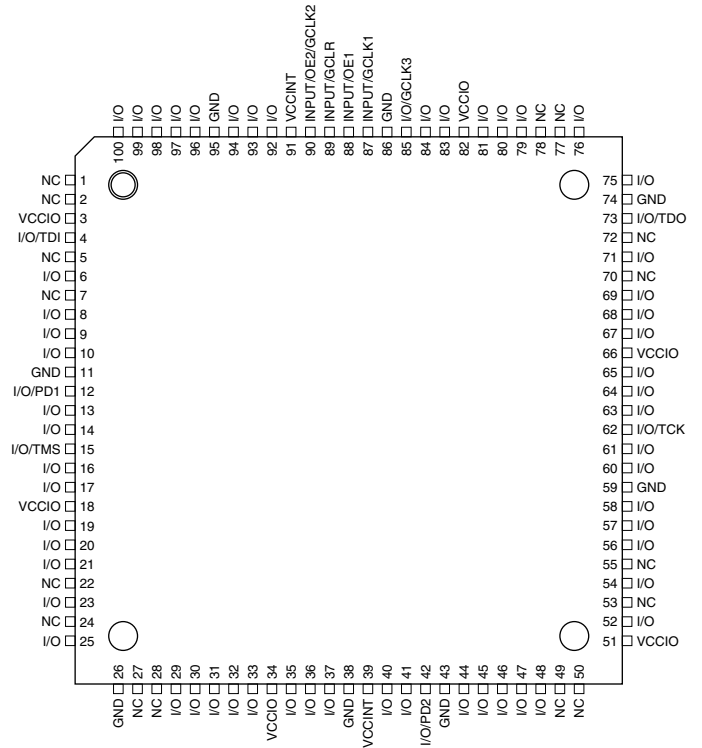
**84-lead PLCC  
Top View**



**100-lead PQFP  
Top View**



**100-lead TQFP  
Top View**



## Description

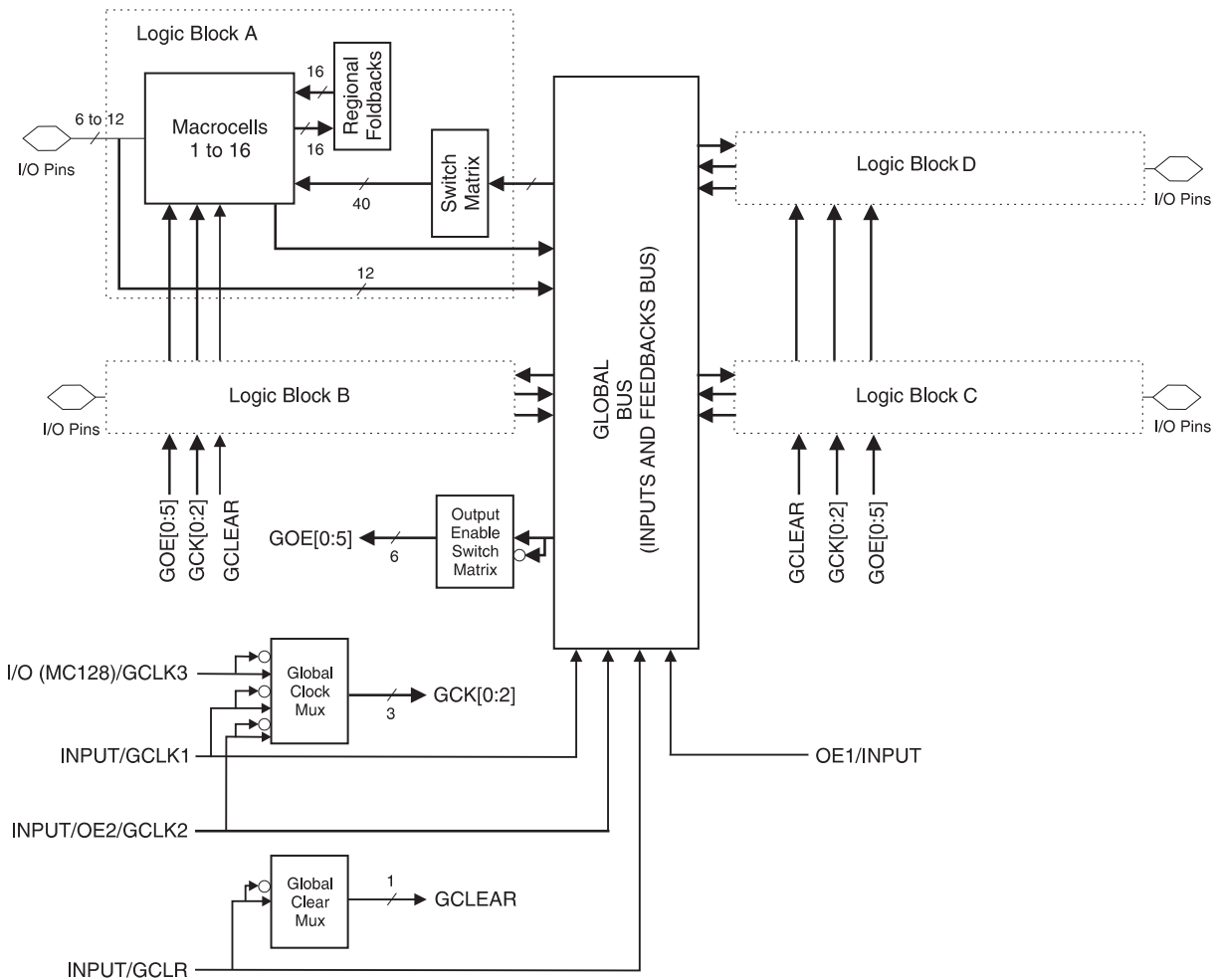
The ATF1504ASV(L) is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable memory technology. With 64 logic macrocells and up to 68 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1504ASV(L)'s enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1504ASV(L) has up to 68 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus. Cascade logic between macrocells in the ATF1504ASV(L) allows fast, efficient generation of complex logic functions. The ATF1504ASV(L) contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

The ATF1504ASV(L) macrocell, shown in Figure 1, is flexible enough to support highly-complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

## Block Diagram



Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1504ASV(L). Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

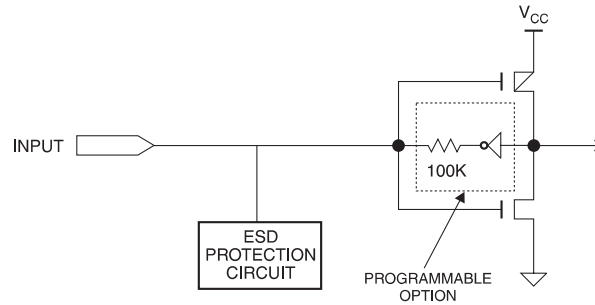
The ATF1504ASV(L) device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully-compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

## Product Terms and Select Mux

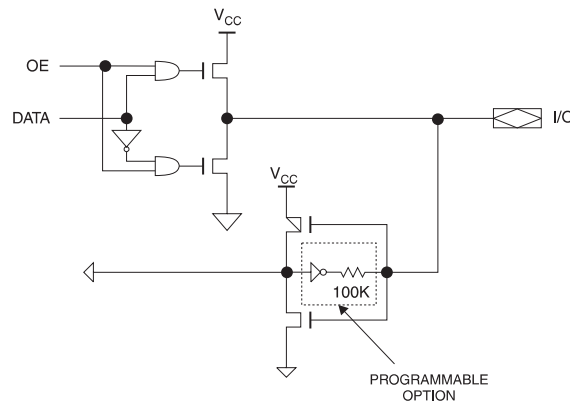
Each ATF1504ASV(L) macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

## Input Diagram



## I/O Diagram



## Speed/Power Management

The ATF1504ASV(L) has several built-in speed and power management features. The ATF1504ASV(L) contains circuitry that automatically puts the device into a low power standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5 MHz. This feature may be selected as a device option.

To further reduce power, each ATF1504ASV(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504ASV(L) also have an optional power-down mode. In this mode, current drops to below 5 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design source file. When enabled, the device goes into power down when either PD1 or PD2 is high. In the power-down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.



## Programming

ATF1504ASV(L) devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Atmel provides ISP hardware and software to allow programming of the ATF1504ASV(L) via the PC. ISP is performed by using either a download cable, a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors. Serial Vector Format (SVF) files can be created by Atmel provided software utilities.

ATF1504ASV(L) devices can also be programmed using standard third-party programmers. With third-party programmer the JTAG ISP port can be disabled thereby allowing four additional I/O pins to be used for logic.

Contact your local Atmel representatives or Atmel PLD applications for details.

## ISP Programming Protection

The ATF1504ASV(L) has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high-Z state during such a condition. In addition the pin keeper option preserves the former state during device programming, if this circuit were previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504ASV(L) is being programmed via ISP.

All ATF1504ASV(L) devices are initially shipped in the erased state thereby making them ready to use for ISP.

Note: For more information refer to the "Designing for In-System Programmability with Atmel CPLDs" application note.

## DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V <sub>CC</sub> (3.3V) Power Supply	3.0V - 3.6V	3.0V - 3.6V

## DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I <sub>IL</sub>	Input or I/O Low Leakage Current	V <sub>IN</sub> = V <sub>CC</sub>				-2	-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current					2	10	
I <sub>OZ</sub>	Tri-State Output Off-State Current	V <sub>O</sub> = V <sub>CC</sub> or GND			-40		40	μA
I <sub>CC1</sub>	Power Supply Current, Standby	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Mode	Com.		60		mA
				Ind.		75		mA
			“L” Mode	Com.		5		μA
				Ind.		5		μA
I <sub>CC2</sub>	Power Supply Current, Power-down Mode	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	“PD” Mode			0.1	5	mA
I <sub>CC3</sub> <sup>(2)</sup>	Reduced-power Mode Supply Current, Standby	V <sub>CC</sub> = Max V <sub>IN</sub> = 0, V <sub>CC</sub>	Std Power	Com		40		ma
				Ind		55		
V <sub>IL</sub>	Input Low Voltage				-0.3		0.8	V
V <sub>IH</sub>	Input High Voltage				1.7		V <sub>CCIO</sub> + 0.3	V
V <sub>OL</sub>	Output Low Voltage (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = Min, I <sub>OL</sub> = 8 mA		Com.			0.45	V
				Ind.			0.45	
	Output Low Voltage (CMOS)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
V <sub>OH</sub>	Output High Voltage - 3.3V (TTL)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = Min, I <sub>OH</sub> = -2.0 mA			2.4			V
	Output High Voltage - 3.3V (CMOS)	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>CCIO</sub> = Min, I <sub>OH</sub> = -0.1 mA			V <sub>CCIO</sub> - 0.2			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.  
2. When microcell reduced-power feature is enabled.

## Pin Capacitance

	Typ	Max	Units	Conditions
C <sub>IN</sub>		8	pF	V <sub>IN</sub> = 0V; f = 1.0 MHz
C <sub>I/O</sub>		8	pF	V <sub>OUT</sub> = 0V; f = 1.0 MHz

Note: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.  
The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.



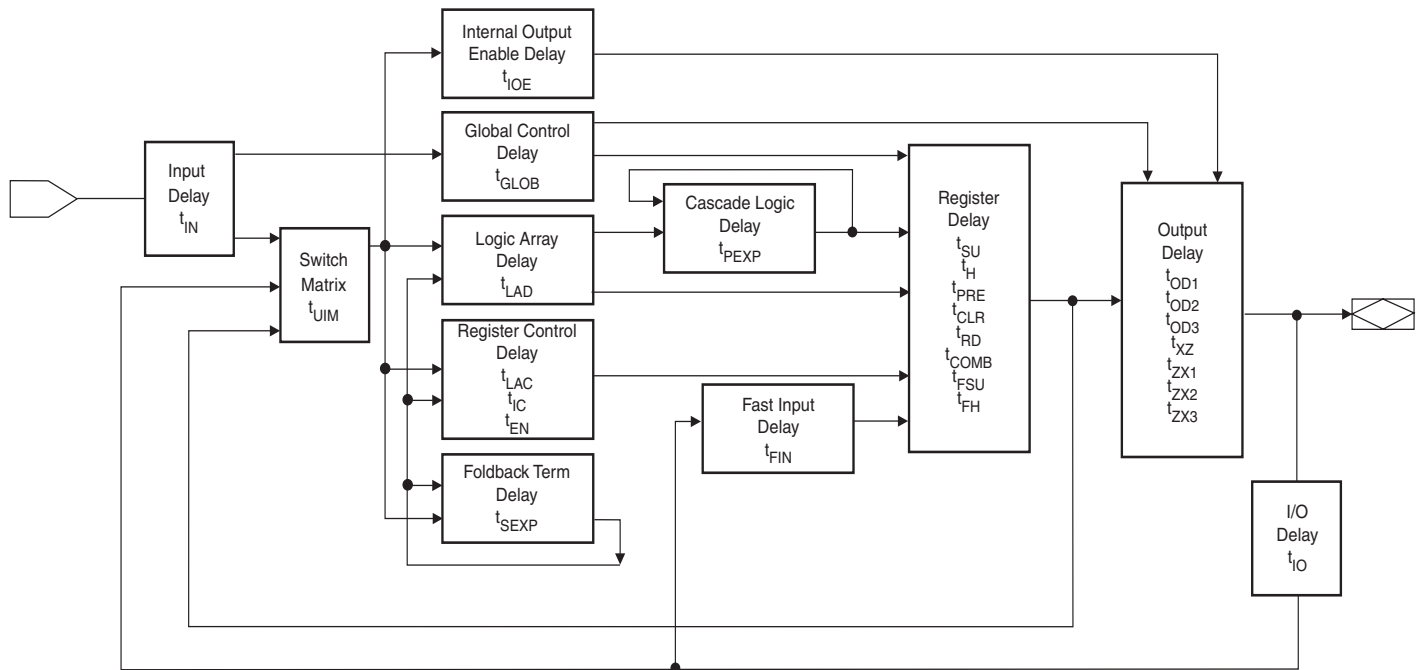
## Absolute Maximum Ratings\*

Temperature Under Bias .....	-40°C to +85°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming .....	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note:** 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20 ns.

## Timing Model



## ATF1504ASV Dedicated Pinouts

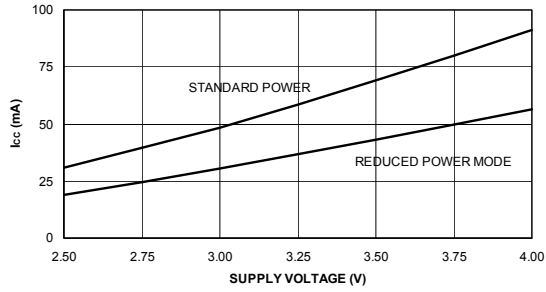
Dedicated Pin	44-lead TQFP	44-lead J-lead	68-lead J-lead	84-lead J-lead	100-lead PQFP	100-lead TQFP
INPUT/OE2/GCLK2	40	2	2	2	92	90
INPUT/GCLR	39	1	1	1	91	89
INPUT/OE1	38	44	68	84	90	88
INPUT/GCLK1	37	43	67	83	89	87
I/O /GCLK3	35	41	65	81	87	85
I/O / PD (1,2)	5, 19	11, 25	17, 37	20, 46	14, 44	12, 42
I/O / TDI (JTAG)	1	7	12	14	6	4
I/O / TMS (JTAG)	7	13	19	23	17	15
I/O / TCK (JTAG)	26	32	50	62	64	62
I/O / TDO (JTAG)	32	38	57	71	75	73
GND	4, 16, 24, 36	10, 22, 30, 42	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	11, 26, 38, 43, 59, 74, 86, 95
V <sub>CC</sub>	9, 17, 29, 41	3, 15, 23, 35	3, 11, 21, 31, 35, 43, 53, 63	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	3, 18, 34, 39, 51, 66, 82, 91
N/C	—	—	—	—	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	52	68	68	68
# User I/O Pins	32	32	48	64	64	64

OE (1, 2) Global OE pins  
 GCLR Global Clear pin  
 GCLK (1, 2, 3) Global Clock pins  
 PD (1, 2) Power-down pins  
 TDI, TMS, TCK, TDO JTAG pins used for boundary-scan testing or in-system programming  
 GND Ground pins  
 VCC VCC pins for the device

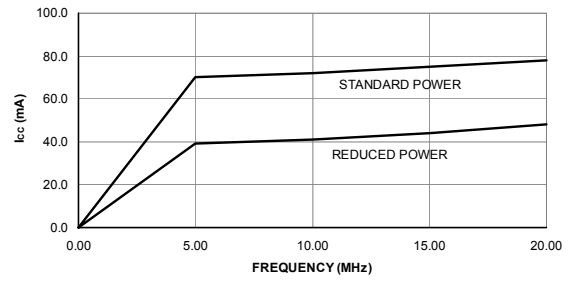
## ATF1504ASV I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100- lead PQFP	100- lead TQFP	MC	PLC	44-lead PLCC	44-lead TQFP	68-lead PLCC	84-lead PLCC	100- lead PQFP	100- lead TQFP
1	A	12	6	18	22	16	14	33	C	24	18	36	44	42	40
2	A	-	-	-	21	15	13	34	C	-	-	-	45	43	41
3	A/ PD1	11	5	17	20	14	12	35	C/ PD2	25	19	37	46	44	42
4	A	9	3	15	18	12	10	36	C	26	20	39	48	46	44
5	A	8	2	14	17	11	9	37	C	27	21	40	49	47	45
6	A	-	-	13	16	10	8	38	C	-	-	41	50	48	46
7	A	-	-	-	15	8	6	39	C	-	-	-	51	49	47
8/ TDI	A	7	1	12	14	6	4	40	C	28	22	42	52	50	48
9	A	-	-	10	12	4	100	41	C	29	23	44	54	54	52
10	A	-	-	-	11	3	99	42	C	-	-	-	55	56	54
11	A	6	44	9	10	100	98	43	C	-	-	45	56	58	56
12	A	-	-	8	9	99	97	44	C	-	-	46	57	59	57
13	A	-	-	7	8	98	96	45	C	-	-	47	58	60	58
14	A	5	43	5	6	96	94	46	C	31	25	49	60	62	60
15	A	-	-	-	5	95	93	47	C	-	-	-	61	63	61
16	A	4	42	4	4	94	92	48/ TCK	C	32	26	50	62	64	62
17	B	21	15	33	41	39	37	49	D	33	27	51	63	65	63
18	B	-	-	-	40	38	36	50	D	-	-	-	64	66	64
19	B	20	14	32	39	37	35	51	D	34	28	52	65	67	65
20	B	19	13	30	37	35	33	52	D	36	30	54	67	69	67
21	B	18	12	29	36	34	32	53	D	37	31	55	68	70	68
22	B	-	-	28	35	33	31	54	D	-	-	56	69	71	69
23	B	-	-	-	34	32	30	55	D	-	-	-	70	73	71
24	B	17	11	27	33	31	29	56/ TDO	D	38	32	57	71	75	73
25	B	16	10	25	31	27	25	57	D	39	33	59	73	77	75
26	B	-	-	-	30	25	23	58	D	-	-	-	74	78	76
27	B	-	-	24	29	23	21	59	D	-	-	60	75	81	79
28	B	-	-	23	28	22	20	60	D	-	-	61	76	82	80
29	B	-	-	22	27	21	19	61	D	-	-	62	77	83	81
30	B	14	8	20	25	19	17	62	D	40	34	64	79	85	83
31	B	-	-	-	24	18	16	63	D	-	-	-	80	86	84
32/ TMS	B	13	7	19	23	17	15	64	D/ GCLK3	41	35	65	81	87	85

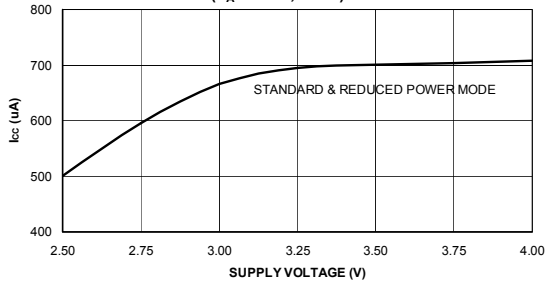
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



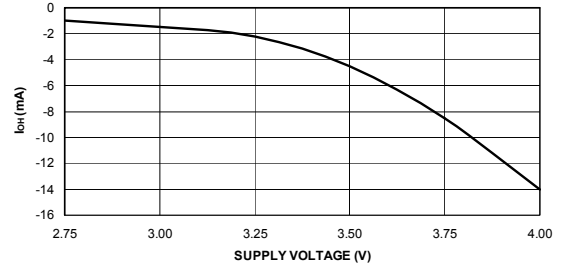
**SUPPLY CURRENT VS. FREQUENCY**  
LOW-POWER ("L") VERSION  
( $T_A = 25^\circ\text{C}$ )



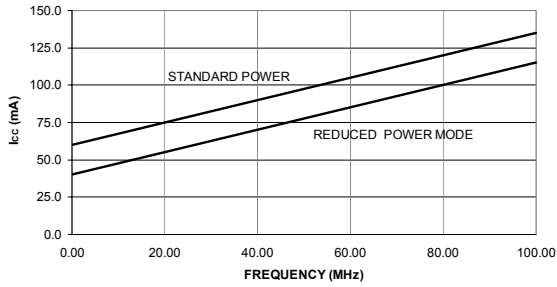
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
PIN-CONTROLLED POWER-DOWN MODE  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



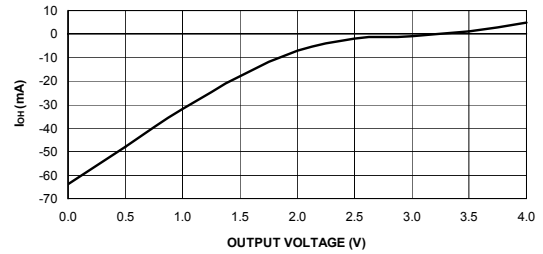
**OUTPUT SOURCE CURRENT**  
VS. SUPPLY VOLTAGE  
( $V_{OH} = 2.4\text{V}$ ,  $T_A = 25^\circ\text{C}$ )



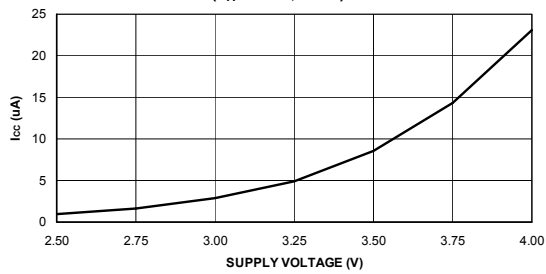
**SUPPLY CURRENT VS. FREQUENCY**  
STANDARD POWER ( $T_A = 25^\circ\text{C}$ )



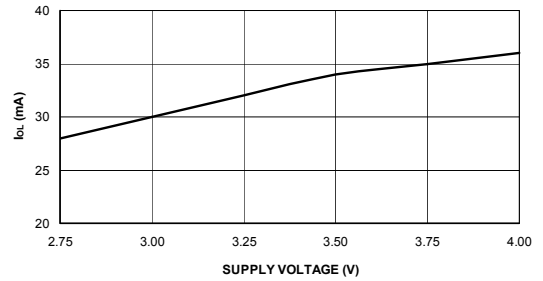
**OUTPUT SOURCE CURRENT**  
VS. OUTPUT VOLTAGE  
( $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$ )



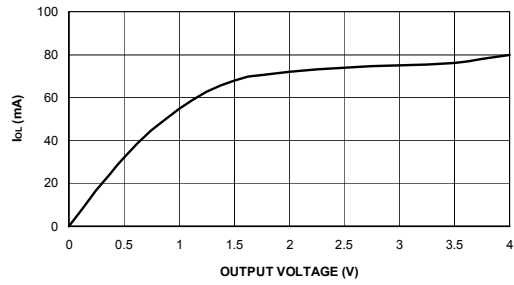
**SUPPLY CURRENT VS. SUPPLY VOLTAGE**  
LOW-POWER ("L") VERSION  
( $T_A = 25^\circ\text{C}$ ,  $F = 0$ )



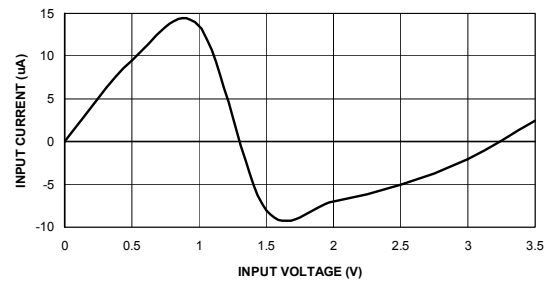
**OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE**  
( $V_{OL} = 0.5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )



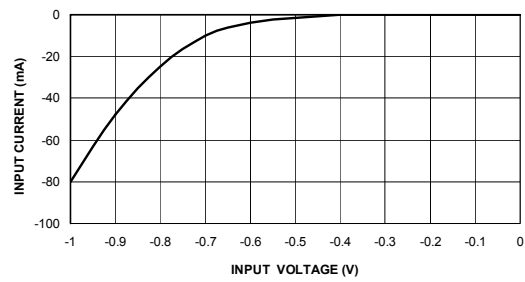
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE  
( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )



INPUT CURRENT VS. INPUT VOLTAGE  
( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )



INPUT CLAMP CURRENT VS. INPUT VOLTAGE  
( $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$ )



## Ordering Information

### ATF1504ASV(L) Standard Package Options

$t_{PD}$ (ns)	$t_{CO1}$ (ns)	$f_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1504ASV-15 AC44	44A	Commercial (0°C to 70°C)
			ATF1504ASV-15 JC44	44J	
			ATF1504ASV-15 JC68 <sup>(2)</sup>	68J	
			ATF1504ASV-15 JC84 <sup>(3)</sup>	84J	
			ATF1504ASV-15 QC100 <sup>(2)</sup>	100Q1	
			ATF1500ASV-15 AC100	100A	
15	8	100	ATF1504ASV-15 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504ASV-15 JI44	44J	
			ATF1504ASV-15 JI68	68J	
			ATF1504ASV-15 JI84	84J	
			ATF1504ASV-15 QI100	100Q1	
			ATF1504ASV-15 AI100	100A	
20	12	83.3	ATF1504ASVL-20 AC44	44A	Commercial (0°C to 70°C)
			ATF1504ASVL-20 JC44	44J	
			ATF1504ASVL-20 JC68 <sup>(2)</sup>	68J	
			ATF1504ASVL-20 JC84 <sup>(3)</sup>	84J	
			ATF1504ASVL-20 QC100 <sup>(2)</sup>	100Q1	
			ATF1504ASVL-20 AC100	100A	
20	12	83.3	ATF1504ASVL-20 AI44	44A	Industrial (-40°C to +85°C)
			ATF1504ASVL-20 JI44	44J	
			ATF1504ASVL-20 JI68	68J	
			ATF1504ASVL-20 JI84	84J	
			ATF1504ASVL-20 QI100	100Q1	
			ATF1504ASVL-20 AI100	100A	

- Note:
1. The last time buy is Sept. 30, 2005 for shaded parts.
  2. The recommended migration for QC100 or JC68 packages is the AU100 or the smaller JU44 packages.
  3. The recommended migration for the JC84 package is the ATF1508ASV-15JU84

### Using “C” Product for Industrial

There is very little risk in using “C” devices for industrial applications because the  $V_{CC}$  conditions for 3.3V products are the same for commercial and industrial (there is only 15°C difference at the high end of the temperature range). To use commercial product for industrial temperature ranges, de-rate  $I_{CC}$  by 15%.

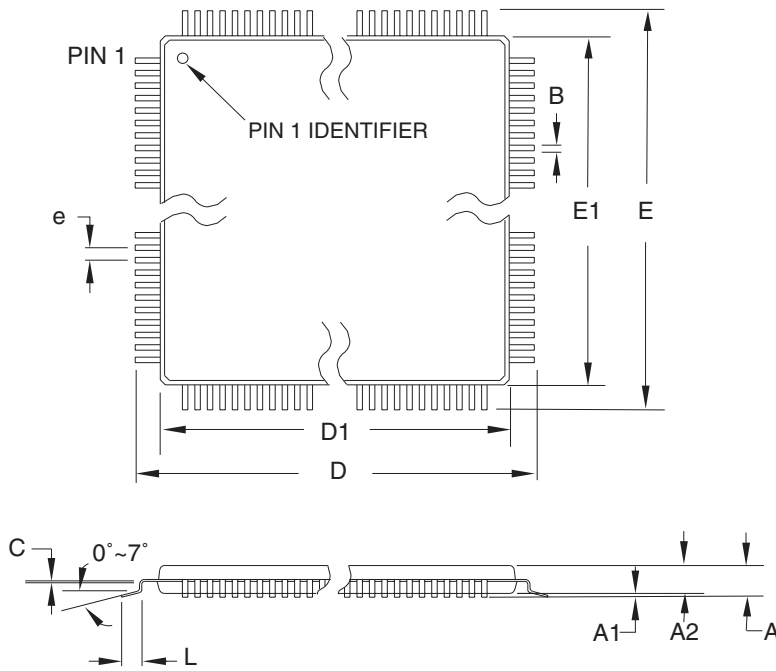
## ATF1504ASV(L) Green Package Options (Pb/Halide-free/RoHS Compliant)

$t_{PD}$ (ns)	$t_{CO1}$ (ns)	$f_{MAX}$ (MHz)	Ordering Code	Package	Operation Range
15	8	100	ATF1504ASV-15 AU44 ATF1504ASV-15 JU44 ATF1504ASV-15 AU100	44A 44J 100A	Industrial (-40°C to +85°C)
20	12	83.3	ATF1504ASVL-20 AU44 ATF1504ASVL-20 JU44 ATF1504ASVL-20 AU100	44A 44J 100A	Industrial (-40°C to +85°C)

Package Type	
<b>44A</b>	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
<b>44J</b>	44-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>68J</b>	68-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>84J</b>	84-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>100Q1</b>	100-lead, 14 x 20 mm Body, Plastic Quad Flat Package (PQFP)
<b>100A</b>	100-lead, 14 x 14 mm Body, Thin Profile Plastic Quad Flat Package (TQFP)

## Packaging Information

### 44A – TQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



2325 Orchard Parkway  
San Jose, CA 95131

#### TITLE

**44A**, 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness,  
0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

#### DRAWING NO.

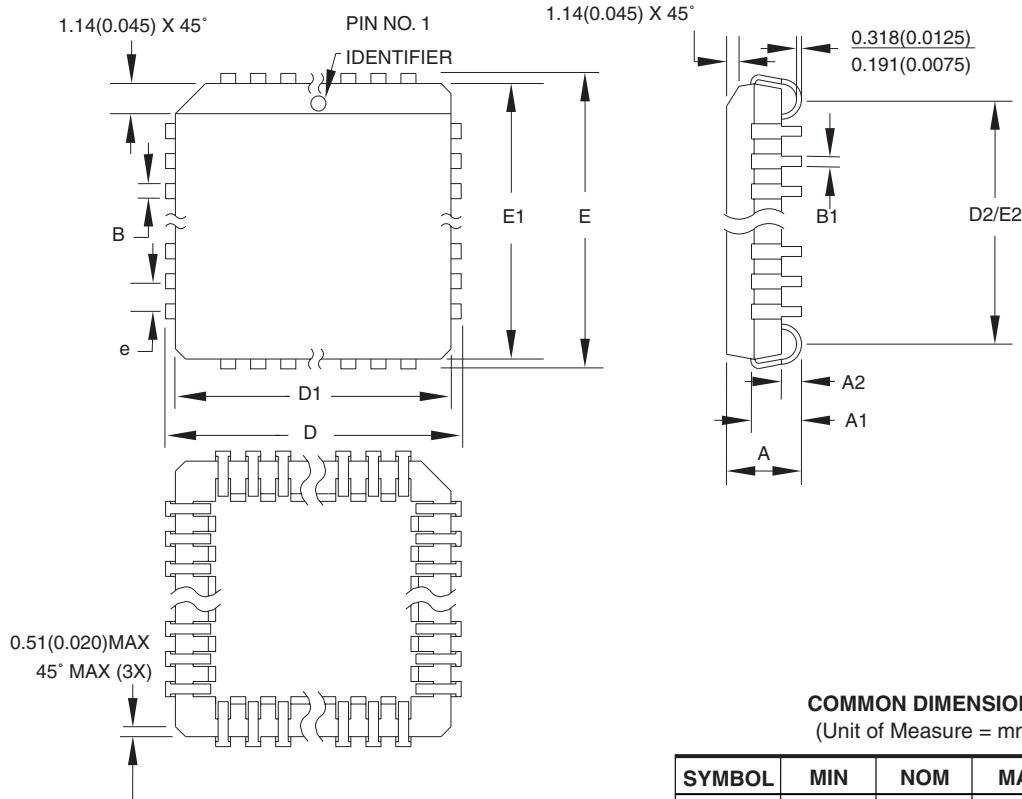
44A

#### REV.

B



84J – PLCC



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	—	4.572	
A1	2.286	—	3.048	
A2	0.508	—	—	
D	30.099	—	30.353	
D1	29.210	—	29.413	Note 2
E	30.099	—	30.353	
E1	29.210	—	29.413	Note 2
D2/E2	27.686	—	28.702	
B	0.660	—	0.813	
B1	0.330	—	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
  3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**84J, 84-lead, Plastic J-leaded Chip Carrier (PLCC)**

**DRAWING NO.**

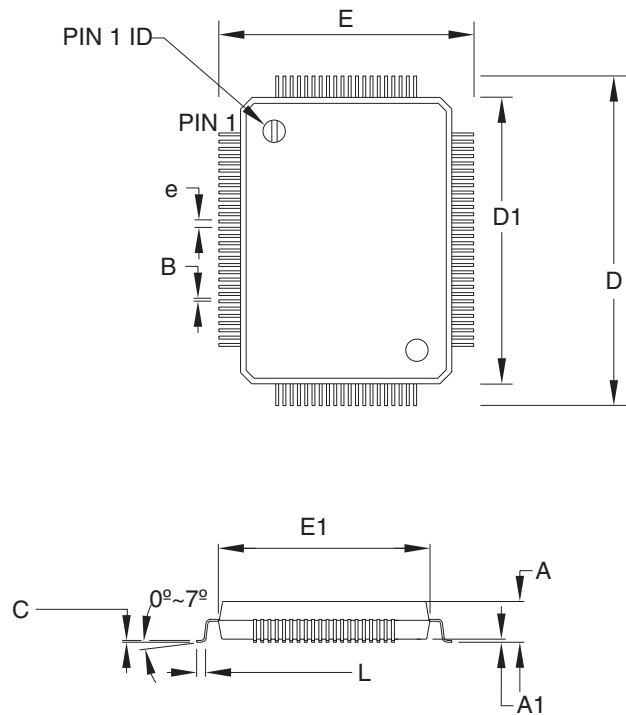
84J

**REV.**

B



# 100Q1 – PQFP



## COMMON DIMENSIONS

(Unit of Measure = mm)

JEDEC STANDARD MS-022, GC-1

SYMBOL	MIN	NOM	MAX	NOTE
A	–	3.04	3.4	
A1	0.25	0.33	0.5	
D	23.20 BSC			
E	17.20 BSC			
E1	14.00 BSC			
B	0.22	–	0.40	
D1	20 BSC			
L	0.73	–	1.03	
e	0.65 BSC			

09/10/2002



2325 Orchard Parkway  
San Jose, CA 95131

## TITLE

**100Q1**, 100-lead, 14 x 20 mm Body, 3.2 mm Footprint, 0.65 mm Pitch,  
Plastic Quad Flat Package (PQFP)

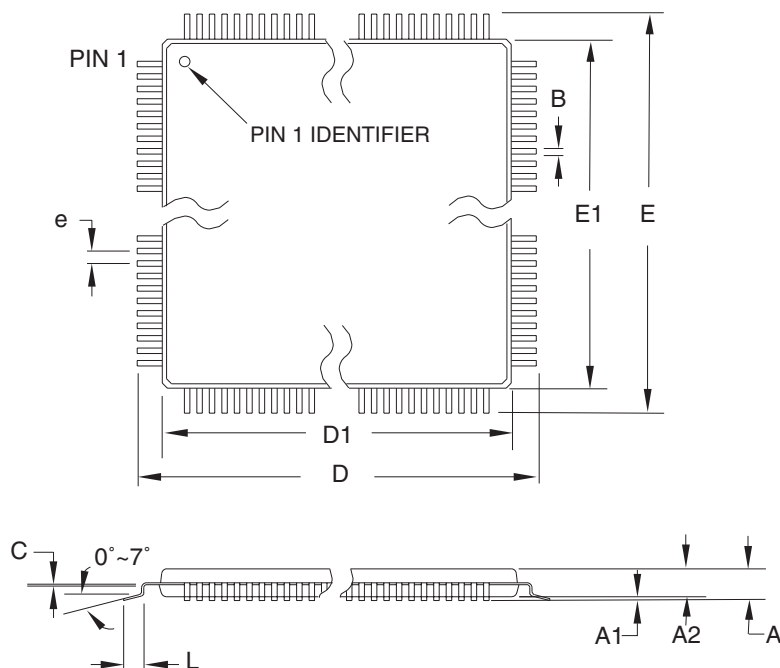
## DRAWING NO.

100Q1

## REV.

B

100A – TQFP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	—	0.27	
C	0.09	—	0.20	
L	0.45	—	0.75	
e	0.50 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
  2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  3. Lead coplanarity is 0.08 mm maximum.

10/5/2001



2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**

**100A**, 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness,  
0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

**DRAWING NO.**

100A

**REV.**

C





## Revision History

Revision	Comments
1409J	Green package options added.



## Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## Regional Headquarters

### Europe

Atmel Sarl  
Route des Arsenalux 41  
Case Postale 80  
CH-1705 Fribourg  
Switzerland  
Tel: (41) 26-426-5555  
Fax: (41) 26-426-5500

### Asia

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

### Japan

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Atmel Operations

### Memory

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

### Microcontrollers

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

La Chantrerie  
BP 70602  
44306 Nantes Cedex 3, France  
Tel: (33) 2-40-18-18-18  
Fax: (33) 2-40-18-19-60

### ASIC/ASSP/Smart Cards

Zone Industrielle  
13106 Rousset Cedex, France  
Tel: (33) 4-42-53-60-00  
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park  
Maxwell Building  
East Kilbride G75 0QR, Scotland  
Tel: (44) 1355-803-000  
Fax: (44) 1355-242-743

### RF/Automotive

Theresienstrasse 2  
Postfach 3535  
74025 Heilbronn, Germany  
Tel: (49) 71-31-67-0  
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

### Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine  
BP 123  
38521 Saint-Egreve Cedex, France  
Tel: (33) 4-76-58-30-00  
Fax: (33) 4-76-58-34-80

---

## Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

**Disclaimer:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© Atmel Corporation 2005. All rights reserved. Atmel®, logo and combinations thereof, Everywhere You Are® and others, are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.



Printed on recycled paper.