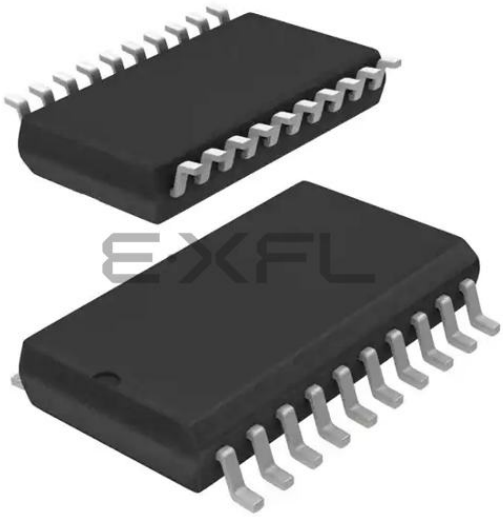

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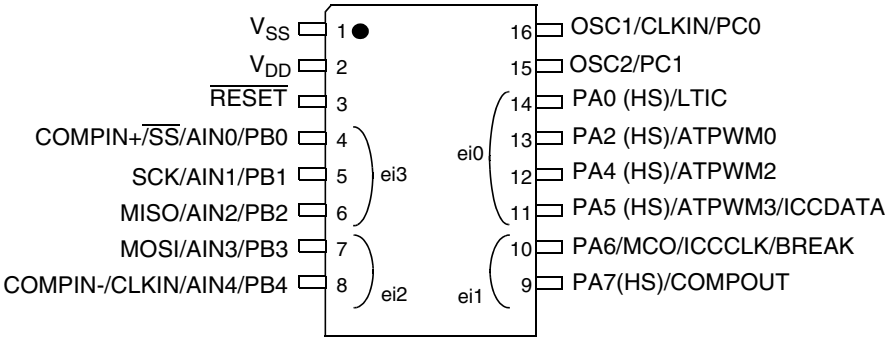
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fli19bf1m3tr

PIN DESCRIPTION (Cont'd)

Figure 4. 16-Pin SO and DIP Package Pinout



(HS) 20mA high sink capability
eix associated external interrupt vector

7.3 REGISTER DESCRIPTION

MAIN CLOCK CONTROL/STATUS REGISTER (MCCSR)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	MCO	SMS

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **MCO** *Main Clock Out enable*
This bit is read/write by software and cleared by hardware after a reset. This bit allows to enable the MCO output clock.
0: MCO clock disabled, I/O port free for general purpose I/O.
1: MCO clock enabled.

Bit 0 = **SMS** *Slow Mode select*
This bit is read/write by software and cleared by hardware after a reset. This bit selects the input clock f_{OSC} or $f_{OSC}/32$.
0: Normal mode ($f_{CPU} = f_{OSC}$
1: Slow mode ($f_{CPU} = f_{OSC}/32$)

RC CONTROL REGISTER (RCCR)
Read / Write
Reset Value: 1111 1111 (FFh)

7							0
CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2

Bits 7:0 = **CR[9:2]** *RC Oscillator Frequency Adjustment Bits*
These bits must be written immediately after reset to adjust the RC oscillator frequency and to obtain an accuracy of 1%. The application can store the correct value for each voltage range in EEPROM and write it to this register at start-up.
00h = maximum available frequency
FFh = lowest available frequency
These bits are used with the CR[1:0] bits in the SICSR register. Refer to section 7.6.4 on page 35.

Note: To tune the oscillator, write a series of different values in the register until the correct frequency is reached. The fastest method is to use a dichotomy starting with 80h.

RESET SEQUENCE MANAGER (Cont'd)

The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

7.5.3 External Power-On RESET

If the LVD is disabled by option byte, to start up the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency.

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the $\overline{\text{RESET}}$ pin.

7.5.4 Internal Low Voltage Detector (LVD) RESET

Two different RESET sequences caused by the internal LVD circuitry can be distinguished:

- Power-On RESET
- Voltage Drop RESET

The device $\overline{\text{RESET}}$ pin acts as an output that is pulled low when $V_{DD}<V_{IT+}$ (rising edge) or $V_{DD}<V_{IT-}$ (falling edge) as shown in Figure 17.

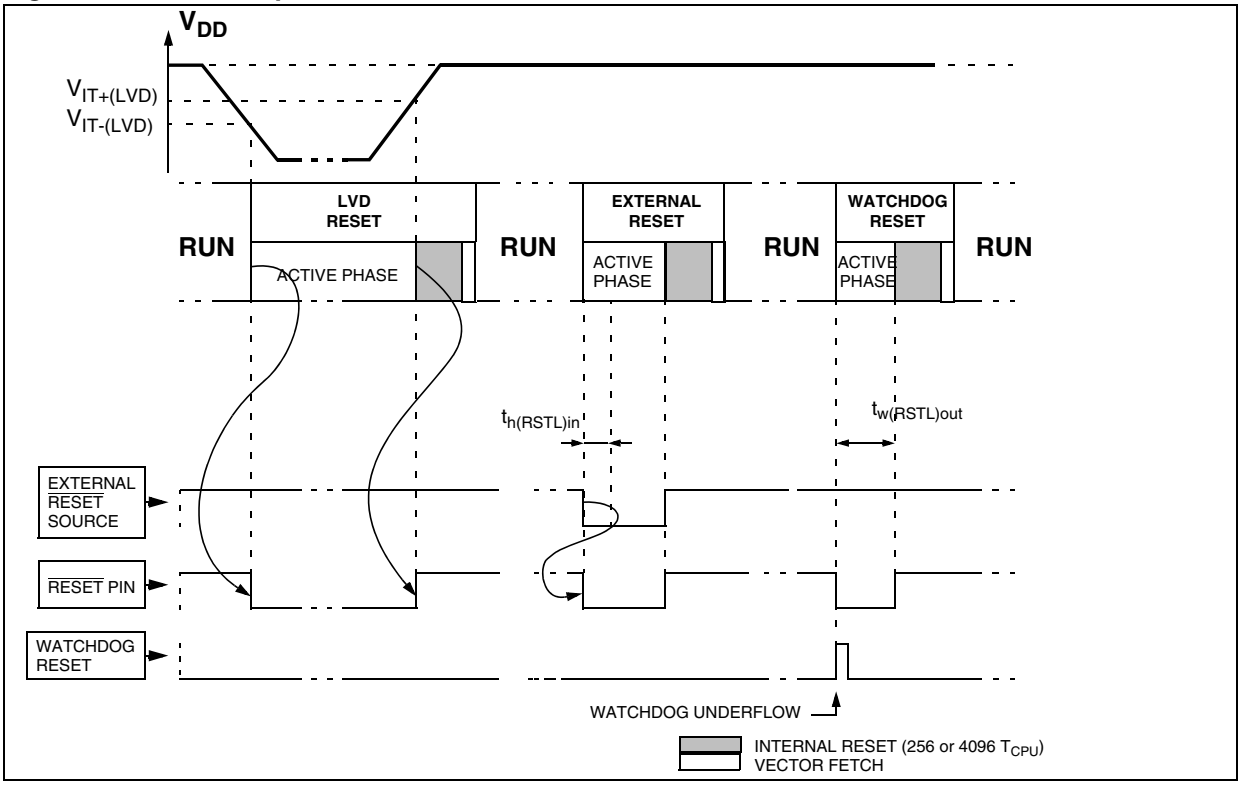
The LVD filters spikes on V_{DD} larger than $t_{g(VDD)}$ to avoid parasitic resets.

7.5.5 Internal Watchdog RESET

The RESET sequence generated by a internal Watchdog counter overflow is shown in Figure 17.

Starting from the Watchdog counter underflow, the device $\overline{\text{RESET}}$ pin acts as an output that is pulled low during at least $t_{w(RSTL)out}$.

Figure 17. RESET Sequences



I/O PORTS (Cont'd)

10.7 DEVICE-SPECIFIC I/O PORT CONFIGURATION

The I/O port register configurations are summarised as follows.

Standard Ports

PA7:0, PB6:0

MODE	DDR	OR
floating input	0	0
pull-up input	0	1
open drain output	1	0
push-pull output	1	1

PC1:0 (multiplexed with OSC1,OSC2)

MODE	DDR
floating input	0
push-pull output	1

The selection between OSC1 or PC0 and OSC2 or PC1 is done by option byte. Refer to section 15.1 on page 149. Interrupt capability is not available on PC1:0.

Note: PCOR not implemented but p-transistor always active in output mode (refer to Figure 32 on page 50)

Interrupt Ports

Ports where the external interrupt capability is selected using the EISR register

MODE	DDR	OR
floating input	0	0
pull-up interrupt input	0	1
open drain output	1	0
push-pull output	1	1

Table 10. Port Configuration (Standard ports)

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	floating	pull-up	open drain	push-pull
Port B	PB6:0	floating	pull-up	open drain	push-pull

Note: On ports where the external interrupt capability is selected using the EISR register, the configuration will be as follows:

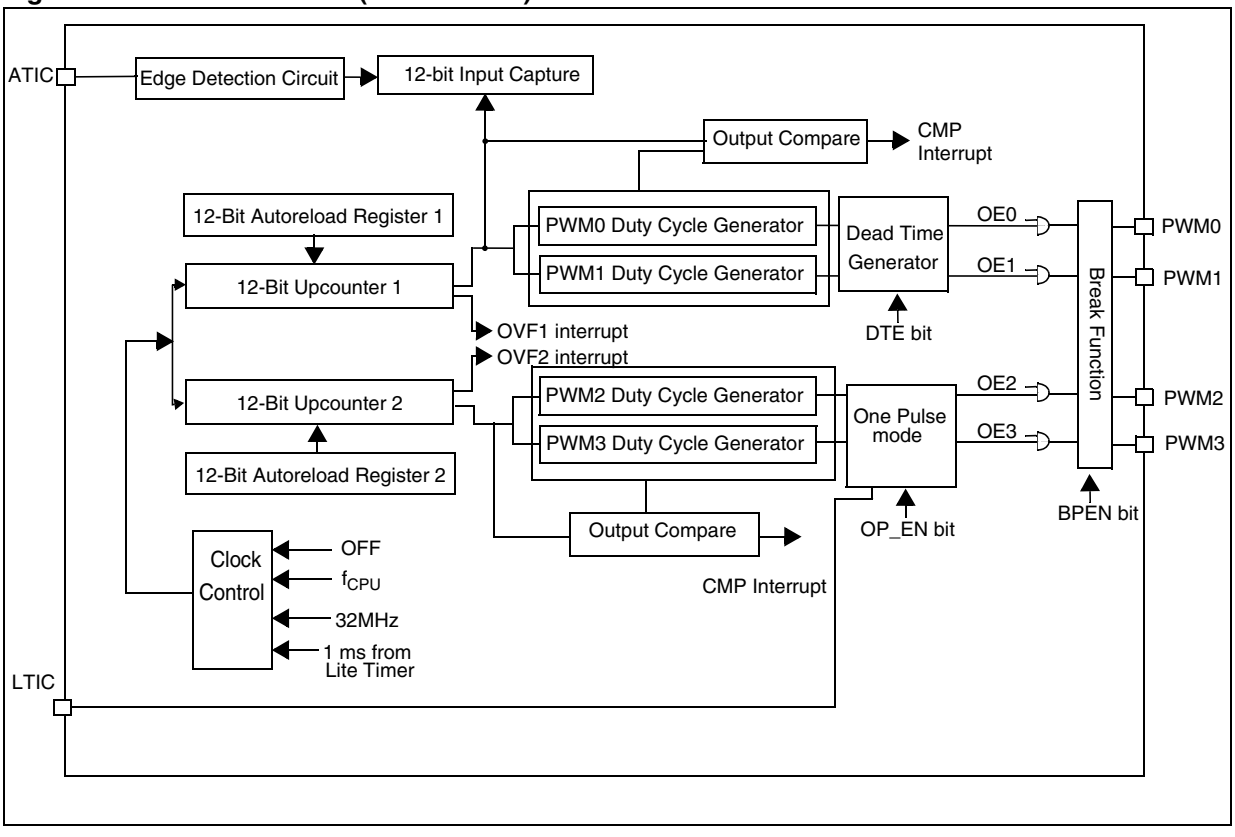
Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	floating	pull-up interrupt	open drain	push-pull
Port B	PB6:0	floating	pull-up interrupt	open drain	push-pull

Table 11. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0000h	**PADR**	MSB							LSB
	Reset Value	1	1	1	1	1	1	1	1
0001h	**PADDR**	MSB							LSB
	Reset Value	0	0	0	0	0	0	0	0

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

Figure 36. Dual Timer Mode (ENCNTR2=1)



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.3.4 Output Compare Mode

To use this function, load a 12-bit value in the Preload DCRxH and DCRxL registers.

When the 12-bit upcounter CNTR1 reaches the value stored in the Active DCRxH and DCRxL registers, the CMPFx bit in the PWMxCSR register is set and an interrupt request is generated if the CMPIE bit is set.

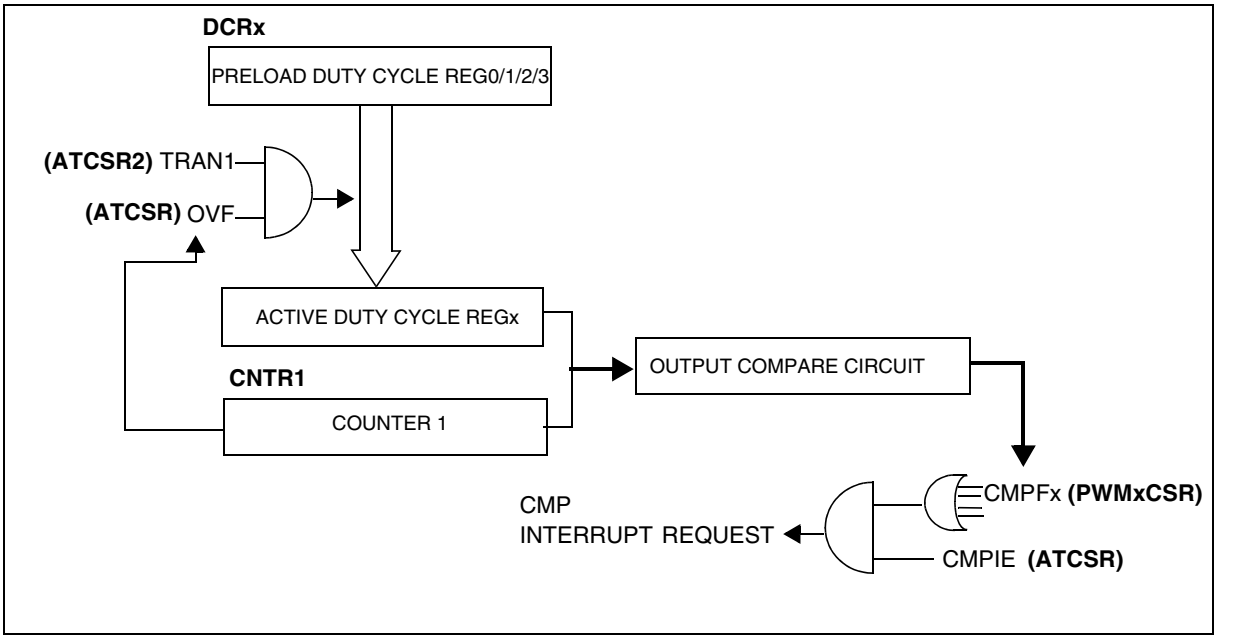
In single Timer mode the output compare function is performed only on CNTR1. The difference between both the modes is that, in Single Timer mode, CNTR1 can be compared with any of the four DCR registers, and in Dual Timer mode, CNTR1 is compared with DCR0 or DCR1 and CNTR2 is compared with DCR2 or DCR3.

Notes:

1. The output compare function is only available for DCRx values other than 0 (reset value).

2. Duty cycle registers are buffered internally. The CPU writes in Preload Duty Cycle Registers and these values are transferred in Active Duty Cycle Registers after an overflow event if the corresponding transfer bit (TRANx bit) is set. Output compare is done by comparing these active DCRx values with the counters.

Figure 42. Block Diagram of Output Compare Mode (single timer)



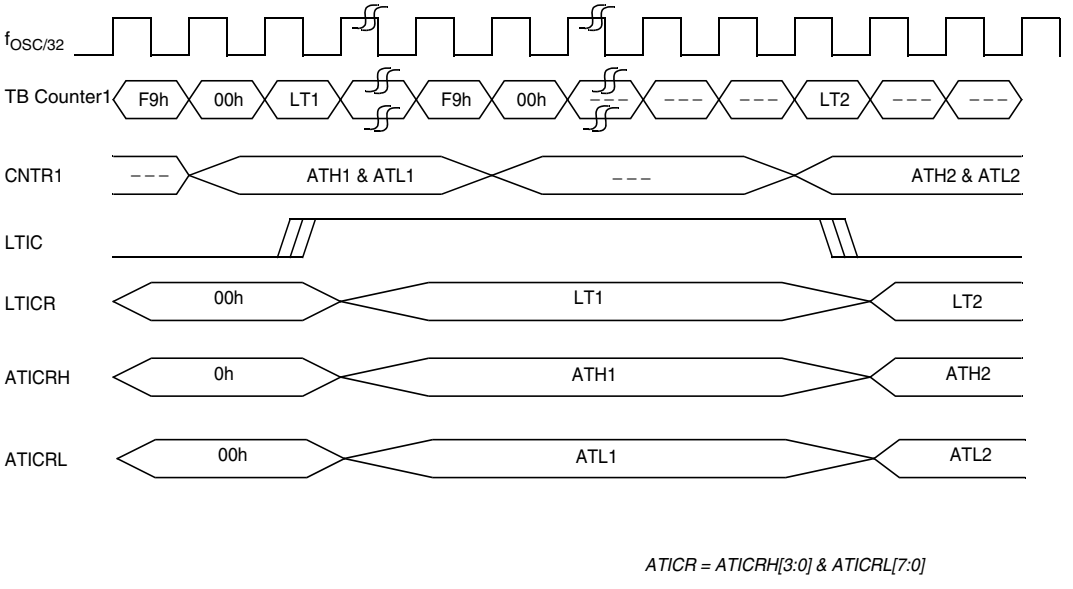
DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

– At the second input capture on the falling edge of the pulse, we assume that the values in the registers are as follows:
LTICR = LT2
ATICRH = ATH2
ATICRL = ATL2
Hence ATICR2 [11:0] = ATH2 & ATL2

Now pulse width P between first capture and second capture will be:

P = decimal (F9 – LT1 + LT2 + 1) * 0.004ms + decimal ((FFF * N) + N + ATICR2 - ATICR1 – 1) * 1ms where N = No of overflows of 12-bit CNTR1.

Figure 46. Long Range Input Capture Timing Diagram



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

BREAK CONTROL REGISTER (BREAKCR)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
BRSEL	BREDGE	BA	BPEN	PWM3	PWM2	PWM1	PWM0

Bit 7 = **BRSEL** *Break Input Selection*
This bit is read/write by software and cleared by hardware after reset. It selects the active Break signal from external BREAK pin and the output of the comparator.

0: External BREAK pin is selected for break mode.

1: Comparator output is selected for break mode.

Bit 6 = **BREDGE** *Break Input Edge Selection*
This bit is read/write by software and cleared by hardware after reset. It selects the active level of Break signal.

0: Low level of Break selected as active level.
1: High level of Break selected as active level.

Bit 5 = **BA** *Break Active.*
This bit is read/write by software, cleared by hardware after reset and set by hardware when the active level defined by the BREDGE bit is applied on the BREAK pin. It activates/deactivates the Break function.
0: Break not active
1: Break active

Bit 4 = **BPEN** *Break Pin Enable.*
This bit is read/write by software and cleared by hardware after Reset.
0: Break pin disabled
1: Break pin enabled

Bits 3:0 = **PWM[3:0]** *Break Pattern.*
These bits are read/write by software and cleared by hardware after a reset. They are used to force the four PWMx output signals into a stable state when the Break function is active and corresponding OEx bit is set.

PWMx DUTY CYCLE REGISTER HIGH (DCRxH)
Read / Write
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	DCR11	DCR10	DCR9	DCR8

Bits 15:12 = Reserved.

PWMx DUTY CYCLE REGISTER LOW (DCRxL)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
DCR7	DCR6	DCR5	DCR4	DCR3	DCR2	DCR1	DCR0

Bits 11:0 = **DCRx[11:0]** *PWMx Duty Cycle Value*
This 12-bit value is written by software. It defines the duty cycle of the corresponding PWM output signal (see Figure 4).

In PWM mode (OEx=1 in the PWMCR register) the DCR[11:0] bits define the duty cycle of the PWMx output signal (see Figure 4). In Output Compare mode, they define the value to be compared with the 12-bit upcounter value.

INPUT CAPTURE REGISTER HIGH (ATICRH)
Read only
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ICR11	ICR10	ICR9	ICR8

Bits 15:12 = Reserved.

INPUT CAPTURE REGISTER LOW (ATICRL)
Read only
Reset Value: 0000 0000 (00h)

7							0
ICR7	ICR6	ICR5	ICR4	ICR3	ICR2	ICR1	ICR0

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

Bits 11:0 = **ICR[11:0]** *Input Capture Data*.
This is a 12-bit register which is readable by software and cleared by hardware after a reset. The ATICR register contains captured the value of the 12-bit CNTR1 register when a rising or falling edge occurs on the ATIC or LTIC pin (depending on

ICS). Capture will only be performed when the ICF flag is cleared.

BREAK ENABLE REGISTER (BREAKEN)

Read/Write
Reset Value: 0000 0011 (03h)

7							0
0	0	0	0	0	0	BREN2	BREN1

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **BREN2** *Break Enable for Counter 2*
This bit is read/write by software. It enables the break functionality for Counter2 if BA bit is set in BREAKCR. It controls PWM2/3 if ENCNTR2 bit is set.
0: No Break applied for CNTR2
1: Break applied for CNTR2

Bit 0 = **BREN1** *Break Enable for Counter 1*
This bit is read/write by software. It enables the break functionality for Counter1. If BA bit is set, it controls PWM0/1 by default, and controls PWM2/3 also if ENCNTR2 bit is reset.
0: No Break applied for CNTR1
1: Break applied for CNTR1

TIMER CONTROL REGISTER2 (ATCSR2)
Read/Write
Reset Value: 0000 0011 (03h)

7							0
FORCE 2	FORCE 1	ICS	OVFIE2	OVF2	ENCNT R2	TRAN2	TRAN1

Bit 7 = **FORCE2** *Force Counter 2 Overflow*
This bit is read/set by software. When set, it loads FFFh in the CNTR2 register. It is reset by hardware one CPU clock cycle after counter 2 overflow has occurred.

0 : No effect on CNTR2
1 : Loads FFFh in CNTR2

Note: This bit must not be reset by software

Bit 6 = **FORCE1** *Force Counter 1 Overflow*
This bit is read/set by software. When set, it loads FFFh in CNTR1 register. It is reset by hardware one CPU clock cycle after counter 1 overflow has occurred.

0 : No effect on CNTR1
1 : Loads FFFh in CNTR1

Note: This bit must not be reset by software

Bit 5 = **ICS** *Input Capture Shorted*
This bit is read/write by software. It allows the AT-timer CNTR1 to use the LTIC pin for long input capture.
0 : ATIC for CNTR1 input capture
1 : LTIC for CNTR1 input capture

Bit 4 = **OVFIE2** *Overflow interrupt 2 enable*
This bit is read/write by software and controls the overflow interrupt of counter2.
0: Overflow interrupt disabled.
1: Overflow interrupt enabled.

Bit 3 = **OVF2** *Overflow Flag.*
This bit is set by hardware and cleared by software by reading the ATCSR2 register. It indicates the transition of the counter2 from FFFh to ATR2 value.
0: No counter overflow occurred
1: Counter overflow occurred

Bit 2 = **ENCNTR2** *Enable counter2* for PWM2/3

This bit is read/write by software and switches the PWM2/3 operation to the CNTR2 counter. If this bit is set, PWM2/3 will be generated using CNTR2.
0: PWM2/3 is generated using CNTR1.
1: PWM2/3 is generated using CNTR2.

Note: Counter 2 gets frozen when the ENCNTR2 bit is reset. When ENCNTR2 is set again, the counter will restart from the last value.

ANALOG COMPARATOR (Cont'd)

Figure 61. Analog Comparator and Internal Voltage Reference

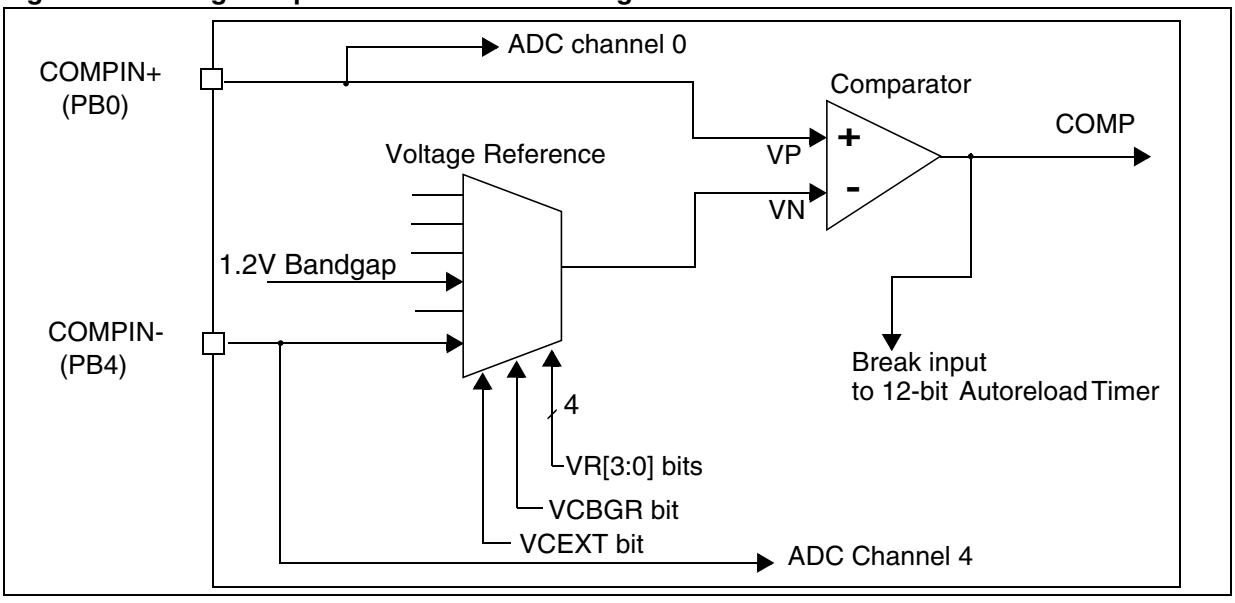
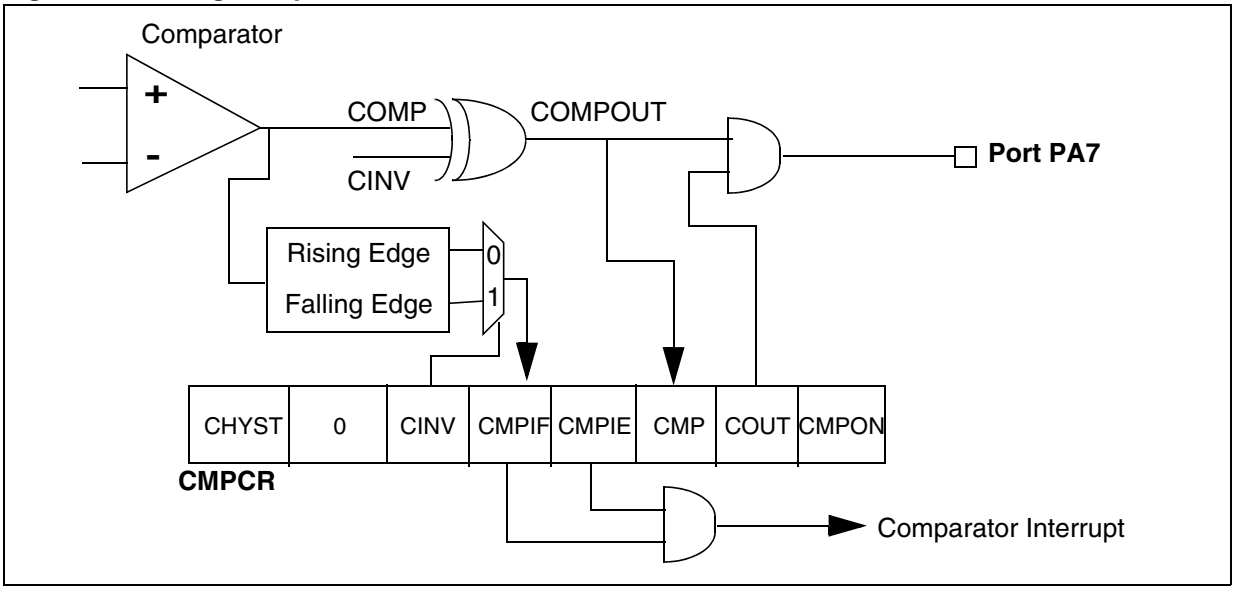


Figure 62. Analog Comparator



ANALOG COMPARATOR (Cont'd)

Bit 4 = **CMPIF** *Comparator Interrupt Flag*

This bit is set by hardware when interrupt is generated at the rising edge (CINV = 0) or falling edge (CINV = 1) of comparator output. This bit is cleared by reading the CMPCR register. Writing to this bit does not change the value.
0 : Comparator interrupt flag cleared
1 : Comparator interrupt flag set and can generate interrupt if CMPIE is set.

Bit 3 : **CMPIE** *Comparator Interrupt Enable*

This bit is set or reset by software and cleared by hardware reset. This bit enables or disables the interrupt generation depending on interrupt flag
0: Interrupt not generated
1: Interrupt generated if interrupt flag is set

Note:

This bit should be set to enable interrupt only after the comparator has been switched ON, i.e. when CMPON is set.

Once CMPON bit is set, it is recommended to wait the specified stabilization time before setting CMPIE bit in order to avoid a spurious interrupt (see section 13.12 on page 143).

Bit 2 : **CMP** *Comparator Output*

This bit is set or reset by software and cleared by hardware reset. It stores the value of comparator output.

Bit 1 = **COUT** *Comparator Output Enable on Port*
This bit is set or cleared by software. When this bit is set, the comparator output is available on PA7 port.
0 : Comparator output not connected to PA7
1 : Comparator output connected to PA7

Bit 0 : **CMPON** *Comparator ON/OFF*
This bit is set or cleared by software and reset by hardware reset. This bit is used to switch ON/OFF the comparator, internal voltage reference and current bias which provides 4µA current to both.
0: Comparator, Internal Voltage Reference, Bias OFF (in power-down state).
1: Comparator, Internal Voltage Reference, Bias ON

Note: For the comparator interrupt generation, it takes 250ns delay from comparator output change to rising or falling edge of interrupt generated.

Table 21. Analog Comparator Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Ch	**VREFCR**	VCEXT	VCBGR	VR3	VR2	VR1	VR0	-	-
	Reset Value	0	0	0	0	0	0	0	0
002Dh	**CMPCR**	CHYST	-	CINV	CMPIF	CMPIE	CMP	COUT	CMPON
	Reset value	1	0	0	0	0	0	0	0

INSTRUCTION GROUPS (cont'd)

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
JRULE	Jump if (C + Z = 1)	Unsigned <=							
LD	Load	dst <= src	reg, M	M, reg			N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0				0
NEG	Negate (2's compl)	neg $10	reg, M				N	Z	C
NOP	No Operation								
OR	OR operation	A = A + M	A	M			N	Z	
POP	Pop from the Stack	pop reg	reg	M					
		pop CC	CC	M	H	I	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC					
RCF	Reset carry flag	C = 0							0
RET	Subroutine Return								
RIM	Enable Interrupts	I = 0				0			
RLC	Rotate left true C	C <= Dst <= C	reg, M				N	Z	C
RRC	Rotate right true C	C => Dst => C	reg, M				N	Z	C
RSP	Reset Stack Pointer	S = Max allowed							
SBC	Subtract with Carry	A = A - M - C	A	M			N	Z	C
SCF	Set carry flag	C = 1							1
SIM	Disable Interrupts	I = 1				1			
SLA	Shift left Arithmetic	C <= Dst <= 0	reg, M				N	Z	C
SLL	Shift left Logic	C <= Dst <= 0	reg, M				N	Z	C
SRL	Shift right Logic	0 => Dst => C	reg, M				0	Z	C
SRA	Shift right Arithmetic	Dst7 => Dst => C	reg, M				N	Z	C
SUB	Subtraction	A = A - M	A	M			N	Z	C
SWAP	SWAP nibbles	Dst[7..4] <=> Dst[3..0]	reg, M				N	Z	
TNZ	Test for Neg & Zero	tnz lbl1					N	Z	
TRAP	S/W trap	S/W interrupt				1			
WFI	Wait for Interrupt					0			
XOR	Exclusive OR	A = A XOR M	A	M			N	Z	

13.6 MEMORY CHARACTERISTICS

T_A = -40°C to 125°C, unless otherwise specified

13.6.1 RAM and Hardware Registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode [1]	HALT mode (or RESET)	1.6			V

13.6.2 FLASH Program Memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage for Flash write/erase	Refer to operating range of V_{DD} with T_A, section 13.3.1 on page 112	2.7		5.5	V
t_{prog}	Programming time for 1~32 bytes [2]	T_A=–40 to +125°C		5	10	ms
	Programming time for 1.5 kBytes	T_A=+25°C		0.24	0.48	s
t_{RET}	Data retention [4]	T_A=+55°C[3]	20			years
N_{RW}	Write erase cycles	T_A=+25°C	10K			cycles
I_{DD}	Supply current [6]	Read / Write / Erase modes f_{CPU} = 8MHz, V_{DD} = 5.5V			2.6	mA
		No Read/No Write Mode			100	µA
		Power down mode / HALT		0	0.1	µA

13.6.3 EEPROM Data Memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage for EEPROM write/erase	Refer to operating range of V_{DD} with T_A, section 13.3.1 on page 112	2.7		5.5	V
t_{prog}	Programming time for 1~32 bytes	T_A=–40 to +125°C		5	10	ms
t_{ret}	Data retention [4]	T_A=+55°C [3]	20			years
N_{RW}	Write erase cycles	T_A=+25°C	300K			cycles

Notes:

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in HALT mode or under RESET) or in hardware registers (only in HALT mode). Guaranteed by construction, not tested in production.

2. Up to 32 bytes can be programmed at a time.

3. The data retention time increases when the T_A decreases.

4. Data based on reliability test results and monitored in production.

5. Data based on characterization results, not tested in production.

6. Guaranteed by Design. Not tested in production.

13.8 I/O PORT PIN CHARACTERISTICS

13.8.1 General Characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage			V_{SS} - 0.3		0.3xV_{DD}	V
V_{IH}	Input high level voltage			0.7xV_{DD}		V_{DD} + 0.3	
V_{hys}	Schmitt trigger voltage hysteresis [1]				400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$				±1	µA
I_S	Static current consumption induced by each floating input pin [2]	Floating input mode			400		
R_{PU}	Weak pull-up equivalent resistor [3]	$V_{IN}=V_{SS}$	V_{DD}=5V	50	120	250	kΩ
			V_{DD}=3V		160		
C_{IO}	I/O pin capacitance				5		pF
$t_{f(IO)out}$	Output high to low level fall time [1]	C_L=50pF Between 10% and 90%			25		ns
$t_{r(IO)out}$	Output low to high level rise time [1]				25		
$t_{w(IT)in}$	External interrupt pulse time [4]			1			t_{CPU}

Notes:

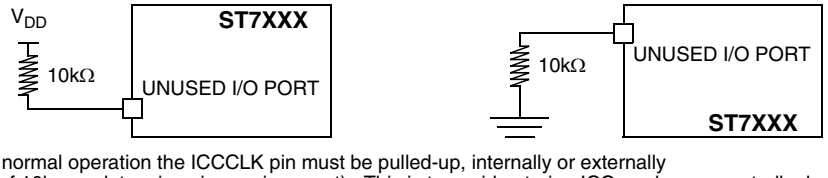
1. Data based on validation/design results.

2. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see Figure 80). Static peak current value taken at a fixed V_{IN} value, based on design simulation and technology characteristics, not tested in production. This value depends on V_{DD} and temperature values.

3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.

4. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 80. Two typical Applications with unused I/O Pin



Caution: During normal operation the ICCCLK pin must be pulled-up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset.
Note: I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

I/O PORT PIN CHARACTERISTICS (Cont'd)

13.8.2 Output Driving Current

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL} 1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 83)	V_{DD}=5V	I_{IO}=+5mA $T_A \leq 125°C$		1.0	V
			I_{IO}=+2mA $T_A \leq 125°C$		0.4	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 89)		I_{IO}=+20mA,$T_A \leq 125°C$		1.3	
			I_{IO}=+8mA $T_A \leq 125°C$		0.75	
V_{OH} 2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 95)		I_{IO}=-5mA, $T_A \leq 125°C$	V_{DD}-1.5		
			I_{IO}=-2mA $T_A \leq 125°C$	V_{DD}-0.8		
V_{OL} 1)3)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 82)	V_{DD}=3.3V	I_{IO}=+2mA $T_A \leq 125°C$		0.5	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time		I_{IO}=+8mA $T_A \leq 125°C$		0.5	
V_{OH} 2)3)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (Figure 94)		I_{IO}=-2mA $T_A \leq 125°C$	V_{DD}-0.8		
V_{OL} 1)3)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 87)	V_{DD}=2.7V	I_{IO}=+2mA $T_A \leq 125°C$		0.6	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time		I_{IO}=+8mA $T_A \leq 125°C$		0.6	
V_{OH} 2)3)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 101)		I_{IO}=-2mA $T_A \leq 125°C$	V_{DD}-0.9		

Notes:

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

2. The I_{IO} current sourced must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.

3. Not tested in production, based on characterization results.

I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 81. Typical V_{OL} at V_{DD}=2.7V (standard)

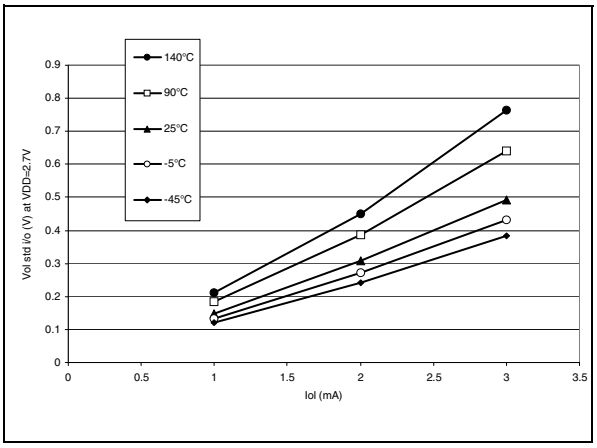


Figure 82. Typical V_{OL} at V_{DD}=3.3V (standard)

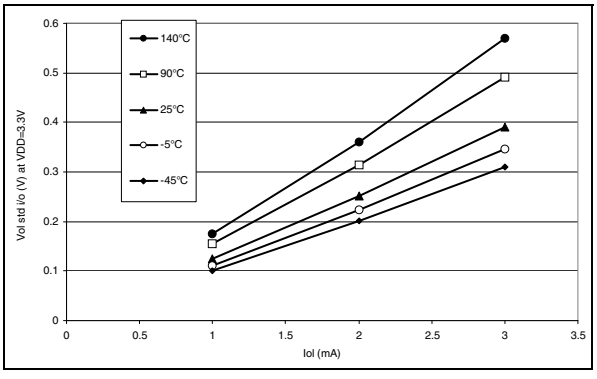


Figure 83. Typical V_{OL} at V_{DD}=5V (standard)

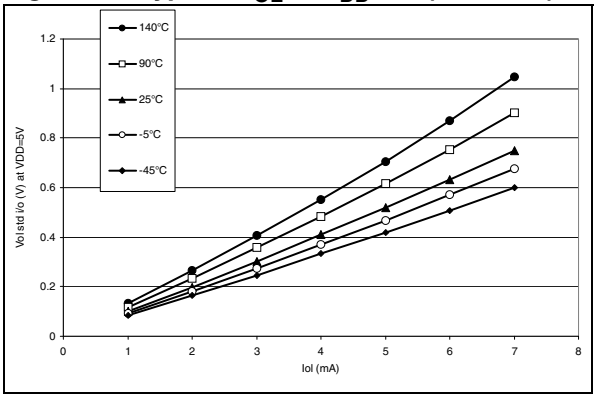


Figure 84. Typical V_{OL} at V_{DD}=2.7V (Port C)

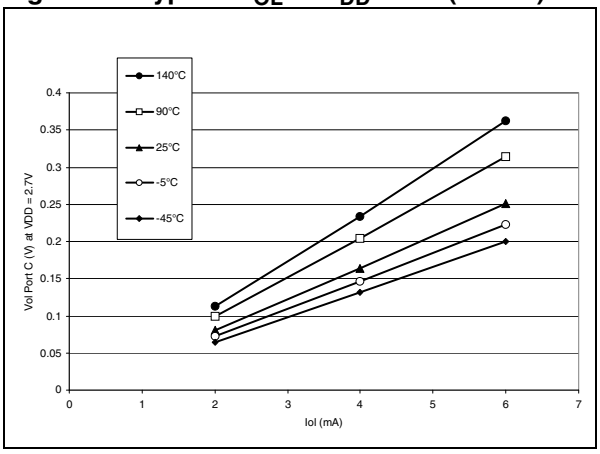


Figure 85. Typical V_{OL} at V_{DD}=3.3V (Port C)

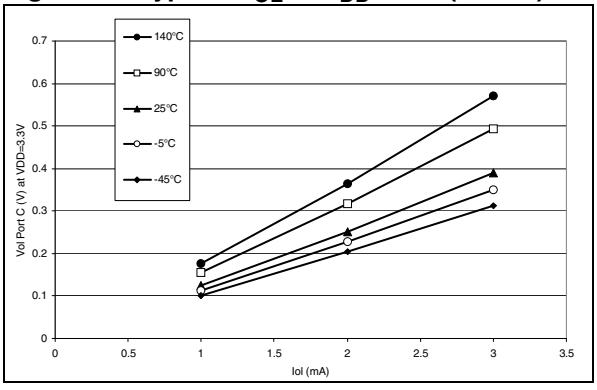
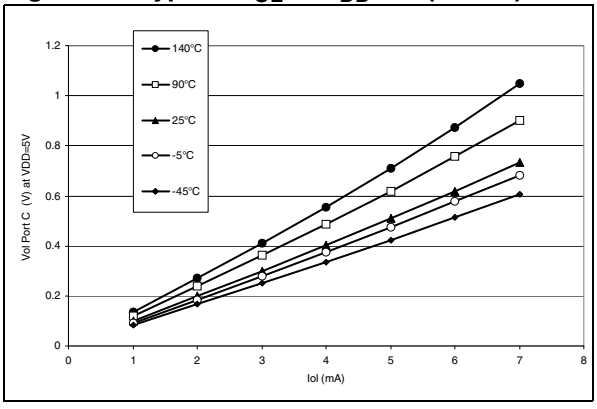


Figure 86. Typical V_{OL} at V_{DD}=5V (Port C)

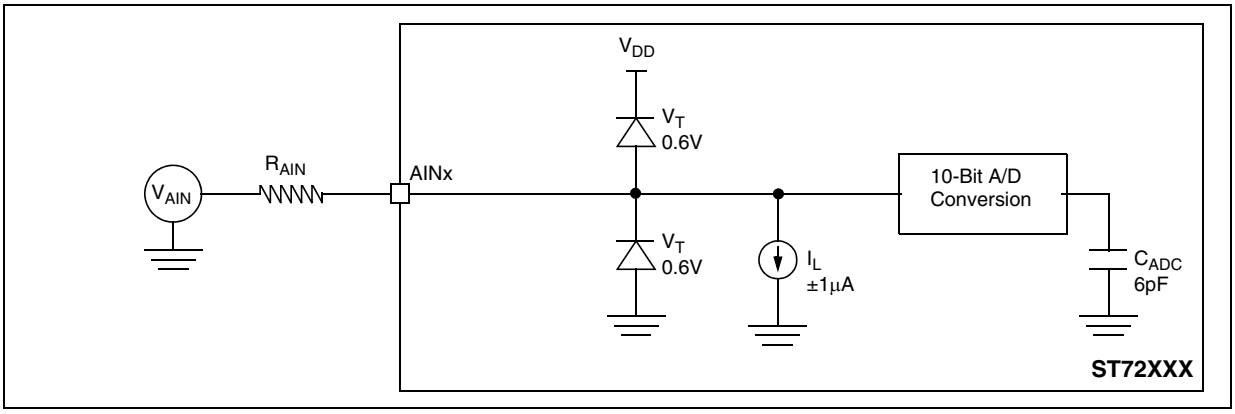


13.11 10-BIT ADC CHARACTERISTICS

Subject to general operating condition for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{ADC}	ADC clock frequency				4	MHz
V_{AIN}	Conversion voltage range [2]		V_{SSA}		V_{DDA}	V
R_{AIN}	External input resistor				10 [3]	kΩ
C_{ADC}	Internal sample and hold capacitor			6		pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU}=8MHz, f_{ADC}=4MHz	0 [4]			µs
t_{ADC}	Conversion time (Sample+Hold)		3.5			
	- Sample capacitor loading time - Hold conversion time		4 10			$1/f_{ADC}$
I_{ADC}	Analog Part			1		mA
	Digital Part			0.2		

Figure 110. Typical Application with ADC



Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5V. They are given only as design guidelines and are not tested.

2. When V_{DDA} and V_{SSA} pins are not available on the pinout, the ADC refers to V_{DD} and V_{SS}.

3. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.

4. The stabilization time of the AD converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.

Related application notes:

Understanding and minimizing ADC conversion errors (AN1636)

Software techniques for compensating ST7 ADC errors (AN1711)

ADC CHARACTERISTICS (Cont'd)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(AMP)}$	Amplifier operating voltage		3.6		5.5	V
V_{IN}	Amplifier input voltage[4]	V_{DD}=3.6V	0		350	mV
		V_{DD}=5V	0		500	
V_{OFFSET} [1]	Amplifier output offset voltage[5]	V_{DD}=5V		200		mV
V_{STEP} [1]	Step size for monotonicity[3]	V_{DD}=3.6V	3.5			mV
		V_{DD}=5V	4.89			
Linearity [1]	Output Voltage Response		Linear			
Gain factor [1]	Amplified Analog input Gain[2]			8		
Vmax [1]	Output Linearity Max Voltage	V_{INmax} = 430mV, V_{DD}=5V		3.65		V
Vmin [1]	Output Linearity Min Voltage			200		mV

Notes:

1. Data based on characterization results over the whole temperature range, not tested in production.

2. For precise conversion results it is recommended to calibrate the amplifier at the following two points:

– offset at V_{INmin} = 0V

– gain at full scale (for example V_{IN}=430mV)

3. Monotonicity guaranteed if V_{IN} increases or decreases in steps of min. 5mV.

4. Please refer to the Application Note AN1830 for details of TE% vs Vin.

5. Refer to the offset variation in temperature below

Amplifier output offset variation

The offset is quite sensitive to temperature variations. In order to ensure a good reliability in measurements, the offset must be recalibrated periodically i.e. during power on or whenever the device is reset depending on the customer application and during temperature variation. The table below gives the typical offset variation over temperature:

Typical Offset Variation (LSB)				UNIT
-45	-20	+25	+90	°C
-12	-7	-	+13	LSB

14.2 SOLDERING INFORMATION

In accordance with the RoHS European directive, all STMicroelectronics packages have been converted to lead-free technology, named ECOPACK™.

- ECOPACK™ packages are qualified according to the JEDEC STD-020C compliant soldering profile.
- Detailed information on the STMicroelectronics ECOPACK™ transition program is available on www.st.com/stonline/leadfree/, with specific technical Application notes covering the main technical aspects related to lead-free conversion (AN2033, AN2034, AN2035, AN2036).

Backward and forward compatibility:

The main difference between Pb and Pb-free soldering process is the temperature range.

– ECOPACK™ TQFP, SDIP, SO and QFN20 packages are fully compatible with Lead (Pb) containing soldering process (see application note AN2034)

– TQFP, SDIP and SO Pb-packages are compatible with Lead-free soldering process, nevertheless it's the customer's duty to verify that the Pb-packages maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering temperature.

Table 25. Soldering Compatibility (wave and reflow soldering process)

Package	Plating material devices	Pb solder paste	Pb-free solder paste
SDIP & PDIP	Sn (pure Tin)	Yes	Yes *
QFN	Sn (pure Tin)	Yes	Yes *
TQFP and SO	NiPdAu (Nickel-palladium-Gold)	Yes	Yes *

* Assemblers must verify that the Pb-package maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering process.

Date	Revision	Main changes
27-Nov-06	4	Added QFN20 pinout with new mechanical data (Figure 3 on page 5 and Figure 117 on page 145) Added ST7FLI19BY1M3TR sales type in Table 1, “Supported Flash part numbers,” Modifed “DEVELOPMENT TOOLS” on page 153
23-April-07	5	Added note 1 to Table 1 on page 7 Modified note 1 in section 7.1 on page 23 Added caution to section 7.5.1 on page 28 Modified section 11.2.3.6 on page 67 Modified title of Figure 48 on page 68 and added note 1 Modified Figure 49 on page 69 Modified section 11.5.3.4 on page 97 and added section 11.5.3.5 on page 97 Modified EOC bit description in section 11.5.6 on page 98 Modified V_{FFTB} parameter in section 13.7.1 on page 127 Modified Table 28 on page 153
17-June-08	6	Modified first page Added note 2 in Table 1, “Device Pin Description,” on page 7 Modified WDGRF bit description in section 7.6.4 on page 35 Modified note 1 in section 11.2.3.6 on page 67 Added section 13.3.6 on page 120 Modified CLKSEL option bits description in section 15.1 on page 149 Modified section 15.2 on page 151 and option list