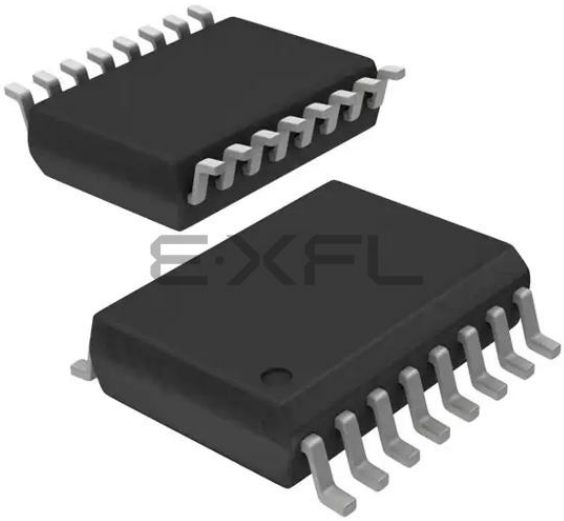

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7fli19by1m3tr

2 PIN DESCRIPTION

Figure 2. 20-Pin SO and DIP Package Pinout

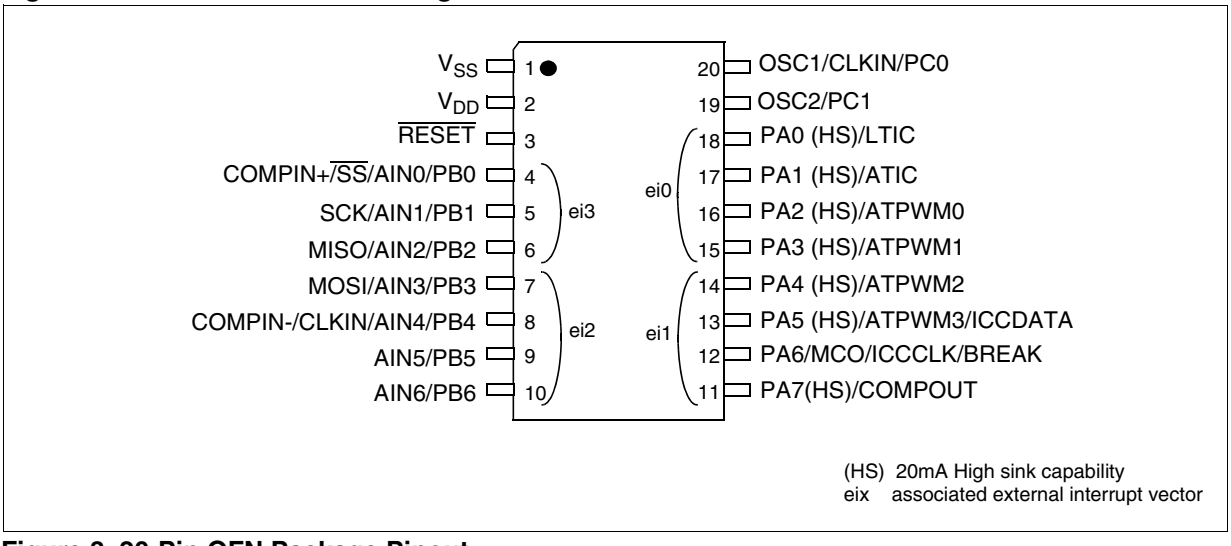
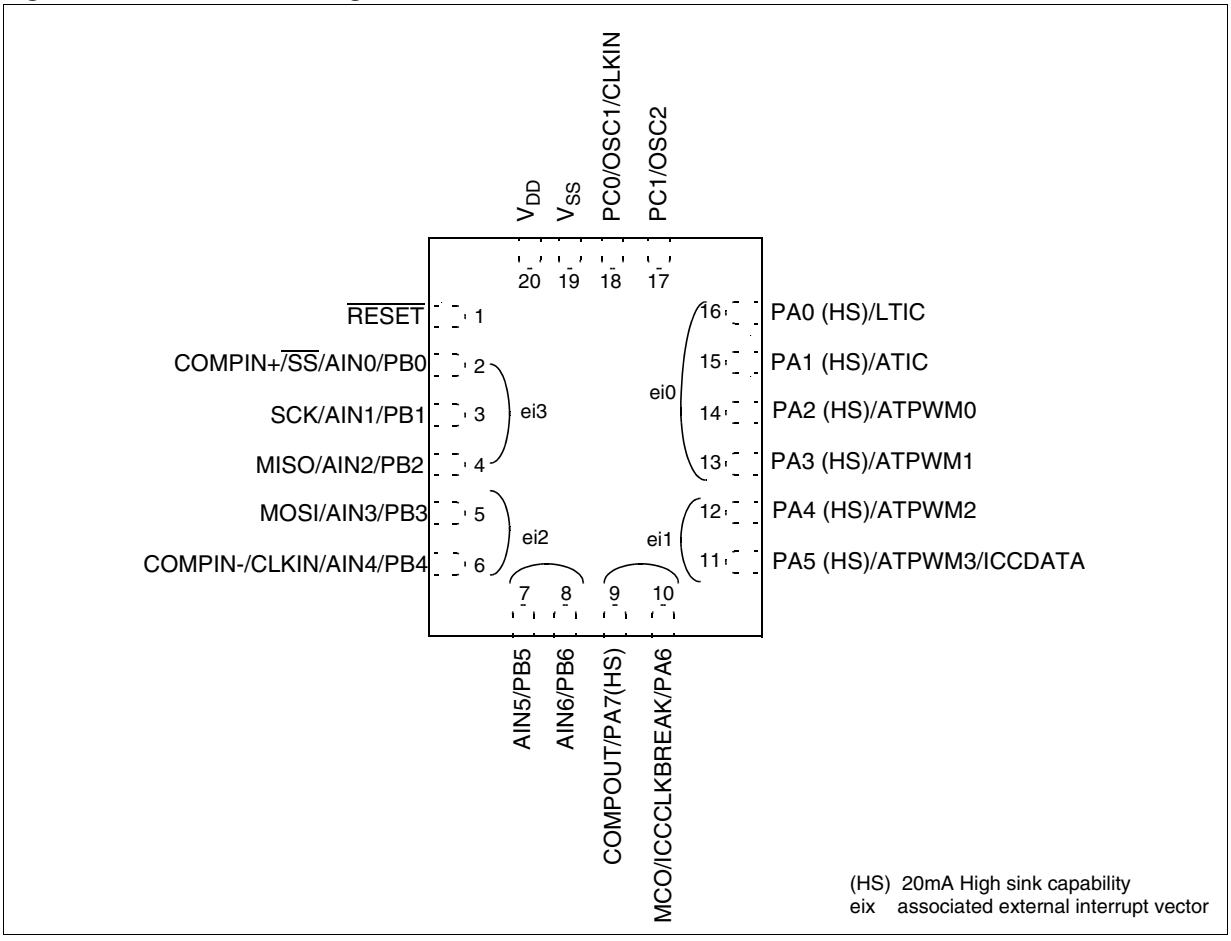


Figure 3. 20-Pin QFN Package Pinout



Pin No.			Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
							Input				Output			
SO20/DPI20	QFN20	SO16/DIP16			Input	Output	float	wpu	int	ana	OD	PP		
12	10	10	PA6 /MCO/ ICCCLK/BREAK	I/O	C_T		X	**ei1**			X	X	**Port A6**	Main Clock Output or In Circuit Communication Clock or External BREAK **Caution:** During normal operation this pin must be pulled- up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up
13	11	11	PA5 /ICCDATA/ ATPWM3	I/O	C_T	HS	**X**	ei1			X	X	**Port A5**	In Circuit Communication Data or Auto-Reload Timer PWM3
14	12	12	PA4/ATPWM2	I/O	C_T	HS	**X**				X	X	**Port A4**	Auto-Reload Timer PWM2
15	13	-	PA3/ATPWM1	I/O	C_T	HS	**X**	ei0			X	X	**Port A3**	Auto-Reload Timer PWM1
16	14	13	PA2/ATPWM0	I/O	C_T	HS	**X**				X	X	**Port A2**	Auto-Reload Timer PWM0
17	15	-	PA1/ATIC	I/O	C_T	HS	**X**				X	X	**Port A1**	Auto-Reload Timer Input Capture
18	16	14	PA0/LTIC	I/O	C_T	HS	**X**				X	X	**Port A0**	Lite Timer Input Capture
19	17	15	OSC2/PC1	I/O			**X**					X	**Port C1**[3]	Resonator oscillator inverter output
20	18	16	OSC1/CLKIN/PC0	I/O			**X**					X	**Port C0**[3]	Resonator oscillator inverter input or External clock input

Notes:

1. It is mandatory to connect all available V_{DD} and V_{DDA} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.

2. When the pin is configured as analog input, positive and negative current injections are not allowed.

3. PCOR not implemented but p-transistor always active in output mode (refer to Figure 32 on page 50).

7.3 REGISTER DESCRIPTION

MAIN CLOCK CONTROL/STATUS REGISTER (MCCSR)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	MCO	SMS

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **MCO** *Main Clock Out enable*
This bit is read/write by software and cleared by hardware after a reset. This bit allows to enable the MCO output clock.
0: MCO clock disabled, I/O port free for general purpose I/O.
1: MCO clock enabled.

Bit 0 = **SMS** *Slow Mode select*
This bit is read/write by software and cleared by hardware after a reset. This bit selects the input clock f_{OSC} or $f_{OSC}/32$.
0: Normal mode ($f_{CPU} = f_{OSC}$
1: Slow mode ($f_{CPU} = f_{OSC}/32$)

RC CONTROL REGISTER (RCCR)
Read / Write
Reset Value: 1111 1111 (FFh)

7							0
CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2

Bits 7:0 = **CR[9:2]** *RC Oscillator Frequency Adjustment Bits*
These bits must be written immediately after reset to adjust the RC oscillator frequency and to obtain an accuracy of 1%. The application can store the correct value for each voltage range in EEPROM and write it to this register at start-up.
00h = maximum available frequency
FFh = lowest available frequency
These bits are used with the CR[1:0] bits in the SICSR register. Refer to section 7.6.4 on page 35.

Note: To tune the oscillator, write a series of different values in the register until the correct frequency is reached. The fastest method is to use a dichotomy starting with 80h.

– select rising edge
– reset the interrupt mask with the RIM instruction (in cases where a pin level change could occur)

10.2.2 Output Modes

Setting the DDRx bit selects output mode. Writing to the DR bits applies a digital value to the I/O through the latch. Reading the DR bits returns the previously stored value.

If an OR bit is available, different output modes can be selected by software: push-pull or open-drain. Refer to I/O Port Implementation section for configuration.

DR Value and Output Pin Status

DR	Push-Pull	Open-Drain
0	V_{OL}	V_{OL}
1	V_{OH}	Floating

10.2.3 Alternate Functions

Many ST7s I/Os have one or more alternate functions. These may include output signals from, or input signals to, on-chip peripherals. The Device Pin Description table describes which peripheral signals can be input/output to which ports.

A signal coming from an on-chip peripheral can be output on an I/O. To do this, enable the on-chip peripheral as an output (enable bit in the peripheral's control register). The peripheral configures the I/O as an output and takes priority over standard I/O programming. The I/O's state is readable by addressing the corresponding I/O data register.

Configuring an I/O as floating enables alternate function input. It is not recommended to configure an I/O as pull-up as this will increase current consumption. Before using an I/O as an alternate input, configure it without interrupt. Otherwise spurious interrupts can occur.

Configure an I/O as input floating for an on-chip peripheral signal which can be input and output.

Caution:
I/Os which can be configured as both an analog and digital alternate function need special attention. The user must control the peripherals so that the signals do not arrive at the same time on the same pin. If an external clock is used, only the clock alternate function should be employed on that I/O pin and not the other alternate function.

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.3.4 Output Compare Mode

To use this function, load a 12-bit value in the Preload DCRxH and DCRxL registers.

When the 12-bit upcounter CNTR1 reaches the value stored in the Active DCRxH and DCRxL registers, the CMPFx bit in the PWMxCSR register is set and an interrupt request is generated if the CMPIE bit is set.

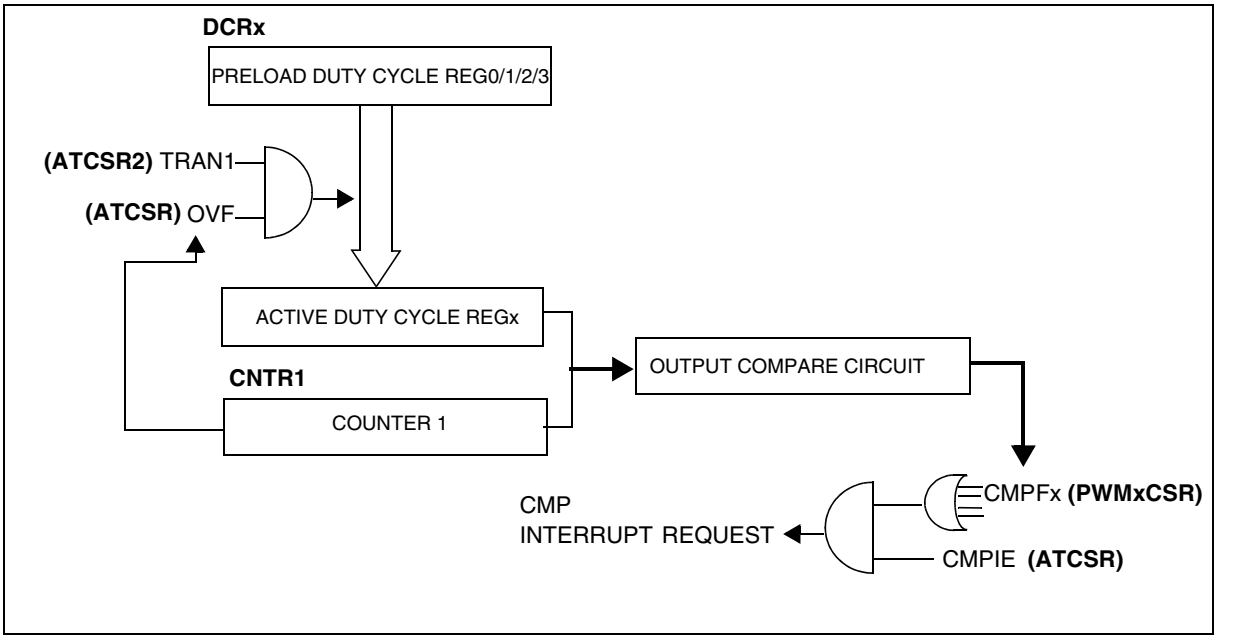
In single Timer mode the output compare function is performed only on CNTR1. The difference between both the modes is that, in Single Timer mode, CNTR1 can be compared with any of the four DCR registers, and in Dual Timer mode, CNTR1 is compared with DCR0 or DCR1 and CNTR2 is compared with DCR2 or DCR3.

Notes:

1. The output compare function is only available for DCRx values other than 0 (reset value).

2. Duty cycle registers are buffered internally. The CPU writes in Preload Duty Cycle Registers and these values are transferred in Active Duty Cycle Registers after an overflow event if the corresponding transfer bit (TRANx bit) is set. Output compare is done by comparing these active DCRx values with the counters.

Figure 42. Block Diagram of Output Compare Mode (single timer)



11.3 LITE TIMER 2 (LT2)

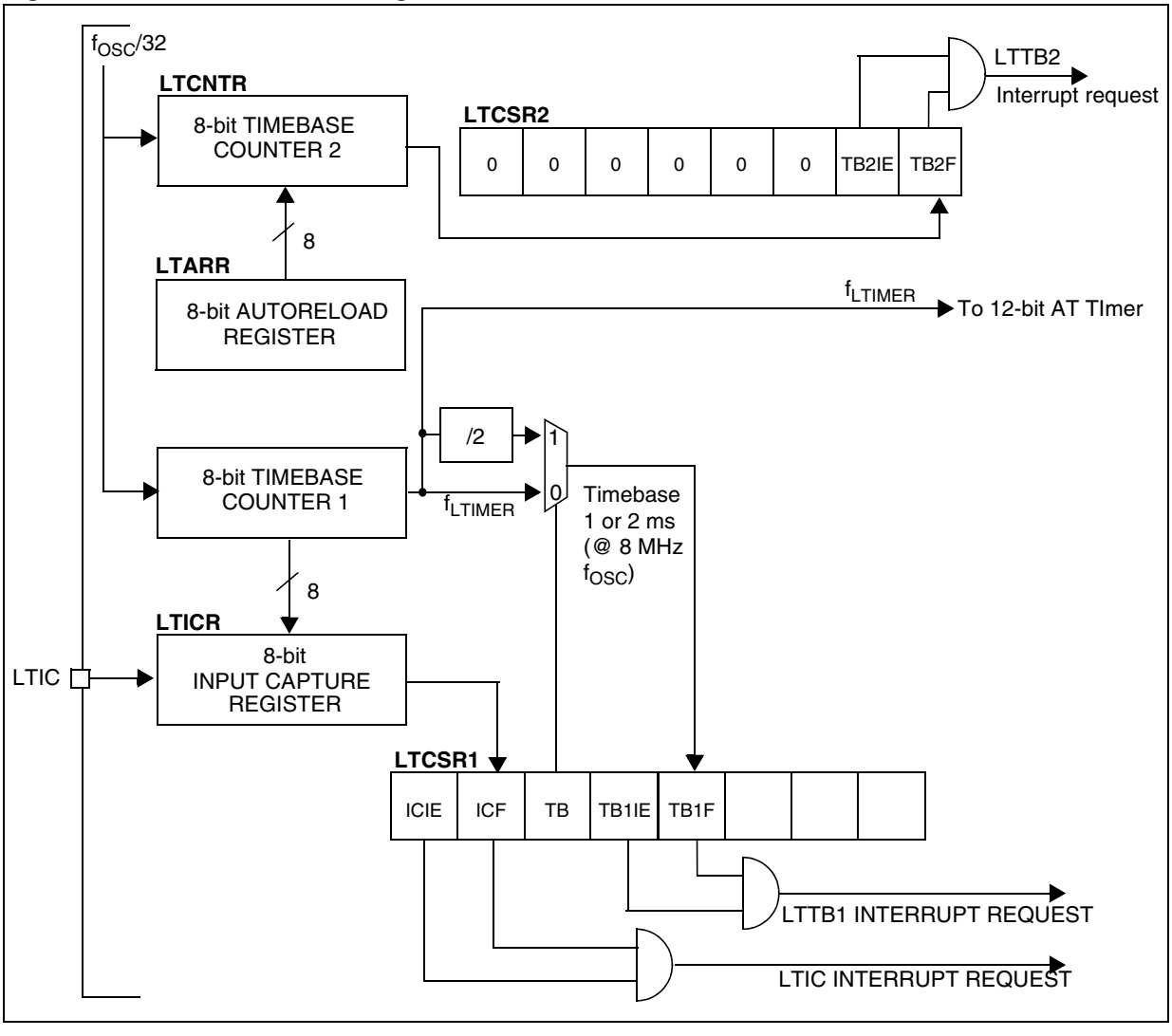
11.3.1 Introduction

The Lite Timer can be used for general-purpose timing functions. It is based on two free-running 8-bit upcounters and an 8-bit input capture register.

11.3.2 Main Features

- Realtime Clock
  - One 8-bit upcounter 1 ms or 2 ms timebase period (@ 8 MHz f_{OSC})
  - One 8-bit upcounter with autoreload and programmable timebase period from 4µs to 1.024ms in 4µs increments (@ 8 MHz f_{OSC})
  - 2 Maskable timebase interrupts
- Input Capture
  - 8-bit input capture register (LTICR)
  - Maskable interrupt with wake-up from Halt mode capability

Figure 51. Lite Timer 2 Block Diagram



SERIAL PERIPHERAL INTERFACE (cont'd)

11.4.3.1 Functional Description

A basic example of interconnections between a single master and a single slave is illustrated in Figure 2.

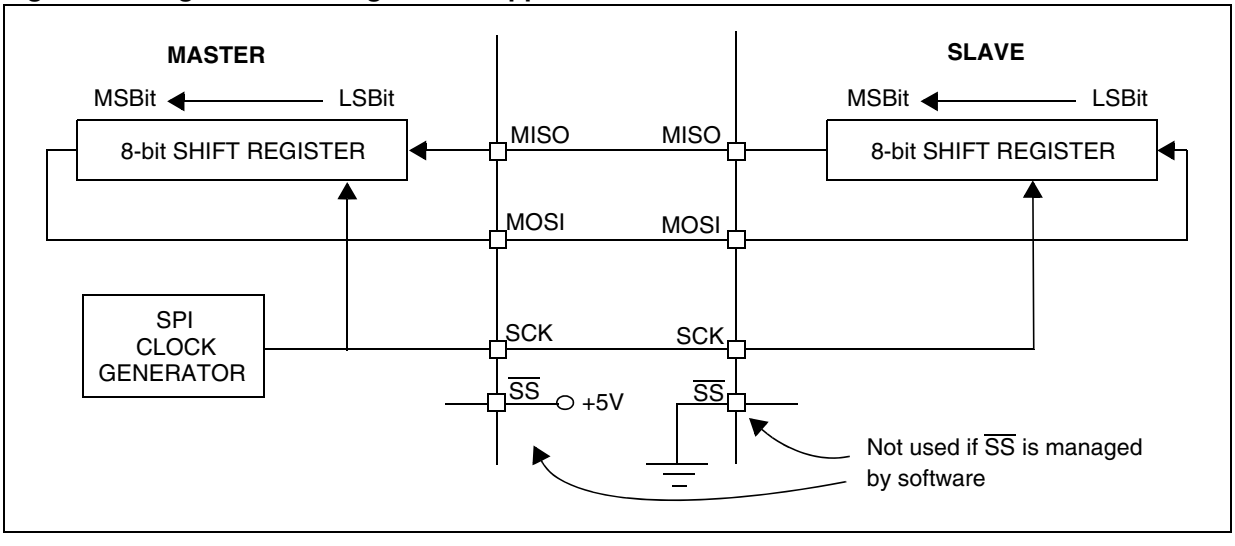
The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see Figure 5 on page 7) but master and slave must be programmed with the same timing mode.

Figure 54. Single Master/ Single Slave Application



SERIAL PERIPHERAL INTERFACE (cont'd)

11.4.5.4 Single Master and Multimaster Configurations

There are two types of SPI systems:

– Single Master System

– Multimaster System

Single Master System

A typical single master system may be configured using a device as the master and four devices as slaves (see Figure 7).

The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices.

The $\overline{SS}$ pins are pulled high during reset since the master device ports will be forced to be inputs at that time, thus disabling the slave devices.

Note: To prevent a bus conflict on the MISO line, the master allows only one active slave device during a transmission.

For more security, the slave device may respond to the master with the received data byte. Then the master will receive the previous byte back from the slave device if all MISO and MOSI pins are connected and the slave has not written to its SPIDR register.

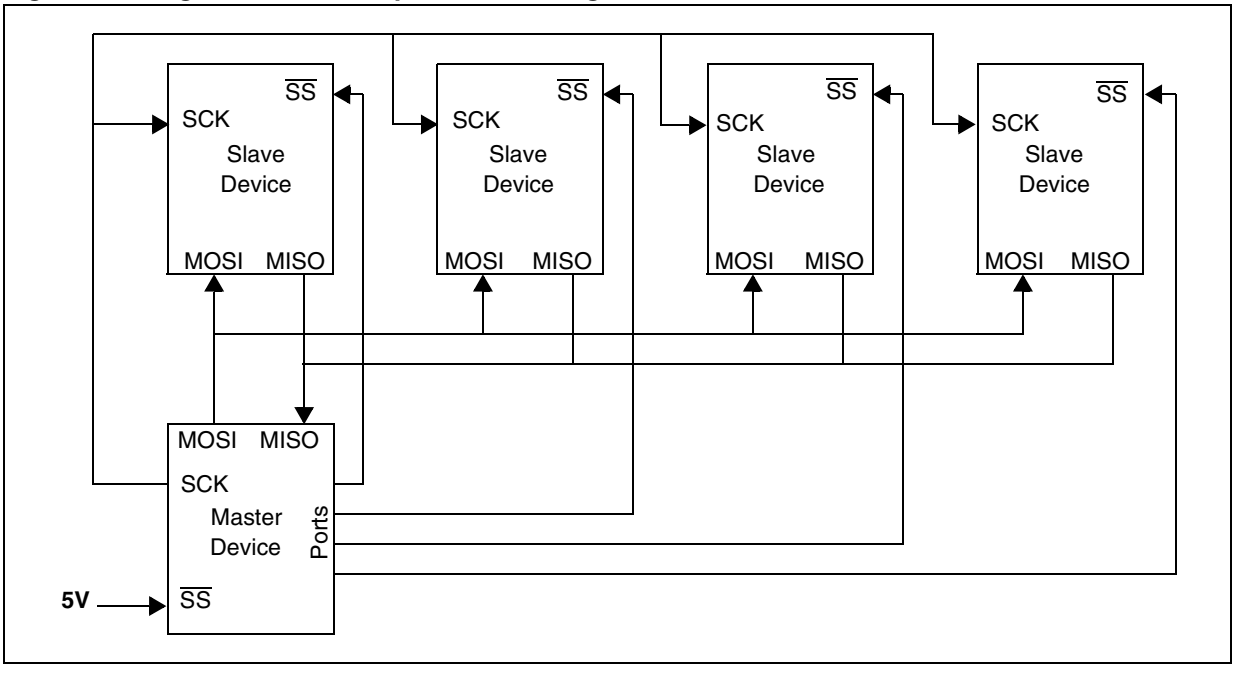
Other transmission security methods can use ports for handshake lines or data bytes with command fields.

Multimaster System

A multimaster system may also be configured by the user. Transfer of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system.

The multimaster system is principally handled by the MSTR bit in the SPICR register and the MODF bit in the SPICSR register.

Figure 59. Single Master / Multiple Slave Configuration



11.5 10-BIT A/D CONVERTER (ADC)

11.5.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 7 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 7 different sources.

The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

11.5.2 Main Features

- 10-bit conversion
- Up to 7 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in Figure 60.

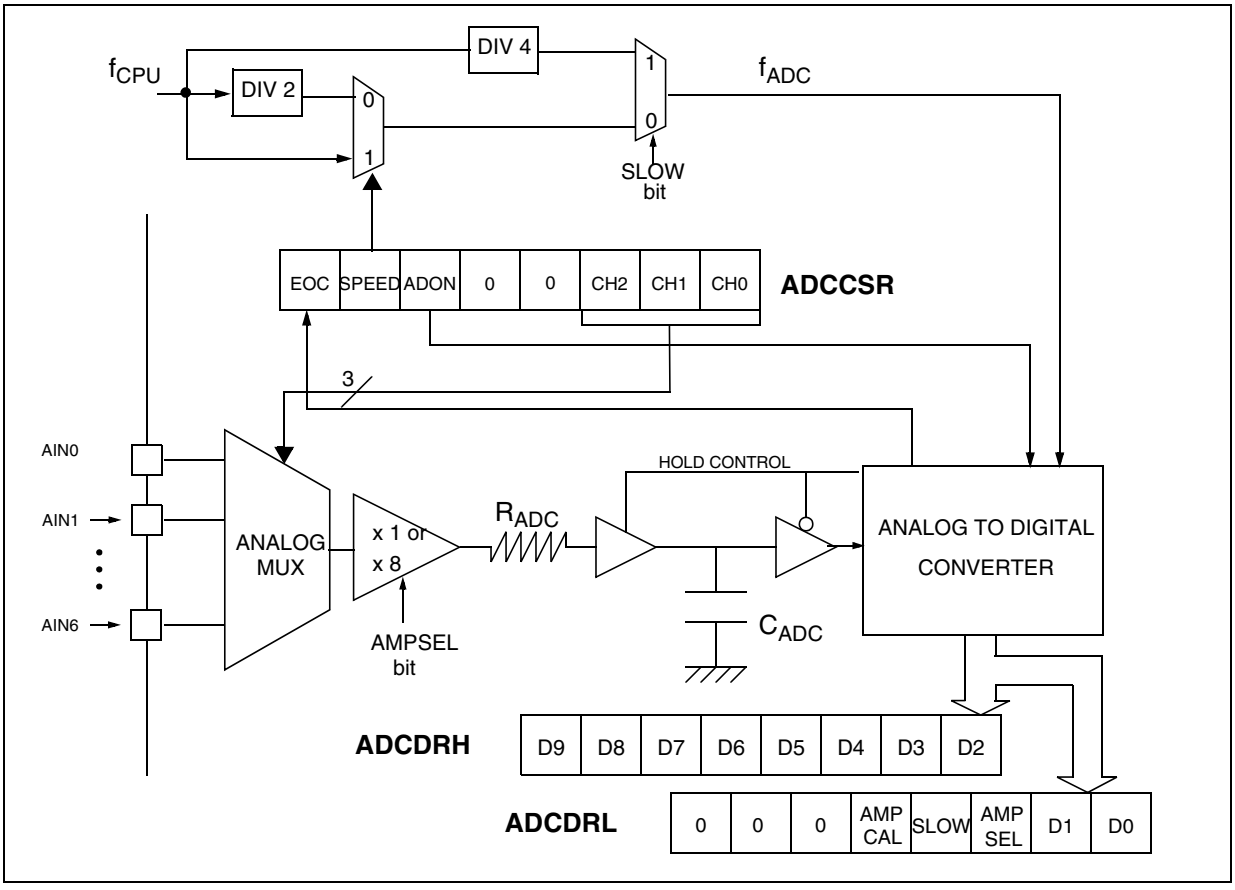
11.5.3 Functional Description

11.5.3.1 Analog Power Supply

V_{DDA} and V_{SSA} are the high and low level reference voltage pins. In some devices (refer to device pin out description) they are internally connected to the V_{DD} and V_{SS} pins.

Conversion accuracy may therefore be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines.

Figure 60. ADC Block Diagram



10-BIT A/D CONVERTER (ADC) (Cont'd)

11.5.3.2 Input Voltage Amplifier

The input voltage can be amplified by a factor of 8 by enabling the AMPSEL bit in the ADCDRL register.

When the amplifier is enabled, the input range is 0V to $V_{DD}/8$.

For example, if V_{DD} = 5V, then the ADC can convert voltages in the range 0V to 430mV with an ideal resolution of 0.6mV (equivalent to 13-bit resolution with reference to a V_{SS} to V_{DD} range).

For more details, refer to the Electrical characteristics section.

Note: The amplifier is switched on by the ADON bit in the ADCCSR register, so no additional start-up time is required when the amplifier is selected by the AMPSEL bit.

11.5.3.3 Digital A/D Conversion Result

The conversion is monotonic, meaning that the result never decreases if the analog input does not and never increases if the analog input does not.

If the input voltage (V_{AIN}) is greater than V_{DDA} (high-level voltage reference) then the conversion result is FFh in the ADCDRH register and 03h in the ADCDRL register (without overflow indication).

If the input voltage (V_{AIN}) is lower than V_{SSA} (low-level voltage reference) then the conversion result in the ADCDRH and ADCDRL registers is 00 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDRH and ADCDRL registers. The accuracy of the conversion is described in the Electrical Characteristics Section.

R_{AIN} is the maximum recommended impedance for an analog input signal. If the impedance is too high, this will result in a loss of accuracy due to leakage and sampling not being completed in the alloted time.

11.5.3.4 A/D Conversion

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to the «I/O ports» chapter. Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the ADCCSR register:

– Select the CH[2:0] bits to assign the analog channel to convert.

ADC Conversion mode

In the ADCCSR register:

Set the ADON bit to enable the A/D converter and to start the conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete:

– The EOC bit is set by hardware.
– The result is in the ADCDR registers.

A read to the ADCDRH or a write to any bit of the ADCCSR register resets the EOC bit.

To read the 10 bits, perform the following steps:

1. Poll the EOC bit
2. Read ADCDRL
3. Read ADCDRH. This clears EOC automatically.

To read only 8 bits, perform the following steps:

1. Poll EOC bit
2. Read ADCDRH. This clears EOC automatically.

11.5.3.5 Changing the conversion channel

The application can change channels during conversion.

When software modifies the CH[2:0] bits in the ADCCSR register, the current conversion is stopped, the EOC bit is cleared, and the A/D converter starts converting the newly selected channel.

11.5.4 Low Power Modes

Note: The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed and between single shot conversions.

Mode	Description
WAIT	No effect on A/D Converter
HALT	A/D Converter disabled. After wakeup from Halt mode, the A/D Converter requires a stabilization time t_{STAB} (see Electrical Characteristics) before accurate conversions can be performed.

11.5.5 Interrupts

None.

OPERATING CONDITIONS (Cont'd)

The RC oscillator and PLL characteristics are temperature-dependent and are grouped in four tables.

13.3.5.1 Devices with '"6" or "3"order code suffix (tested for T_A = -40 to +125°C) @ V_{DD} = 5V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	Internal RC oscillator frequency [1]	RCCR = FF (reset value), T_A=25°C,V_{DD}=5V		700		kHz
		RCCR = RCCR0[2],T_A=25°C,V_{DD}=5V	992	1000	1008	
ACC_{RC}	Accuracy of Internal RC oscillator with RCCR=RCCR0[2]	T_A=25°C,V_{DD}=5V	-0.8		+0.8	%
		T_A=25°C, V_{DD}=4.5 to 5.5V[3]	-1		+1	%
		T_A=25°C to +85°C,V_{DD}=5V	-3		+3	%
		T_A=25°C to +85°C,V_{DD}=4.5 to 5.5V[3]	-3.5		+3.5	%
		T_A=85°C to +125°C,V_{DD}=5V	-3.5		+5	%
		T_A=85°C to +125°C,V_{DD}=4.5 to 5.5V[3]	-3.5		+6	%
		T_A=-40 to +25°C, V_{DD}=5V[3]	-3		+7	%
$I_{DD(RC)}$	RC oscillator current consumption	T_A=25°C,V_{DD}=5V		600[3]		µA
$t_{su(RC)}$	RC oscillator setup time	T_A=25°C,V_{DD}=5V			10[2]	µs
f_{PLL}	x8 PLL input clock			1[3]		MHz
t_{LOCK}	PLL Lock time[5]			2		ms
t_{STAB}	PLL Stabilization time[5]			4		ms
ACC_{PLL}	x8 PLL Accuracy	f_{RC} = 1MHz@T_A=25°C,V_{DD}=4.5 to 5.5V		0.1[4]		%
		f_{RC} = 1MHz@T_A=-40 to +85°C,V_{DD}=5V		0.1[4]		%
$t_{w(JIT)}$	PLL jitter period [6]	f_{RC} = 1MHz		120		µs
JIT_{PLL}	PLL jitter ($\Delta f_{CPU}/f_{CPU}$)			1[7]		%
$I_{DD(PLL)}$	PLL current consumption	T_A=25°C		600[3]		µA

Notes:

1. If the RC oscillator clock is selected, to improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

2. See "INTERNAL RC OSCILLATOR ADJUSTMENT" on page 23

3. Data based on characterization results, not tested in production

4. Averaged over a 4ms period. After the LOCKED bit is set, a period of t_{STAB} is required to reach ACC_{PLL} accuracy.

5. After the LOCKED bit is set ACC_{PLL} is max. 10% until t_{STAB} has elapsed. See Figure 13 on page 24.

6. This period is the phase servo loop period. During this period, the frequency remains unchanged.

7. Guaranteed by design.

OPERATING CONDITIONS (Cont'd)

Figure 68. Typical accuracy with RCCR=RCCR1 vs V_{DD}= 3-3.6V and Temperature

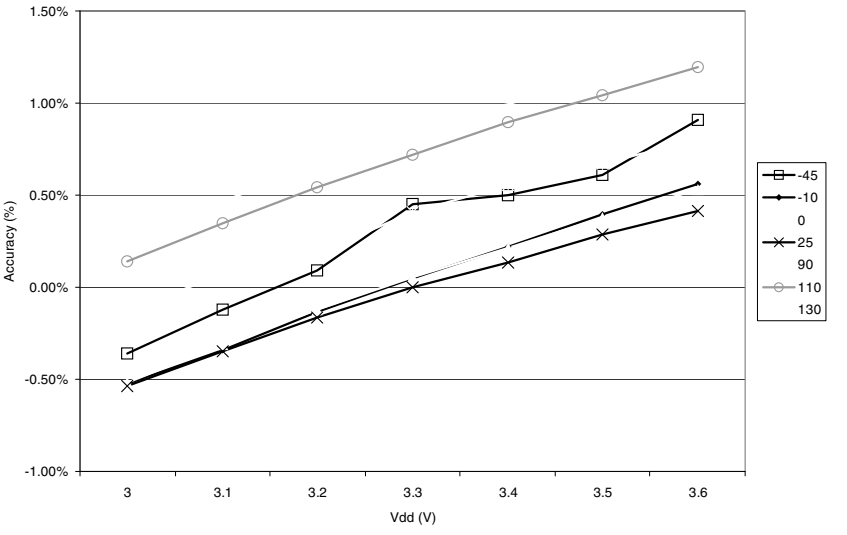
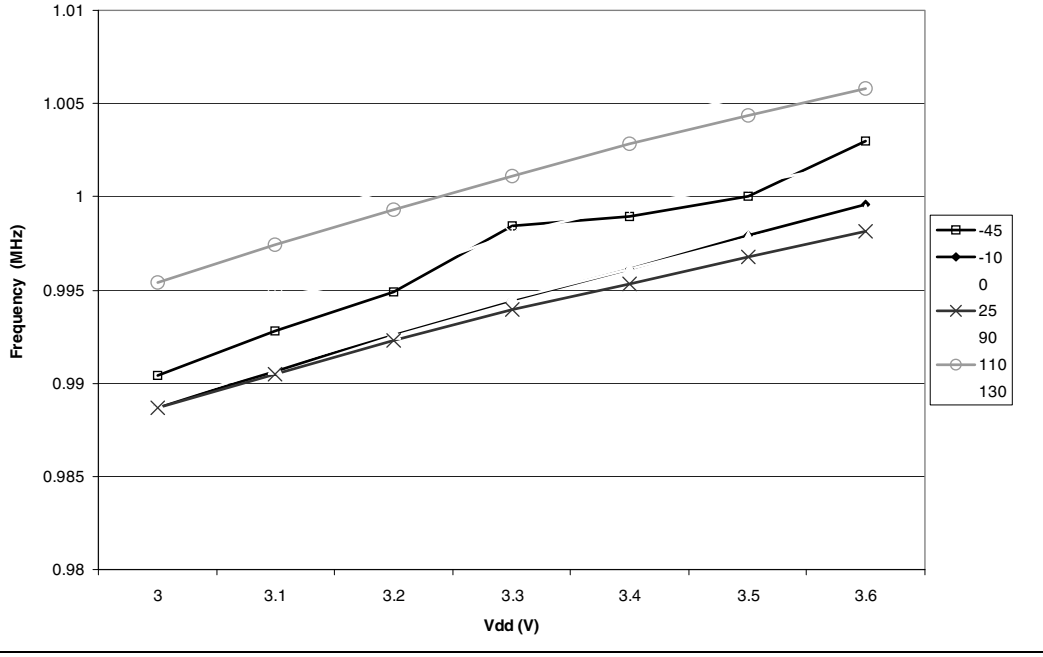
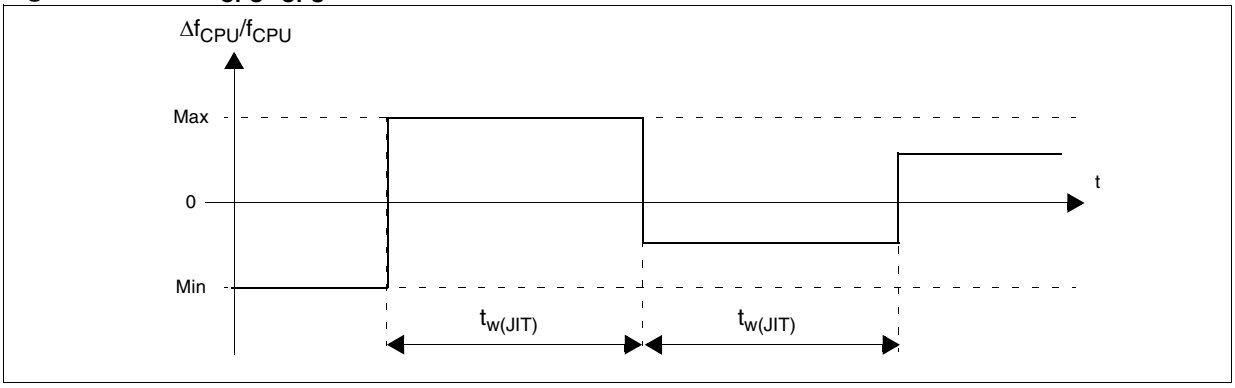


Figure 69. Typical RCCR1 vs V_{DD} and Temperature



OPERATING CONDITIONS (Cont'd)

Figure 70. PLL $\Delta f_{CPU}/f_{CPU}$ versus time



13.3.5.3 32MHz PLL

T_A = -40 to 125°C, unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Voltage [1]	4.5	5	5.5	V
f_{PLL32}	Frequency [1]		32		MHz
f_{INPUT}	Input Frequency	7	8	9	MHz

Note:
1. 32 MHz is guaranteed within this voltage range.

CLOCK AND TIMING CHARACTERISTICS (Cont'd)

13.5.4 Crystal and Ceramic Resonator Oscillators

The ST7 internal clock can be supplied with ten different Crystal/Ceramic resonator oscillators. All the information given in this paragraph are based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CrOSC}	Crystal Oscillator Frequency		2		16	MHz
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S)		See table below			pF

Supplier	f_{CrOSC} (MHz)	Typical Ceramic Resonators[1]		CL1 [3] [pF]	CL2 [3] [pF]	Rd [Ω]	Supply Voltage Range [V]	Temperature Range [°C]
		Type[2]	Reference					
Murata	1	SMD	CSBFB1M00J58-R0	220	*220*	2.2k	3.3V to 5.5V	-40 to 85
		LEAD	CSBLA1M00J58-B0	220	220	2.2k		
	2	SMD	CSTCC2M00G56Z-R0	(47)	(47)	0	3.0V to 5.5V	
	4	SMD	CSTCR4M00G53Z-R0	(15)	(15)	0		
		LEAD	CSTLS4M00G53Z-B0	(15)	(15)	0		
	8	SMD	CSTCE8M00G52Z-R0	(10)	(10)	0		
		LEAD	CSTLS8M00G53Z-B0	(15)	(15)	0		
	12	SMD	CSTCE12M0G52Z-R0	(10)	(10)	0	3.3V to 5.5V	
	16	SMD	CSTCE16M0V51Z-R0	(5)	(5)	0		
		LEAD	CSTLS16M0X51Z-B0	(5)	(5)	0		

Notes:

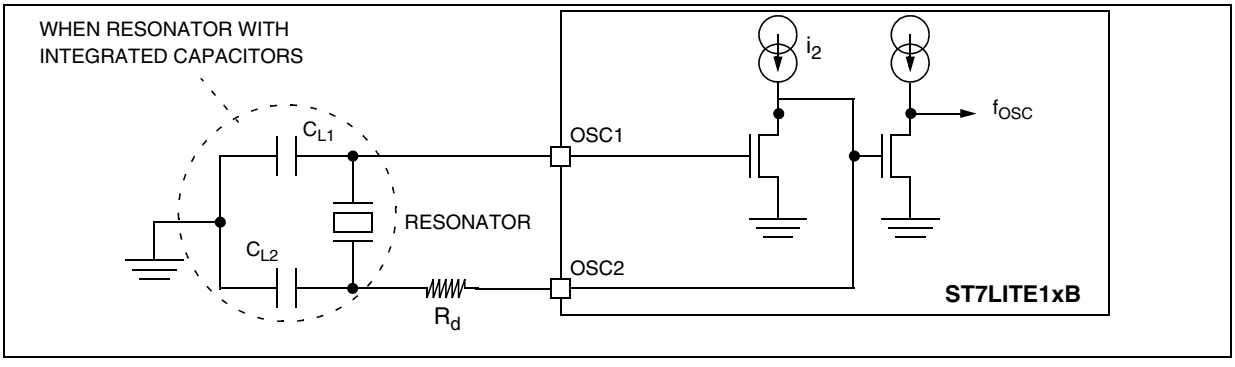
1. Resonator characteristics given by the ceramic resonator manufacturer. For more information on these resonators, please consult www.murata.com

2. SMD = [-R0: Plastic tape package (∅ =180mm)]

LEAD = [-B0: Bulk]

3. () means load capacitor built in resonator

Figure 79. Typical Application with a Crystal or Ceramic Resonator



13.7 EMC CHARACTERISTICS

Susceptibility tests are performed on a sample basis during product characterization.

13.7.1 Functional EMS (Electro Magnetic Susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electro magnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electro-Static Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

13.7.1.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations:

The software flowchart must include the management of runaway conditions such as:

– Corrupted program counter

– Unexpected reset

– Critical Data corruption (control registers...)

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behaviour is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-2	2B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}=5V, T_A=+25°C, f_{OSC}=8MHz conforms to IEC 1000-4-4	3B

13.7.2 Electro Magnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}/f_{CPU}]		Unit
				8/4MHz	16/8MHz	
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, SO20 package, conforming to SAE J 1752/3	0.1MHz to 30MHz	15	21	dBµV
			30MHz to 130MHz	22	29	
			130MHz to 1GHz	17	22	
			SAE EMI Level	3.5	3.5	-

Note:

1. Data based on characterization results, not tested in production.

13.8 I/O PORT PIN CHARACTERISTICS

13.8.1 General Characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage			V_{SS} - 0.3		0.3xV_{DD}	V
V_{IH}	Input high level voltage			0.7xV_{DD}		V_{DD} + 0.3	
V_{hys}	Schmitt trigger voltage hysteresis [1]				400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$				±1	µA
I_S	Static current consumption induced by each floating input pin [2]	Floating input mode			400		
R_{PU}	Weak pull-up equivalent resistor [3]	$V_{IN}=V_{SS}$	V_{DD}=5V	50	120	250	kΩ
			V_{DD}=3V		160		
C_{IO}	I/O pin capacitance				5		pF
$t_{f(IO)out}$	Output high to low level fall time [1]	C_L=50pF Between 10% and 90%			25		ns
$t_{r(IO)out}$	Output low to high level rise time [1]				25		
$t_{w(IT)in}$	External interrupt pulse time [4]			1			t_{CPU}

Notes:

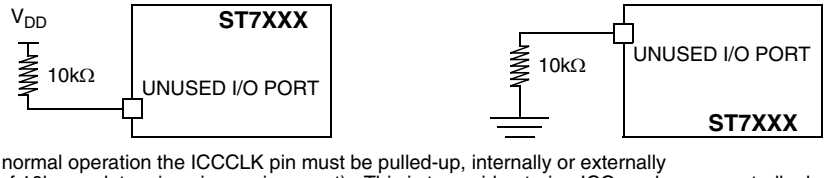
1. Data based on validation/design results.

2. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see Figure 80). Static peak current value taken at a fixed V_{IN} value, based on design simulation and technology characteristics, not tested in production. This value depends on V_{DD} and temperature values.

3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.

4. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 80. Two typical Applications with unused I/O Pin



Caution: During normal operation the ICCCLK pin must be pulled-up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset.
Note: I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

13.12 ANALOG COMPARATOR CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{DDA}	Supply range		4.5		5.5	V
V_{IN}	Comparator input voltage range		0		V_{DDA}	V
Temp	Temperature range		-40		125	°C
V_{offset}	Comparator offset error			20		mV
$I_{DD(CMP)}$	Analog Comparator Consumption			120		µA
	Analog Comparator Consumption during power-down			200		pA
t_{propag}	Comparator propagation delay			40		ns
$t_{startup}$	Startup filter duration			500[2]		ns
t_{stab}	Stabilisation time			500		ns

13.13 PROGRAMMABLE INTERNAL VOLTAGE REFERENCE CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{DDA}	Supply range		4	5	5.5	V
Temp	Temperature range		-40	27	125	°C
$I_{DD(VOLTREF)}$	Internal Voltage Reference Consumption			50		µA
	Internal Voltage Reference Consumption during power-down			200		pA
$t_{startup}$	Startup duration			1[2]		µs

13.14 CURRENT BIAS CHARACTERISTICS (for Comparator and Internal Voltage Reference)

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{DDA}	Supply range		4.5	5	5.5	V
Temp	Temperature range		-40	27	125	°C
IDD (Bias)	Bias Consumption in run mode			50		µA
	Bias Consumption during power-down			36		pA
$t_{startup}$	Startup time			1[2]		µs

Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5V. They are given only as design guidelines and are not tested.

2. Since startup time for internal voltage reference and bias is 1 µs, comparator correct output should not be expected before 1 µs during startup.

14.2 SOLDERING INFORMATION

In accordance with the RoHS European directive, all STMicroelectronics packages have been converted to lead-free technology, named ECOPACK™.

- ECOPACK™ packages are qualified according to the JEDEC STD-020C compliant soldering profile.
- Detailed information on the STMicroelectronics ECOPACK™ transition program is available on www.st.com/stonline/leadfree/, with specific technical Application notes covering the main technical aspects related to lead-free conversion (AN2033, AN2034, AN2035, AN2036).

Backward and forward compatibility:

The main difference between Pb and Pb-free soldering process is the temperature range.

– ECOPACK™ TQFP, SDIP, SO and QFN20 packages are fully compatible with Lead (Pb) containing soldering process (see application note AN2034)

– TQFP, SDIP and SO Pb-packages are compatible with Lead-free soldering process, nevertheless it's the customer's duty to verify that the Pb-packages maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering temperature.

Table 25. Soldering Compatibility (wave and reflow soldering process)

Package	Plating material devices	Pb solder paste	Pb-free solder paste
SDIP & PDIP	Sn (pure Tin)	Yes	Yes *
QFN	Sn (pure Tin)	Yes	Yes *
TQFP and SO	NiPdAu (Nickel-palladium-Gold)	Yes	Yes *

* Assemblers must verify that the Pb-package maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering process.

15.2 DEVICE ORDERING INFORMATION

Figure 118. Ordering information scheme

Example: ST7 F LIT1xB F 0 M 3 TR

Family

ST7 Microcontroller Family

Memory type

F: Flash
P: FASTROM

Version

10B, 15B or 19B

No. of pins

F = 20
Y = 16

Memory size

0 = 2K
1 = 4K

Package

B = DIP
M = SO
U = VFQFPN

Temperature range

6 = -40 °C to 85 °C
3 = -40 °C to 125 °C

Shipping Option

TR = Tape & Reel packing
Blank = Tube (DIP or SO) or Tray (VFQFPN)

For a list of available options (e.g. data EEPROM, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 29. ST7 Application Notes

IDENTIFICATION	DESCRIPTION
AN1947	ST7MC PMAC SINE WAVE MOTOR CONTROL SOFTWARE LIBRARY
GENERAL PURPOSE	
AN1476	LOW COST POWER SUPPLY FOR HOME APPLIANCES
AN1526	ST7FLITE0 QUICK REFERENCE NOTE
AN1709	EMC DESIGN FOR ST MICROCONTROLLERS
AN1752	ST72324 QUICK REFERENCE NOTE
PRODUCT EVALUATION	
AN 910	PERFORMANCE BENCHMARKING
AN 990	ST7 BENEFITS VERSUS INDUSTRY STANDARD
AN1077	OVERVIEW OF ENHANCED CAN CONTROLLERS FOR ST7 AND ST9 MCUS
AN1086	U435 CAN-DO SOLUTIONS FOR CAR MULTIPLEXING
AN1103	IMPROVED B-EMF DETECTION FOR LOW SPEED, LOW VOLTAGE WITH ST72141
AN1150	BENCHMARK ST72 VS PC16
AN1151	PERFORMANCE COMPARISON BETWEEN ST72254 & PC16F876
AN1278	LIN (LOCAL INTERCONNECT NETWORK) SOLUTIONS
PRODUCT MIGRATION	
AN1131	MIGRATING APPLICATIONS FROM ST72511/311/214/124 TO ST72521/321/324
AN1322	MIGRATING AN APPLICATION FROM ST7263 REV.B TO ST7263B
AN1365	GUIDELINES FOR MIGRATING ST72C254 APPLICATIONS TO ST72F264
AN1604	HOW TO USE ST7MDT1-TRAIN WITH ST72F264
AN2200	GUIDELINES FOR MIGRATING ST7LITE1X APPLICATIONS TO ST7FLITE1XB
PRODUCT OPTIMIZATION	
AN 982	USING ST7 WITH CERAMIC RESONATOR
AN1014	HOW TO MINIMIZE THE ST7 POWER CONSUMPTION
AN1015	SOFTWARE TECHNIQUES FOR IMPROVING MICROCONTROLLER EMC PERFORMANCE
AN1040	MONITORING THE VBUS SIGNAL FOR USB SELF-POWERED DEVICES
AN1070	ST7 CHECKSUM SELF-CHECKING CAPABILITY
AN1181	ELECTROSTATIC DISCHARGE SENSITIVE MEASUREMENT
AN1324	CALIBRATING THE RC OSCILLATOR OF THE ST7FLITE0 MCU USING THE MAINS
AN1502	EMULATED DATA EEPROM WITH ST7 HDFLASH MEMORY
AN1529	EXTENDING THE CURRENT & VOLTAGE CAPABILITY ON THE ST7265 VDDF SUPPLY
AN1530	ACCURATE TIMEBASE FOR LOW-COST ST7 APPLICATIONS WITH INTERNAL RC OSCILLATOR
AN1605	USING AN ACTIVE RC TO WAKEUP THE ST7LITE0 FROM POWER SAVING MODE
AN1636	UNDERSTANDING AND MINIMIZING ADC CONVERSION ERRORS
AN1828	PIR (PASSIVE INFRARED) DETECTOR USING THE ST7FLITE05/09/SUPERLITE
AN1946	SENSORLESS BLDC MOTOR CONTROL AND BEMF SAMPLING METHODS WITH ST7MC
AN1953	PFC FOR ST7MC STARTER KIT
AN1971	ST7LITE0 MICROCONTROLLED BALLAST
PROGRAMMING AND TOOLS	
AN 978	ST7 VISUAL DEVELOP SOFTWARE KEY DEBUGGING FEATURES
AN 983	KEY FEATURES OF THE COSMIC ST7 C-COMPILER PACKAGE
AN 985	EXECUTING CODE IN ST7 RAM
AN 986	USING THE INDIRECT ADDRESSING MODE WITH ST7
AN 987	ST7 SERIAL TEST CONTROLLER PROGRAMMING
AN 988	STARTING WITH ST7 ASSEMBLY TOOL CHAIN
AN 989	GETTING STARTED WITH THE ST7 HIWARE C TOOLCHAIN