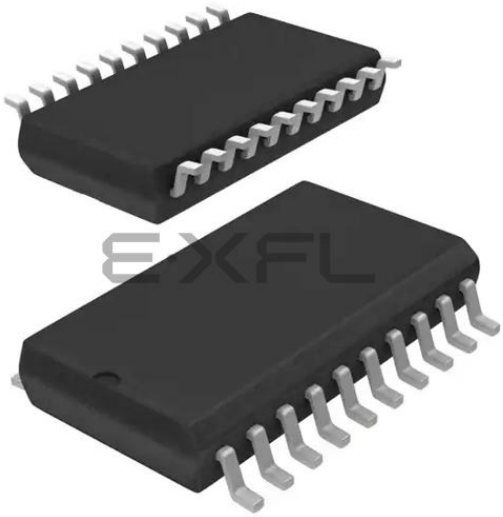

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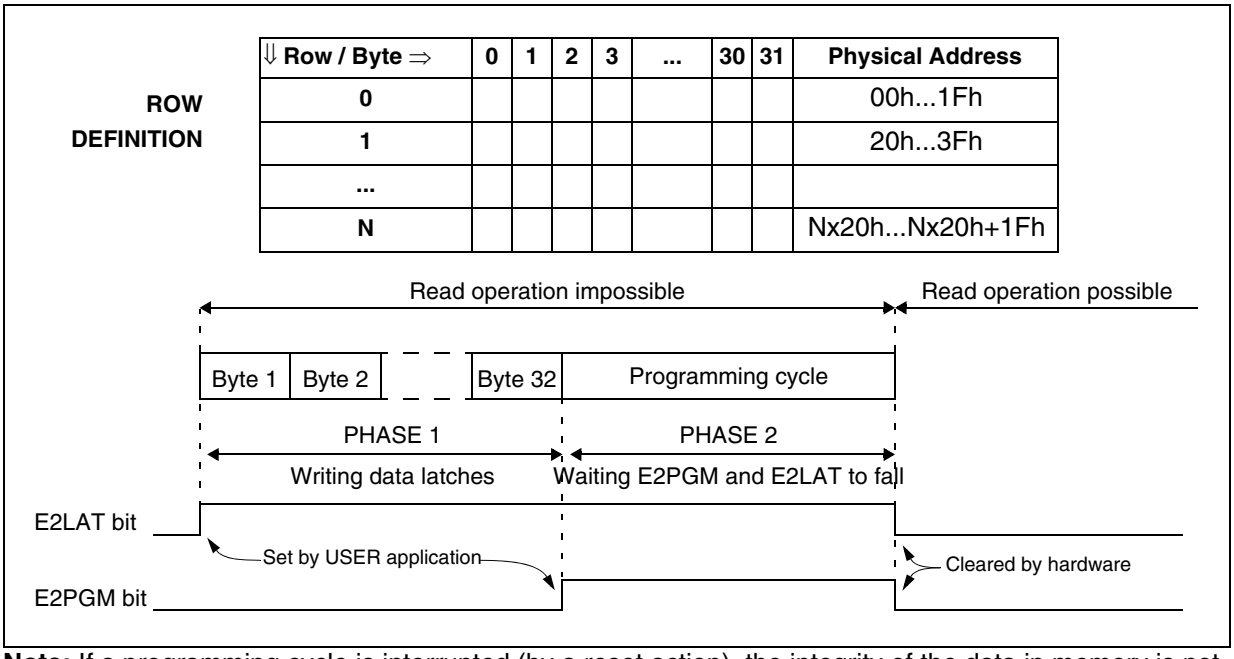
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flit15bm6tr

DATA EEPROM (Cont'd)

Figure 9. Data E^2PROM Write Operation



Note: If a programming cycle is interrupted (by a reset action), the integrity of the data in memory is not guaranteed.

CPU REGISTERS (cont'd)

CONDITION CODE REGISTER (CC)

Read/Write

Reset Value: 111x1xxx

7							0
1	1	1	H	I	N	Z	C

The 8-bit Condition Code register contains the interrupt mask and four flags representative of the result of the instruction just executed. This register can also be handled by the PUSH and POP instructions.

These bits can be individually tested and/or controlled by specific instructions.

Bit 4 = **H** Half carry

This bit is set by hardware when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. It is reset by hardware during the same instructions.
0: No half carry has occurred.
1: A half carry has occurred.

This bit is tested using the JRH or JRNH instruction. The H bit is useful in BCD arithmetic subroutines.

Bit 3 = **I** Interrupt mask

This bit is set by hardware when entering in interrupt or by software to disable all interrupts except the TRAP software interrupt. This bit is cleared by software.
0: Interrupts are enabled.
1: Interrupts are disabled.

This bit is controlled by the RIM, SIM and IRET instructions and is tested by the JRM and JRNM instructions.

Note: Interrupts requested while I is set are latched and can be processed when I is cleared. By default an interrupt routine is not interruptible because the I bit is set by hardware at the start of the routine and reset by the IRET instruction at the end of the routine. If the I bit is cleared by software in the interrupt routine, pending interrupts are serviced regardless of the priority level of the current interrupt routine.

Bit 2 = **N** Negative

This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It is a copy of the 7^{th} bit of the result.
0: The result of the last operation is positive or null.
1: The result of the last operation is negative (that is, the most significant bit is a logic 1).

This bit is accessed by the JRMI and JRPL instructions.

Bit 1 = **Z** Zero

This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.
0: The result of the last operation is different from zero.
1: The result of the last operation is zero.

This bit is accessed by the JREQ and JRNE test instructions.

Bit 0 = **C** Carry/borrow

This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.
0: No overflow or underflow has occurred.
1: An overflow or underflow has occurred.

This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the "bit test and branch", shift and rotate instructions.

8 INTERRUPTS

The ST7 core may be interrupted by one of two different methods: Maskable hardware interrupts as listed in the “interrupt mapping” table and a non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in Figure 1.

The maskable interrupts must be enabled by clearing the I bit in order to be serviced. However, disabled interrupts may be latched and processed when they are enabled (see external interrupts subsection).

Note: After reset, all interrupts are disabled.

When an interrupt has to be serviced:

– Normal processing is suspended at the end of the current instruction execution.

– The PC, X, A and CC registers are saved onto the stack.

– The I bit of the CC register is set to prevent additional interrupts.

– The PC is then loaded with the interrupt vector of the interrupt to service and the first instruction of the interrupt service routine is fetched (refer to the Interrupt Mapping table for vector addresses).

The interrupt service routine should finish with the IRET instruction which causes the contents of the saved registers to be recovered from the stack.

Note: As a consequence of the IRET instruction, the I bit is cleared and the main program resumes.

Priority Management

By default, a servicing interrupt cannot be interrupted because the I bit is set by hardware entering in interrupt routine.

In the case when several interrupts are simultaneously pending, an hardware priority defines which one will be serviced first (see the Interrupt Mapping table).

Interrupts and Low Power Mode

All interrupts allow the processor to leave the WAIT low power mode. Only external and specifically mentioned interrupts allow the processor to leave the HALT low power mode (refer to the “Exit from HALT” column in the Interrupt Mapping table).

8.1 NON MASKABLE SOFTWARE INTERRUPT

This interrupt is entered when the TRAP instruction is executed regardless of the state of the I bit. It is serviced according to the flowchart in Figure 1.

8.2 EXTERNAL INTERRUPTS

External interrupt vectors can be loaded into the PC register if the corresponding external interrupt occurred and if the I bit is cleared. These interrupts allow the processor to leave the HALT low power mode.

The external interrupt polarity is selected through the miscellaneous register or interrupt register (if available).

An external interrupt triggered on edge will be latched and the interrupt request automatically cleared upon entering the interrupt service routine.

Caution: The type of sensitivity defined in the Miscellaneous or Interrupt register (if available) applies to the ei source. In case of a NANDed source (as described in the I/O ports section), a low level on an I/O pin, configured as input with interrupt, masks the interrupt request even in case of rising-edge sensitivity.

8.3 PERIPHERAL INTERRUPTS

Different peripheral interrupt flags in the status register are able to cause an interrupt when they are active if both:

– The I bit of the CC register is cleared.

– The corresponding enable bit is set in the control register.

If any of these two conditions is false, the interrupt is latched and thus remains pending.

Clearing an interrupt request is done by:

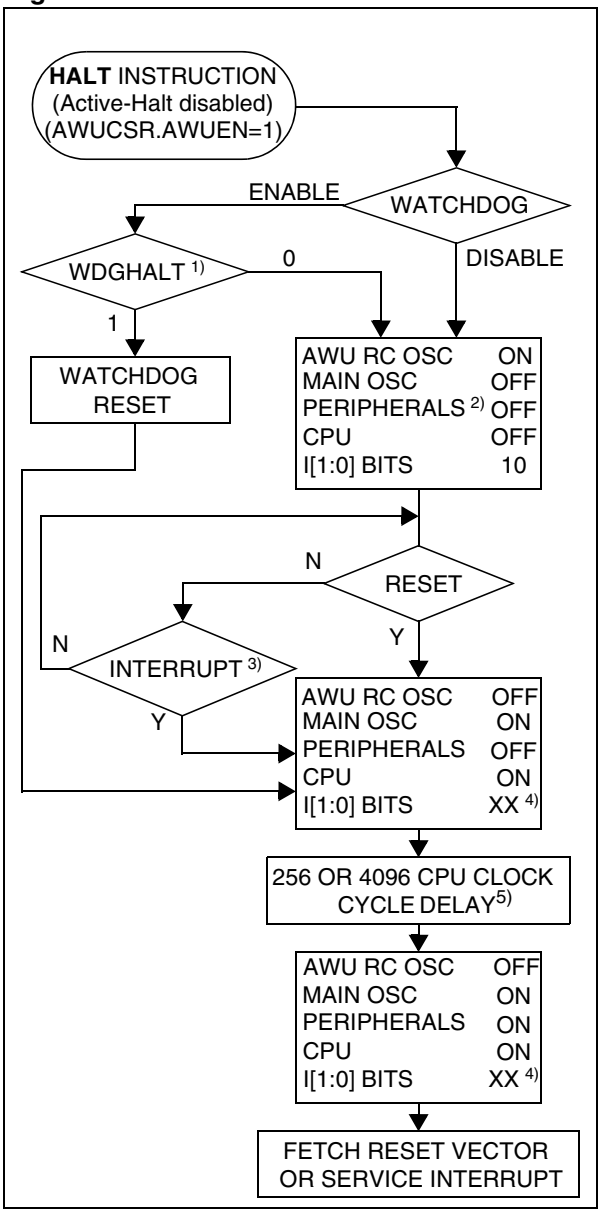
– Writing “0” to the corresponding bit in the status register or

– Access to the status register while the flag is set followed by a read or write of an associated register.

Note: The clearing sequence resets the internal latch. A pending interrupt (that is, waiting for being enabled) will therefore be lost if the clear sequence is executed.

POWER SAVING MODES (Cont'd)

Figure 31. AWUFH Mode Flow-chart



Notes:

1. WDGHALT is an option bit. See option byte section for more details.

2. Peripheral clocked with an external clock source can still be active.

3. Only an AWUFH interrupt and some specific interrupts can exit the MCU from HALT mode (such as external interrupt). Refer to Table 5, "Interrupt Mapping," on page 37 for more details.

4. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

5. If the PLL is enabled by option byte, it outputs the clock after an additional delay of $t_{STARTUP}$ (see Figure 13).

I/O PORTS (Cont'd)

Figure 32. I/O Port General Block Diagram

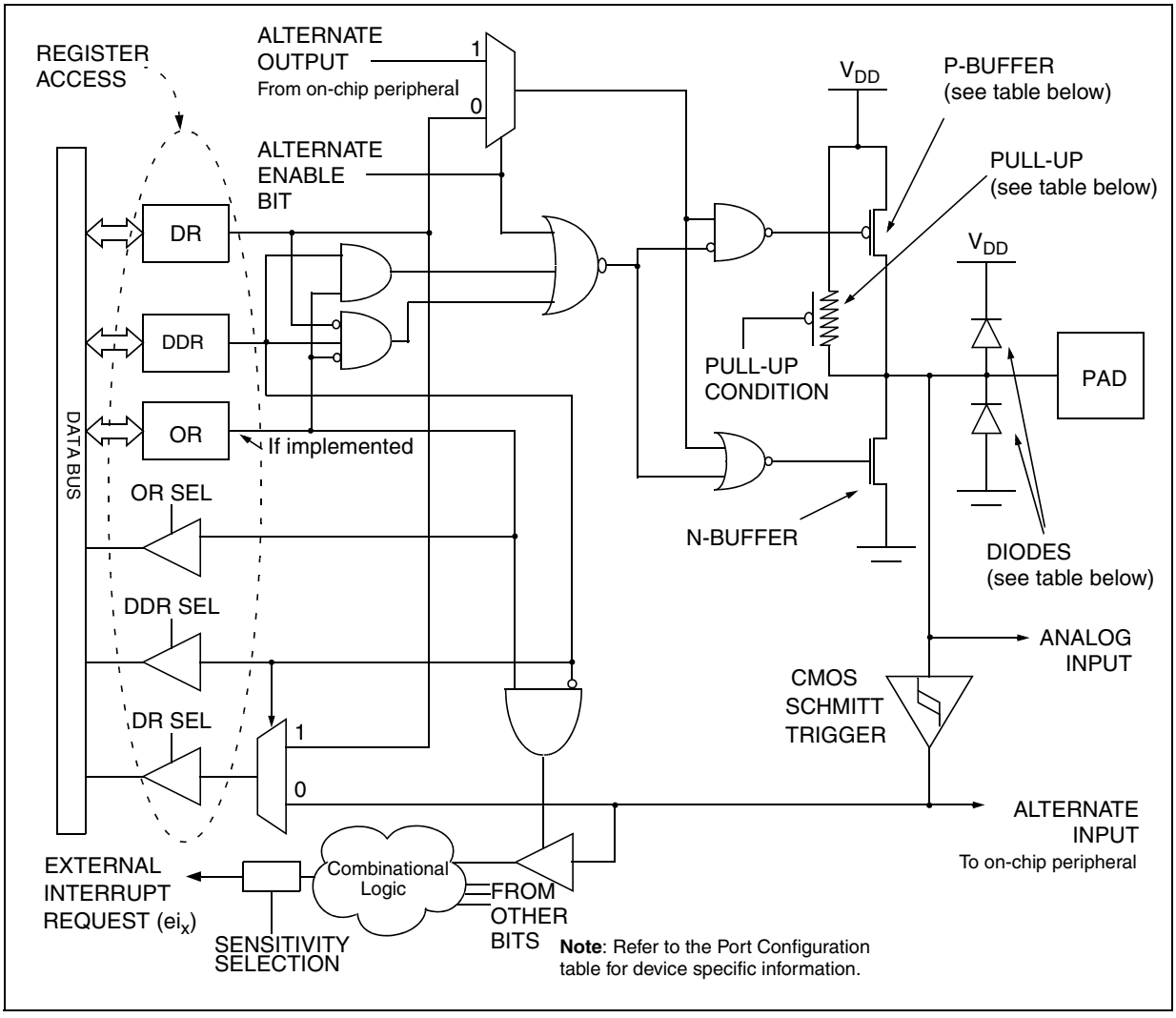


Table 8. I/O Port Mode Options

Configuration Mode		Pull-Up	P-Buffer	Diodes	
				to V_{DD}	to V_{SS}
Input	Floating with/without Interrupt	Off	Off	On	On
	Pull-up with/without Interrupt	On			
Output	Push-pull	Off	On		
	Open Drain (logic level)		Off		

Legend: Off - implemented not activated
On - implemented and activated

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

Figure 38. PWM Function

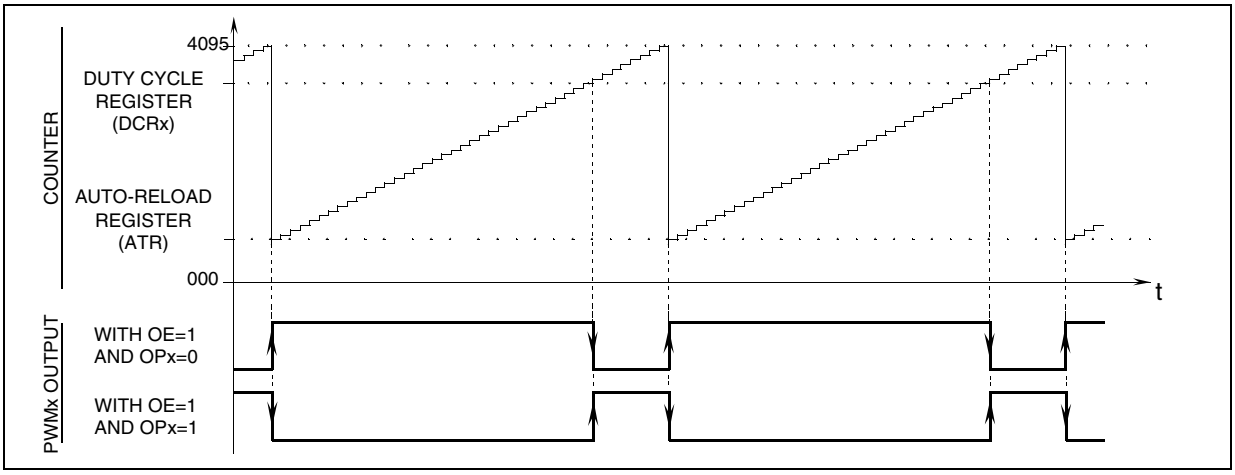
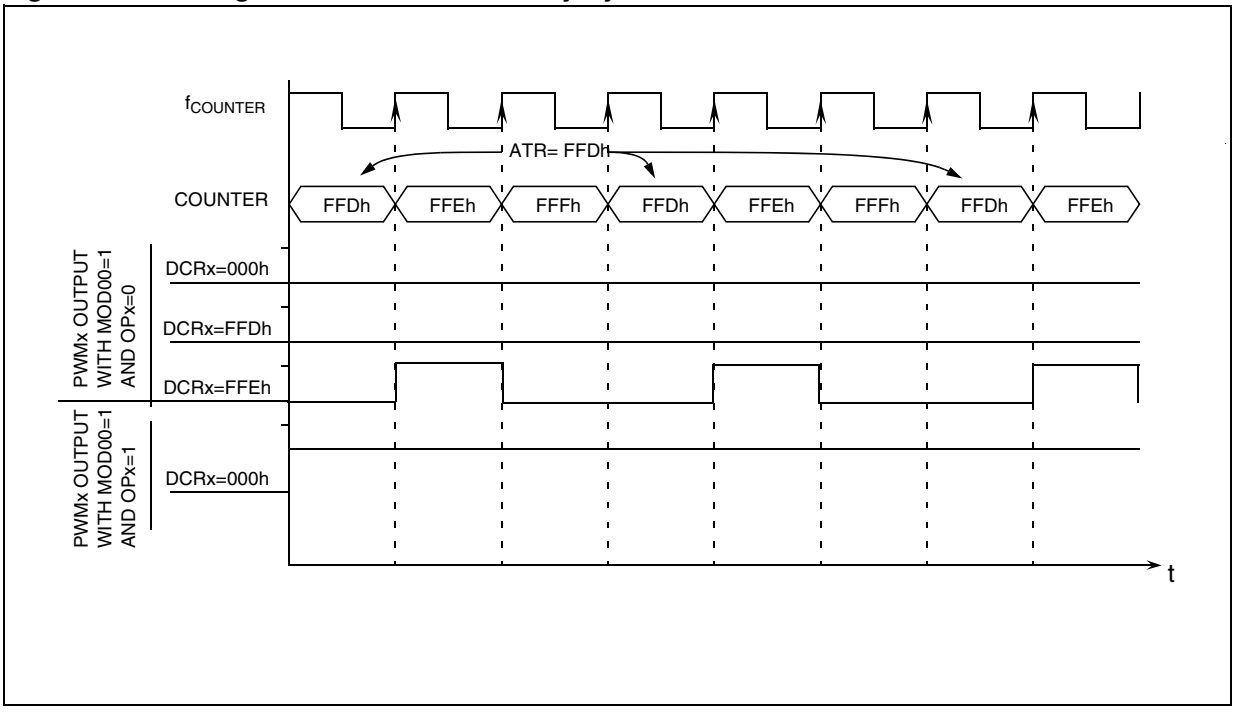


Figure 39. PWM Signal from 0% to 100% Duty Cycle



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.4 Low Power Modes

Mode	Description
WAIT	No effect on AT timer
HALT	AT timer halted.

11.2.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt	Exit from Active-Halt
Overflow Event	OVF1	OVIE1	Yes	No	Yes
AT4 IC Event	ICF	ICIE	Yes	No	No
CMP Event	CMPFx	CMPIE	Yes	No	No
Overflow Event2	OVF2	OVIE2	Yes	No	No

Note: The CMP and AT4 IC events are connected to the same interrupt vector.
The OVF event is mapped on a separate vector (see Interrupts chapter).
They generate an interrupt if the enable bit is set in the ATCSR register and the interrupt mask in the CC register is reset (RIM instruction).

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

BREAK CONTROL REGISTER (BREAKCR)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
BRSEL	BREDGE	BA	BPEN	PWM3	PWM2	PWM1	PWM0

Bit 7 = **BRSEL** Break Input Selection
This bit is read/write by software and cleared by hardware after reset. It selects the active Break signal from external BREAK pin and the output of the comparator.

0: External BREAK pin is selected for break mode.

1: Comparator output is selected for break mode.

Bit 6 = **BREDGE** Break Input Edge Selection
This bit is read/write by software and cleared by hardware after reset. It selects the active level of Break signal.

0: Low level of Break selected as active level.
1: High level of Break selected as active level.

Bit 5 = **BA** Break Active.
This bit is read/write by software, cleared by hardware after reset and set by hardware when the active level defined by the BREDGE bit is applied on the BREAK pin. It activates/deactivates the Break function.
0: Break not active
1: Break active

Bit 4 = **BPEN** Break Pin Enable.
This bit is read/write by software and cleared by hardware after Reset.
0: Break pin disabled
1: Break pin enabled

Bits 3:0 = **PWM[3:0]** Break Pattern.
These bits are read/write by software and cleared by hardware after a reset. They are used to force the four PWMx output signals into a stable state when the Break function is active and corresponding OEx bit is set.

PWMx DUTY CYCLE REGISTER HIGH (DCRxH)
Read / Write
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	DCR11	DCR10	DCR9	DCR8

Bits 15:12 = Reserved.

PWMx DUTY CYCLE REGISTER LOW (DCRxL)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
DCR7	DCR6	DCR5	DCR4	DCR3	DCR2	DCR1	DCR0

Bits 11:0 = **DCRx[11:0]** PWMx Duty Cycle Value
This 12-bit value is written by software. It defines the duty cycle of the corresponding PWM output signal (see Figure 4).

In PWM mode (OEx=1 in the PWMCR register) the DCR[11:0] bits define the duty cycle of the PWMx output signal (see Figure 4). In Output Compare mode, they define the value to be compared with the 12-bit upcounter value.

INPUT CAPTURE REGISTER HIGH (ATICRH)
Read only
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ICR11	ICR10	ICR9	ICR8

Bits 15:12 = Reserved.

INPUT CAPTURE REGISTER LOW (ATICRL)
Read only
Reset Value: 0000 0000 (00h)

7							0
ICR7	ICR6	ICR5	ICR4	ICR3	ICR2	ICR1	ICR0

SERIAL PERIPHERAL INTERFACE (Cont'd)

Table 17. SPI Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0031h	**SPIDR** Reset Value	MSB x	x	x	x	x	x	x	LSB x
0032h	**SPICR** Reset Value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0033h	**SPICSR** Reset Value	SPIF 0	WCOL 0	OVR 0	MODF 0	0	SOD 0	SSM 0	SSI 0

10-BIT A/D CONVERTER (ADC) (Cont'd)

Bit 2 = **AMPSEL** Amplifier Selection Bit
This bit is set and cleared by software.
0: Amplifier is not selected
1: Amplifier is selected

Note: When AMPSEL=1 it is mandatory that f_{ADC} be less than or equal to 2 MHz.

Bits 1:0 = **D[1:0]** LSB of Analog Converted Value

Table 18. ADC Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0034h	**ADCCSR**	EOC	SPEED	ADON	0	0	CH2	CH1	CH0
	Reset Value	0	0	0	0	0	0	0	0
0035h	**ADCDRH**	D9	D8	D7	D6	D5	D4	D3	D2
	Reset Value	x	x	x	x	x	x	x	x
0036h	**ADCDRL**	0	0	0	AMPCAL	SLOW	AMPSEL	D1	D0
	Reset Value	0	0	0	0	0	0	x	x

ANALOG COMPARATOR (Cont'd)

11.6.4 Register Description

Internal Voltage Reference Register (VREFCR)

Read/Write

Reset Value : 0000 0000 (00h)

7							0
VCEXT	VCBGR	VR3	VR2	VR1	VR0	0	0

Bit 7 = **VCEXT** External Voltage Reference for Comparator
This bit is set or cleared by software. It is used to connect the external reference voltage to the VN comparator input.
0: External reference voltage not connected to VN
1: External reference voltage connected to VN

Bit 6 = **VCBGR** Bandgap Voltage for Comparator
This bit is set or cleared by software. It is used to connect the bandgap voltage of 1.2V to the VN comparator input.
0: Bandgap voltage not connected to VN
1: Bandgap voltage connected to VN

Bits 5:2 = **VR[3:0]** Programmable Internal Voltage Reference Range Selection
These bits are set or cleared by software. They are used to select one of 16 different voltages available from the internal voltage reference module and connect it to comparator input VN.

Refer to Table 20.

Table 20. Voltage Reference Programming

VCEXT bit	VCBGR bit	VR3 bit	VR2 bit	VR1 bit	VR0 bit	VN Voltage
1	x	x	x	x	x	VEXT
0	1	x	x	x	x	1.2 bandgap
0	0	1	1	1	1	3.2V
0	0	1	1	1	0	3V
0	0	1	1	0	1	2.8V
0	0	1	1	0	0	2.6V
0	0	1	0	1	1	2.4V
0	0	1	0	1	0	2.2V
0	0	1	0	0	1	2V
0	0	1	0	0	0	1.8V
0	0	0	1	1	1	1.6V
0	0	0	1	1	0	1.4V
0	0	0	1	0	1	1.2V
0	0	0	1	0	0	1V
0	0	0	0	1	1	0.8V
0	0	0	0	1	0	0.6V
0	0	0	0	0	1	0.4V
0	0	0	0	0	0	0.2V

Bits 1:0 = Reserved, Must be kept cleared.

Comparator Control Register (CMPCR)

Read/Write

Reset Value : 1000 0000 (80h)

7							0
CHY-ST	0	CINV	CMPIF	CMPIE	CMP	COUT	CMPON

Bit 7= **CHYST** Comparator Hysteresis Enable

This bit is set or cleared by software and set by hardware reset. When this bit is set, the comparator hysteresis is enabled.
0: Hysteresis disabled
1: Hysteresis enabled
Note: To avoid spurious toggling of the output of the comparator due to noise on the voltage reference, it is recommended to enable the hysteresis.

Bit 6 = Reserved, Must be kept cleared

Bit 5 = **CINV** Comparator Output Inversion Select

This bit is set or cleared by software and cleared by hardware reset. When this bit is set, the comparator output is inverted.

If interrupt enable bit CMPIE is set in the CMPCR register, the CINV bit is also used to select which type of level transition on the comparator output will generate the interrupt. When this bit is reset, interrupt will be generated at the rising edge of the comparator output change (COMP signal, refer to Figure 62 on page 101). When this bit is set, interrupt will be generated at the falling edge of comparator output change (COMP signal, refer to Figure 62 on page 101).
0: Comparator output not inverted and interrupt generated at the rising edge of COMP
1: Comparator output inverted and interrupt generated at the falling edge of COMP

ST7 ADDRESSING MODES (cont'd)

12.1.1 Inherent

All Inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Inherent Instruction	Function
NOP	No operation
TRAP	S/W Interrupt
WFI	Wait For Interrupt (Low Power Mode)
HALT	Halt Oscillator (Lowest Power Mode)
RET	Subroutine Return
IRET	Interrupt Subroutine Return
SIM	Set Interrupt Mask
RIM	Reset Interrupt Mask
SCF	Set Carry Flag
RCF	Reset Carry Flag
RSP	Reset Stack Pointer
LD	Load
CLR	Clear
PUSH/POP	Push/Pop to/from the stack
INC/DEC	Increment/Decrement
TNZ	Test Negative or Zero
CPL, NEG	1 or 2 Complement
MUL	Byte Multiplication
SLL, SRL, SRA, RLC, RRC	Shift and Rotate Operations
SWAP	Swap Nibbles

12.1.2 Immediate

Immediate instructions have 2 bytes, the first byte contains the opcode, the second byte contains the operand value.

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit Compare
AND, OR, XOR	Logical Operations
ADC, ADD, SUB, SBC	Arithmetic Operations

12.1.3 Direct

In Direct instructions, the operands are referenced by their memory address.

The direct addressing mode consists of two submodes:

Direct (Short)

The address is a byte, thus requires only 1 byte after the opcode, but only allows 00 - FF addressing space.

Direct (Long)

The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

12.1.4 Indexed (No Offset, Short, Long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

The indirect addressing mode consists of three submodes:

Indexed (No Offset)

There is no offset (no extra byte after the opcode), and allows 00 - FF addressing space.

Indexed (Short)

The offset is a byte, thus requires only 1 byte after the opcode and allows 00 - 1FE addressing space.

Indexed (Long)

The offset is a word, thus allowing 64 Kbyte addressing space and requires 2 bytes after the opcode.

12.1.5 Indirect (Short, Long)

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two submodes:

Indirect (Short)

The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.

Indirect (Long)

The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

OPERATING CONDITIONS (Cont'd)

The RC oscillator and PLL characteristics are temperature-dependent and are grouped in four tables.

13.3.5.1 Devices with '"6" or "3"order code suffix (tested for T_A = -40 to +125°C) @ V_{DD} = 5V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	Internal RC oscillator frequency [1]					

Notes:

1. If the RC oscillator clock is selected, to improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

2. See "INTERNAL RC OSCILLATOR ADJUSTMENT" on page 23

3. Data based on characterization results, not tested in production

4. Averaged over a 4ms period. After the LOCKED bit is set, a period of t_{STAB} is required to reach ACC_{PLL} accuracy.

5. After the LOCKED bit is set ACC_{PLL} is max. 10% until t_{STAB} has elapsed. See Figure 13 on page 24.

6. This period is the phase servo loop period. During this period, the frequency remains unchanged.

7. Guaranteed by design.

OPERATING CONDITIONS (Cont'd)

Figure 68. Typical accuracy with RCCR=RCCR1 vs V_{DD}= 3-3.6V and Temperature

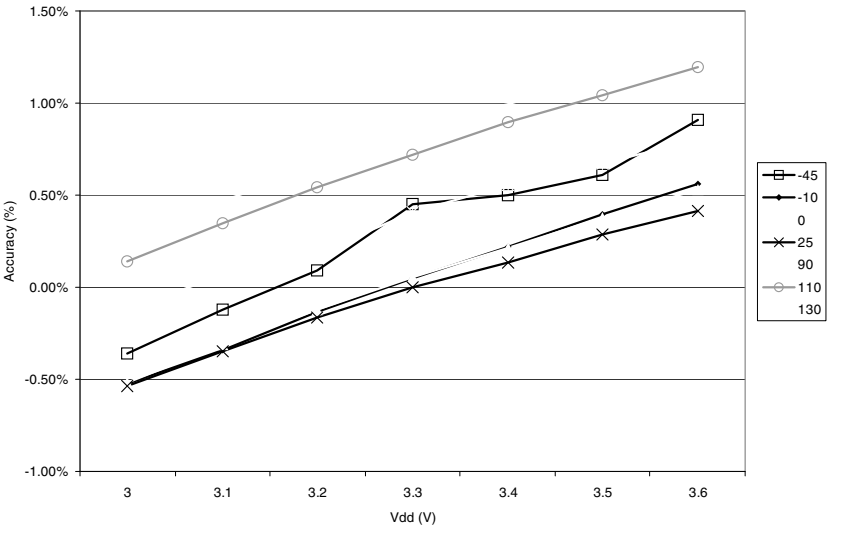
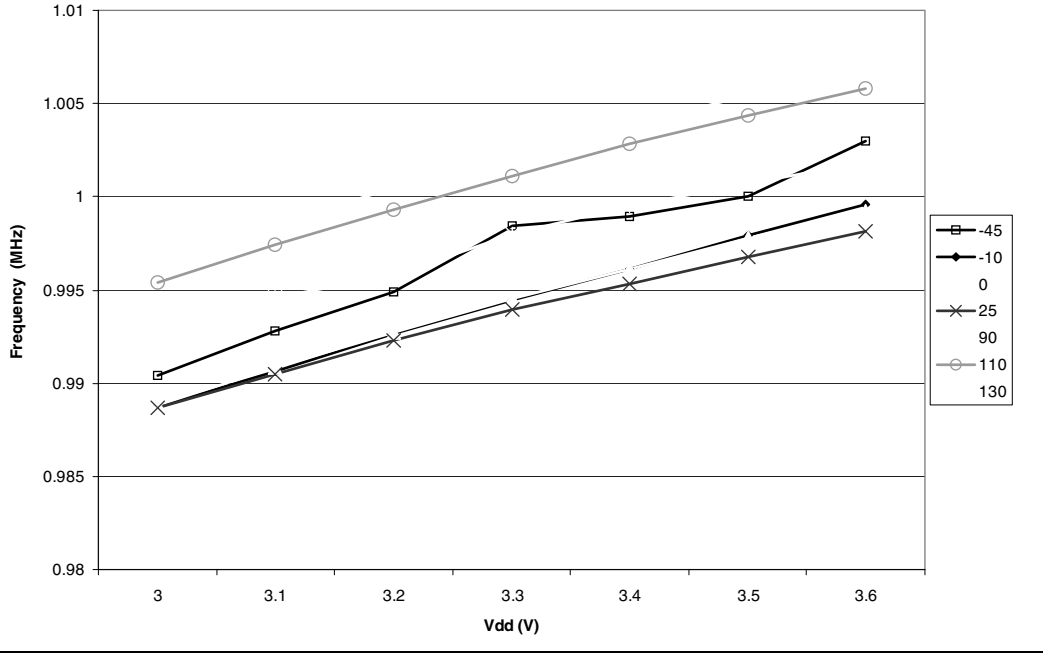


Figure 69. Typical RCCR1 vs V_{DD} and Temperature



13.6 MEMORY CHARACTERISTICS

T_A = -40°C to 125°C, unless otherwise specified

13.6.1 RAM and Hardware Registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode [1]	HALT mode (or RESET)	1.6			V

13.6.2 FLASH Program Memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage for Flash write/erase	Refer to operating range of V_{DD} with T_A, section 13.3.1 on page 112	2.7		5.5	V
t_{prog}	Programming time for 1~32 bytes [2]	T_A=–40 to +125°C		5	10	ms
	Programming time for 1.5 kBytes	T_A=+25°C		0.24	0.48	s
t_{RET}	Data retention [4]	T_A=+55°C[3]	20			years
N_{RW}	Write erase cycles	T_A=+25°C	10K			cycles
I_{DD}	Supply current [6]	Read / Write / Erase modes f_{CPU} = 8MHz, V_{DD} = 5.5V			2.6	mA
		No Read/No Write Mode			100	µA
		Power down mode / HALT		0	0.1	µA

13.6.3 EEPROM Data Memory

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating voltage for EEPROM write/erase	Refer to operating range of V_{DD} with T_A, section 13.3.1 on page 112	2.7		5.5	V
t_{prog}	Programming time for 1~32 bytes	T_A=–40 to +125°C		5	10	ms
t_{ret}	Data retention [4]	T_A=+55°C [3]	20			years
N_{RW}	Write erase cycles	T_A=+25°C	300K			cycles

Notes:

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in HALT mode or under RESET) or in hardware registers (only in HALT mode). Guaranteed by construction, not tested in production.

2. Up to 32 bytes can be programmed at a time.

3. The data retention time increases when the T_A decreases.

4. Data based on reliability test results and monitored in production.

5. Data based on characterization results, not tested in production.

6. Guaranteed by Design. Not tested in production.

EMC CHARACTERISTICS (Cont'd)

13.7.3 Absolute Maximum Ratings (Electrical Sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

13.7.3.1 Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Absolute Maximum Ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	8000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)	T_A=+25°C	400	

Note:

1. Data based on characterization results, not tested in production.

13.7.3.2 Static Latch-Up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Electrical Sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A=+25°C T_A=+85°C	A A

I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 81. Typical V_{OL} at V_{DD}=2.7V (standard)

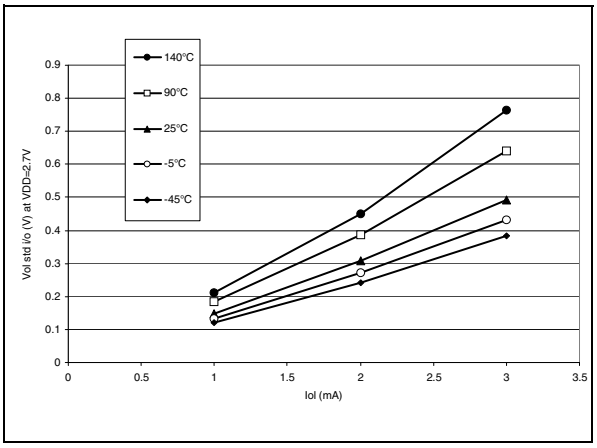


Figure 82. Typical V_{OL} at V_{DD}=3.3V (standard)

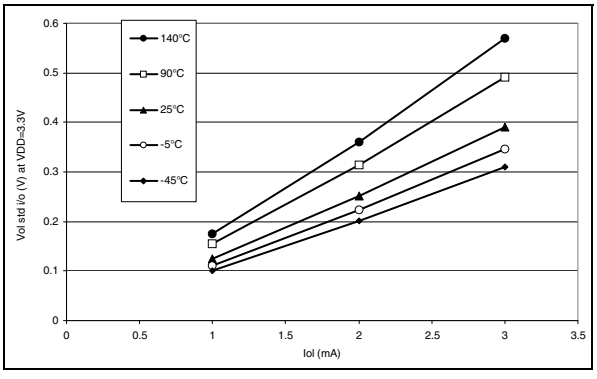


Figure 83. Typical V_{OL} at V_{DD}=5V (standard)

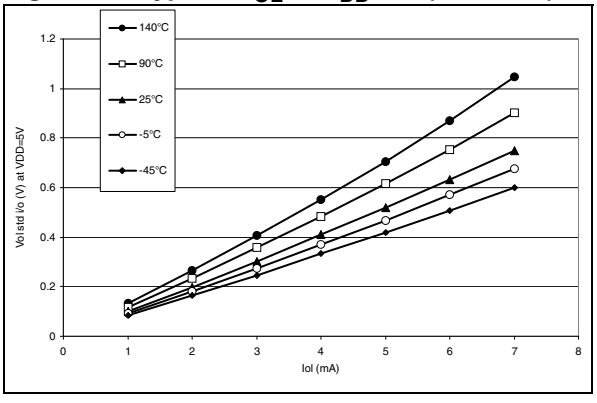


Figure 84. Typical V_{OL} at V_{DD}=2.7V (Port C)

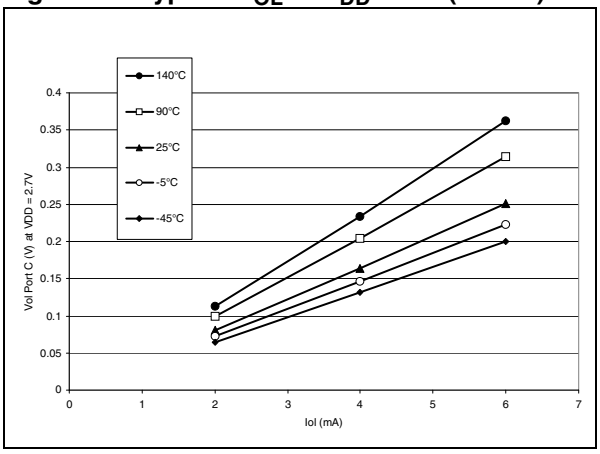


Figure 85. Typical V_{OL} at V_{DD}=3.3V (Port C)

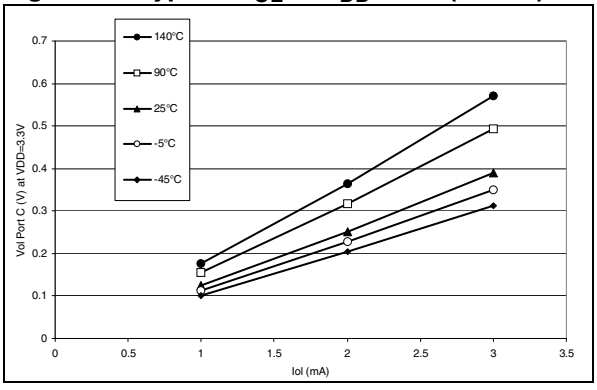
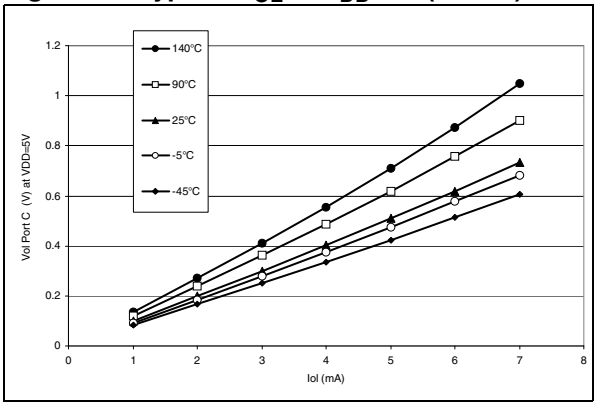


Figure 86. Typical V_{OL} at V_{DD}=5V (Port C)



ST7LITE1xB FASTROM microcontroller option list

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .
Reference/FASTROM Code*: . . . . . .
*FASTROM code name is assigned by STMicroelectronics.
FASTROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option):

FASTROM DEVICE:	2K	4K
VFQFPN20:	[ ] ST7PLIT19BF0Ux	[ ] ST7PLIT19BF1Ux
SO20:	[ ] ST7PLIT19BF0Mx	[ ] ST7PLIT19BF1Mx
PDIP20:	[ ] ST7PLIT19BF0Bx	[ ] ST7PLIT19BF1Bx
SO16:	[ ] ST7PLIT19BY0Mx	[ ] ST7PLIT19BY1Mx
PDIP16:	[ ] ST7PLIT19BY0Bx	[ ] ST7PLIT19BY1Bx

Warning: Addresses DEE0h, DEE1h, DEE2h and DEE3h are reserved areas for ST to program RCCR0 and RCCR1 (see section 7.1 on page 23).

Conditioning (check only one option, do not specify for DIP package) :

VFQFPN	[ ] Tape & Reel	[ ] Tray
SO	[ ] Tape & Reel	[ ] Tube

Special marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Maximum character count: 8 char. max _ _ _ _ _ _ _ _

Temperature range: [ ] -40°C to +85°C [ ] -40°C to +125°C

Watchdog selection (WDG_SW): [ ] Software activation [ ] Hardware activation

Watchdog reset on Halt (WDG_HALT): [ ] Reset [ ] No Reset

LVD reset (LVD): [ ] Disabled [ ] Enabled
[ ] Highest threshold
[ ] Medium threshold
[ ] Lowest threshold

Sector 0 size (SEC): [ ] 0.5K [ ] 1K [ ] 2K [ ] 4K

Readout protection (FMP_R): [ ] Disabled [ ] Enabled

Flash write protection (FMP_W): [ ] Disabled [ ] Enabled

RC oscillator (OSC) : [ ] Disabled [ ] Enabled

Clock source selection (CKSEL):
(if OSC disabled) [ ] External crystal / ceramic resonator:
[ ] External Clock on PB4
[ ] External Clock on PC0

PLL (PLLOFF): [ ] Disabled [ ] Enabled

PLL factor (PLLx4x8): [ ] PLLx4 [ ] PLLx8

PLL32 (PLL32OFF): [ ] Disabled [ ] Enabled

Comments : . . . . . .
Supply operating range in the application : . . . . . .
Notes . . . . . .
Date : . . . . . .
Signature : . . . . . .

Important note : Not all configurations are available. See Table 27 on page 150 for authorized option byte combinations.

ST7LITE1xB FASTROM microcontroller option list

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .
Reference/FASTROM Code*: . . . . . .
*FASTROM code name is assigned by STMicroelectronics.
FASTROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option):

FASTROM DEVICE:	2K	4K
VFQFPN20:	[ ] ST7PLIT19BF0Ux	[ ] ST7PLIT19BF1Ux
SO20:	[ ] ST7PLIT19BF0Mx	[ ] ST7PLIT19BF1Mx
PDIP20:	[ ] ST7PLIT19BF0Bx	[ ] ST7PLIT19BF1Bx
SO16:	[ ] ST7PLIT19BY0Mx	[ ] ST7PLIT19BY1Mx
PDIP16:	[ ] ST7PLIT19BY0Bx	[ ] ST7PLIT19BY1Bx

Warning: Addresses DEE0h, DEE1h, DEE2h and DEE3h are reserved areas for ST to program RCCR0 and RCCR1 (see section 7.1 on page 23).

Conditioning (check only one option, do not specify for DIP package) :

VFQFPN	[ ] Tape & Reel	[ ] Tray
SO	[ ] Tape & Reel	[ ] Tube

Special marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Maximum character count: 8 char. max _ _ _ _ _ _ _ _

Temperature range: [ ] -40°C to +85°C [ ] -40°C to +125°C

Watchdog selection (WDG_SW): [ ] Software activation [ ] Hardware activation

Watchdog reset on Halt (WDG_HALT): [ ] Reset [ ] No Reset

LVD reset (LVD): [ ] Disabled [ ] Enabled
[ ] Highest threshold
[ ] Medium threshold
[ ] Lowest threshold

Sector 0 size (SEC): [ ] 0.5K [ ] 1K [ ] 2K [ ] 4K

Readout protection (FMP_R): [ ] Disabled [ ] Enabled

Flash write protection (FMP_W): [ ] Disabled [ ] Enabled

RC oscillator (OSC) : [ ] Disabled [ ] Enabled

Clock source selection (CKSEL):
(if OSC disabled) [ ] External crystal / ceramic resonator:
[ ] External Clock on PB4
[ ] External Clock on PC0

PLL (PLLOFF): [ ] Disabled [ ] Enabled

PLL factor (PLLx4x8): [ ] PLLx4 [ ] PLLx8

PLL32 (PLL32OFF): [ ] Disabled [ ] Enabled

Comments : . . . . . .
Supply operating range in the application : . . . . . .
Notes . . . . . .
Date : . . . . . .
Signature : . . . . . .

Important note : Not all configurations are available. See Table 27 on page 150 for authorized option byte combinations.

16 REVISION HISTORY

Date	Revision	Main changes
20-Dec-05	1	Initial release on internet
		Added reset default state in bold for RESET, PC0 and PC1 in Table 1, “Device Pin Description,” on page 7 Changed note below Figure 9 on page 17 and the last paragraph of “ACCESS ERROR HANDLING” on page 18 Modified note 3 in Table 2, “Hardware Register Map,” on page 10, changed LTICR reset value and replaced h by b for LTCSR1, ATCSR and SICSR reset values Added note to Figure 14 on page 26 Modified caution in section 7.2 on page 23 Added note 2 in “EXTERNAL INTERRUPT CONTROL REGISTER (EICR)” on page 38 and changed “External Interrupt Function” on page 48 Removed references to true open drain in Table 8 on page 50, Table 9 on page 51 and notes Replaced Auto reload timer 3 by Auto reload timer 4 in section 11.2 on page 57 Modified the BA bit description in the BREAKCR register in section 11.2.6 on page 70 Changed order of Section 11.3.3.2 and section 11.3.3.3 on page 80 and removed two paragraphs before section 11.3.4 on page 81 Modified Section 11.3.3.2 Modified bit names in the description of LTARR and LTCNTR registers in section 11.3.6 on page 81 Added important note in
20-July-06	2	