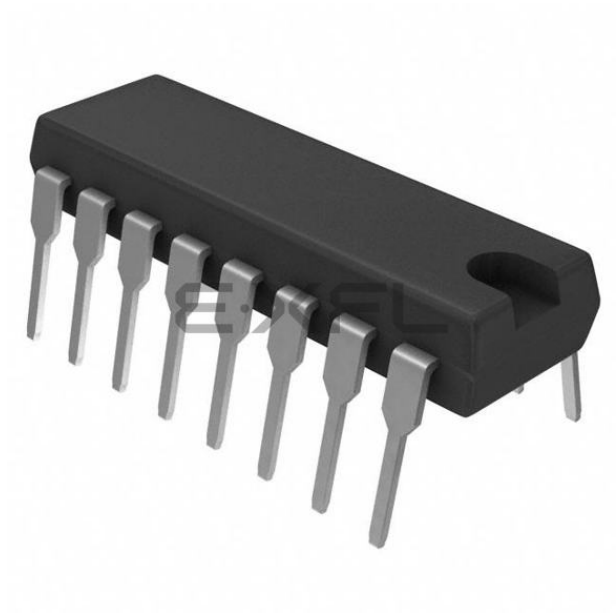


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	11
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flit15by0b6

3 REGISTER & MEMORY MAP

As shown in Figure 5, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, 256 bytes of RAM, 128 bytes of data EEPROM and up to 4 Kbytes of flash program memory. The RAM space includes up to 128 bytes for the stack from 180h to 1FFh.

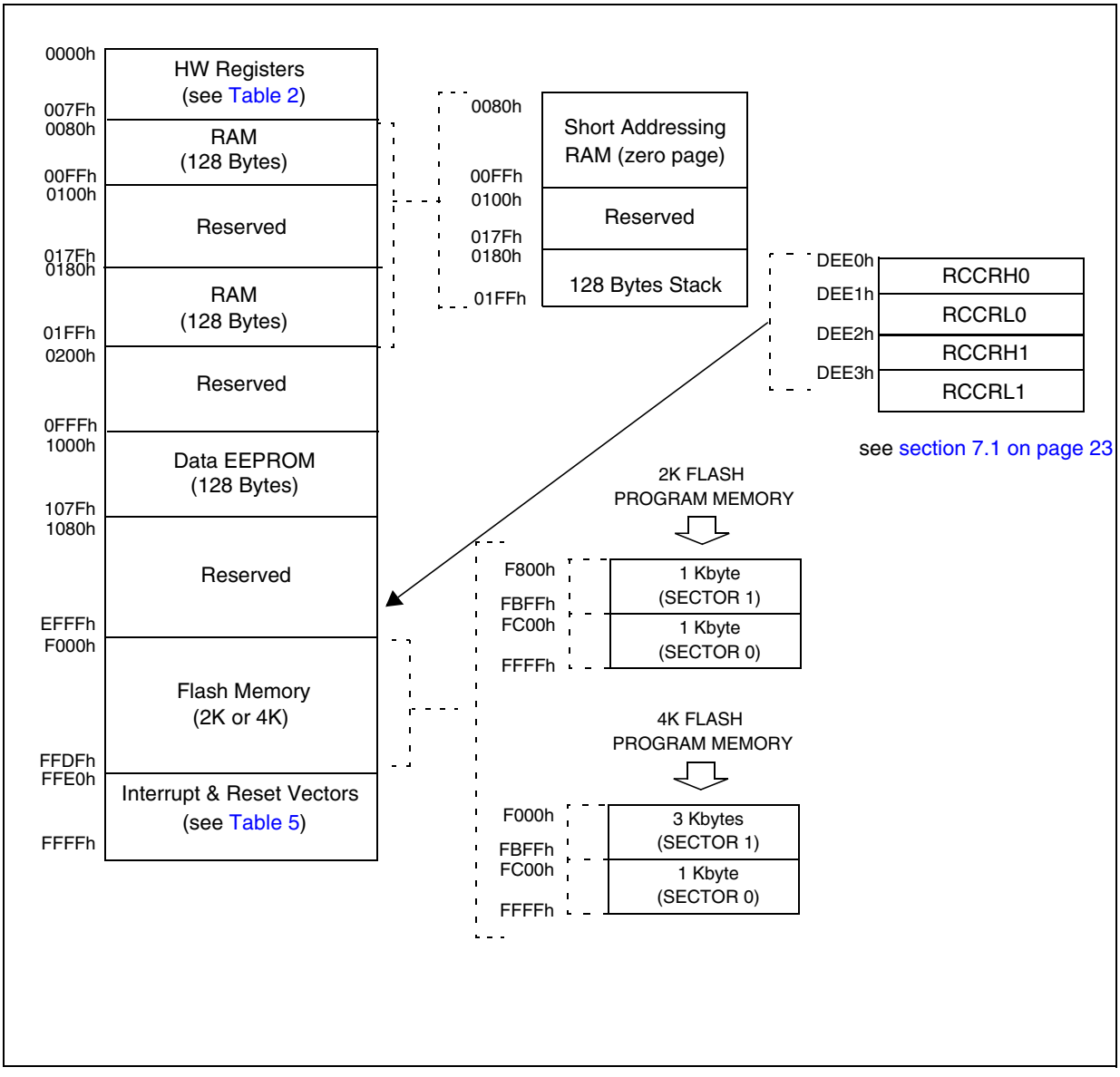
The highest address bytes contain the user reset and interrupt vectors.

The Flash memory contains two sectors (see Figure 5) mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in Sector 0 (F000h-FFFFh).

The size of Flash Sector 0 and other device options are configurable by Option byte (refer to section 15.1 on page 149).

IMPORTANT: Memory locations marked as "Reserved" must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 5. Memory Map



FLASH PROGRAM MEMORY (Cont'd)

4.4 ICC interface

ICP needs a minimum of 4 and up to 6 pins to be connected to the programming tool. These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input serial data pin
- OSC1: main clock input for external source (not required on devices without OSC1/OSC2 pins)
- V_{DD}: application board power supply (optional, see Note 3)

Notes:

1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2. During the ICP session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1K). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R>1K or a reset management IC with open drain output and pull-up resistor>1K, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

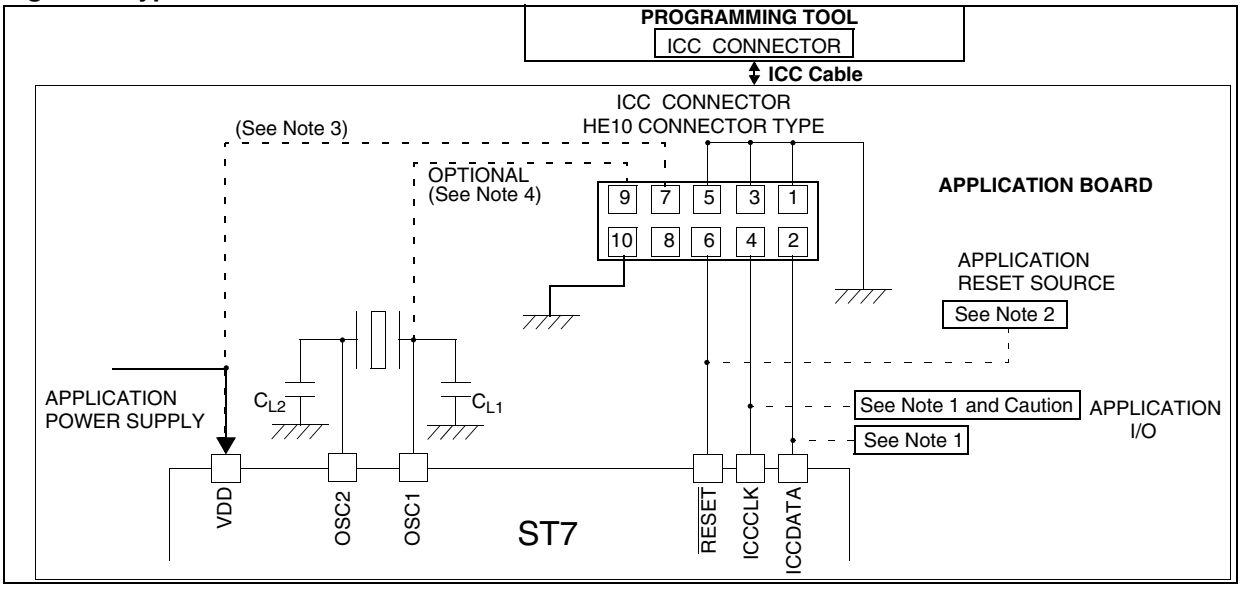
3. The use of pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4. Pin 9 has to be connected to the OSC1 pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC2 grounded in this case.

5. In 38-pulse ICC mode, the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. For ST7LITE10B devices which do not support the internal RC oscillator, the "option byte disabled" mode must be used (35-pulse ICC mode entry, clock provided by the tool).

Caution: During normal operation the ICCCLK pin must be pulled- up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

Figure 6. Typical ICC Interface



7 SUPPLY, RESET AND CLOCK MANAGEMENT

The device includes a range of utility features for securing the application in critical situations (for example in case of a power brown-out), and reducing the number of external components.

Main features

- Clock Management
  - 1 MHz internal RC oscillator (enabled by option byte, available on ST7LITE15B and ST7LITE19B devices only)
  - 1 to 16 MHz External crystal/ceramic resonator (selected by option byte)
  - External Clock Input (enabled by option byte)
  - PLL for multiplying the frequency by 8 or 4 (enabled by option byte)
  - For clock ART counter only: PLL32 for multiplying the 8 MHz frequency by 4 (enabled by option byte). The 8 MHz input frequency is mandatory and can be obtained in the following ways:
    - –1 MHz RC + PLLx8
    - –16 MHz external clock (internally divided by 2)
    - –2 MHz. external clock (internally divided by 2) + PLLx8
    - –Crystal oscillator with 16 MHz output frequency (internally divided by 2)
- Reset Sequence Manager (RSM)
- System Integrity Management (SI)
  - Main supply Low voltage detection (LVD) with reset generation (enabled by option byte)
  - Auxiliary Voltage detector (AVD) with interrupt capability for monitoring the main supply (enabled by option byte)

7.1 INTERNAL RC OSCILLATOR ADJUSTMENT

The device contains an internal RC oscillator with an accuracy of 1% for a given device, temperature and voltage range (4.5V-5.5V). It must be calibrated to obtain the frequency required in the application. This is done by software writing a 10-bit calibration value in the RCCR (RC Control Register) and in the bits 6:5 in the SICSR (SI Control Status Register).

Whenever the microcontroller is reset, the RCCR returns to its default value (FFh), i.e. each time the device is reset, the calibration value must be loaded in the RCCR. Predefined calibration values are stored in EEPROM for 3 and 5V V_{DD} supply voltages at 25°C, as shown in the following table.

RCCR	Conditions	ST7LITE1xB Address
RCCRH0	V_{DD}=5V T_A=25°C f_{RC}=1MHz	DEE0h [1] (CR[9:2])
RCCRL0		DEE1h [1] (CR[1:0])
RCCRH1	V_{DD}=3.3V T_A=25°C f_{RC}=1MHz	DEE2h [1] (CR[9:2])
RCCRL1		DEE3h [1] (CR[1:0])

1. DEE0h, DEE1h, DEE2h and DEE3h addresses are located in a reserved area of non-volatile memory. They are read-only bytes for the application code. This area cannot be erased or programmed by any ICC operation.

For compatibility reasons with the SICSR register, CR[1:0] bits are stored in the 5th and 6th position of DEE1 and DEE3 addresses.

Notes:

– In 38-pulse ICC mode, the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. For ST7LITE10B devices which do not support the internal RC oscillator, the “option byte disabled” mode must be used (35-pulse ICC mode entry, clock provided by the tool).

– See “ELECTRICAL CHARACTERISTICS” on page 110. for more information on the frequency and accuracy of the RC oscillator.

– To improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

– These bytes are systematically programmed by ST, including on FASTROM devices.

Caution: If the voltage or temperature conditions change in the application, the frequency may need to be recalibrated.

Refer to application note AN1324 for information on how to calibrate the RC frequency using an external reference signal.

7.2 PHASE LOCKED LOOP

The PLL can be used to multiply a 1MHz frequency from the RC oscillator or the external clock by 4 or 8 to obtain f_{OSC} of 4 or 8 MHz. The PLL is enabled and the multiplication factor of 4 or 8 is selected by 2 option bits.

– The x4 PLL is intended for operation with V_{DD} in the 2.7V to 3.3V range

10 I/O PORTS

10.1 INTRODUCTION

The I/O ports allow data transfer. An I/O port can contain up to 8 pins. Each pin can be programmed independently either as a digital input or digital output. In addition, specific pins may have several other functions. These functions can include external interrupt, alternate signal input/output for on-chip peripherals or analog input.

10.2 FUNCTIONAL DESCRIPTION

A Data Register (DR) and a Data Direction Register (DDR) are always associated with each port. The Option Register (OR), which allows input/output options, may or may not be implemented. The following description takes into account the OR register. Refer to the Port Configuration table for device specific information.

An I/O pin is programmed using the corresponding bits in the DDR, DR and OR registers: bit x corresponding to pin x of the port.

Figure 32 shows the generic I/O block diagram.

10.2.1 Input Modes

Clearing the DDRx bit selects input mode. In this mode, reading its DR bit returns the digital value from that I/O pin.

If an OR bit is available, different input modes can be configured by software: floating or pull-up. Refer to I/O Port Implementation section for configuration.

Notes:

1. Writing to the DR modifies the latch value but does not change the state of the input pin.
2. Do not use read/modify/write instructions (BSET/BRES) to modify the DR register.

10.2.1.1 External Interrupt Function

Depending on the device, setting the ORx bit while in input mode can configure an I/O as an input with interrupt. In this configuration, a signal edge or level input on the I/O generates an interrupt request via the corresponding interrupt vector (eix).

Falling or rising edge sensitivity is programmed independently for each interrupt vector. The External Interrupt Control Register (EICR) or the Miscellaneous Register controls this sensitivity, depending on the device.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see pinout description and interrupt section). If several I/O interrupt pins on the same interrupt vector are selected simultaneously, they are logically combined. For this reason if one of the interrupt pins is tied low, it may mask the others.

External interrupts are hardware interrupts. Fetching the corresponding interrupt vector automatically clears the request latch. Changing the sensitivity of a particular external interrupt clears this pending interrupt. This can be used to clear unwanted pending interrupts.

Spurious interrupts

When enabling/disabling an external interrupt by setting/resetting the related OR register bit, a spurious interrupt is generated if the pin level is low and its edge sensitivity includes falling/rising edge. This is due to the edge detector input which is switched to '1' when the external interrupt is disabled by the OR register.

To avoid this unwanted interrupt, a "safe" edge sensitivity (rising edge for enabling and falling edge for disabling) has to be selected before changing the OR register bit and configuring the appropriate sensitivity again.

Caution: In case a pin level change occurs during these operations (asynchronous signal input), as interrupts are generated according to the current sensitivity, it is advised to disable all interrupts before and to reenable them after the complete previous sequence in order to avoid an external interrupt occurring on the unwanted edge.

This corresponds to the following steps:

1. To enable an external interrupt:
   - set the interrupt mask with the SIM instruction (in cases where a pin level change could occur)
   - select rising edge
   - enable the external interrupt through the OR register
   - select the desired sensitivity if different from rising edge
   - reset the interrupt mask with the RIM instruction (in cases where a pin level change could occur)
2. To disable an external interrupt:
   - set the interrupt mask with the SIM instruction SIM (in cases where a pin level change could occur)
   - select falling edge
   - disable the external interrupt through the OR register

I/O PORTS (Cont'd)

Figure 32. I/O Port General Block Diagram

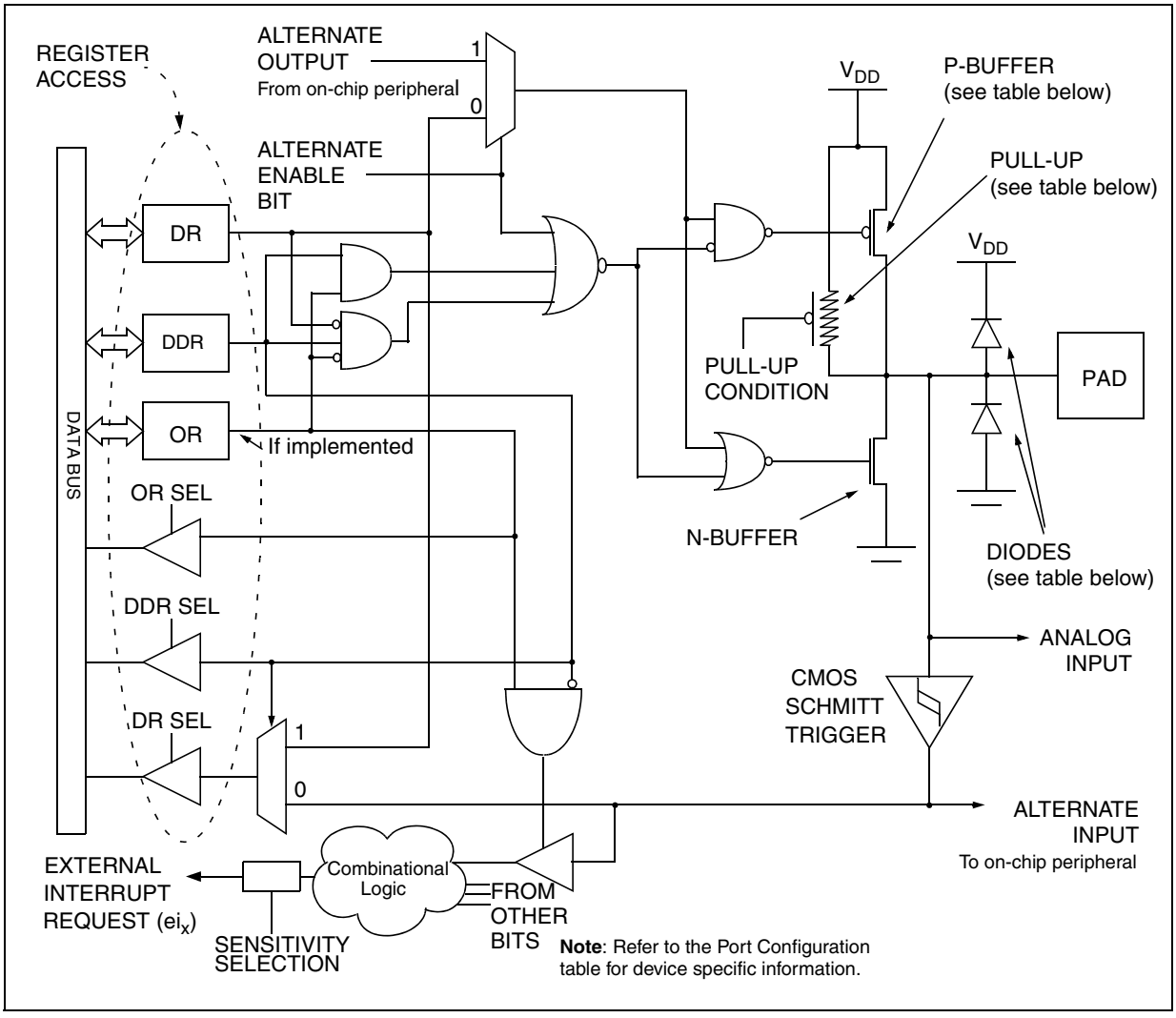


Table 8. I/O Port Mode Options

Configuration Mode		Pull-Up	P-Buffer	Diodes	
				to V_{DD}	to V_{SS}
Input	Floating with/without Interrupt	Off	Off	On	On
	Pull-up with/without Interrupt	On			
Output	Push-pull	Off	On		
	Open Drain (logic level)		Off		

Legend: Off - implemented not activated
On - implemented and activated

11.2 DUAL 12-BIT AUTORELOAD TIMER 4 (AT4)

11.2.1 Introduction

The 12-bit Autoreload Timer can be used for general-purpose timing functions. It is based on one or two free-running 12-bit upcounters with an input capture register and four PWM output channels. There are 7 external pins:

– Four PWM outputs

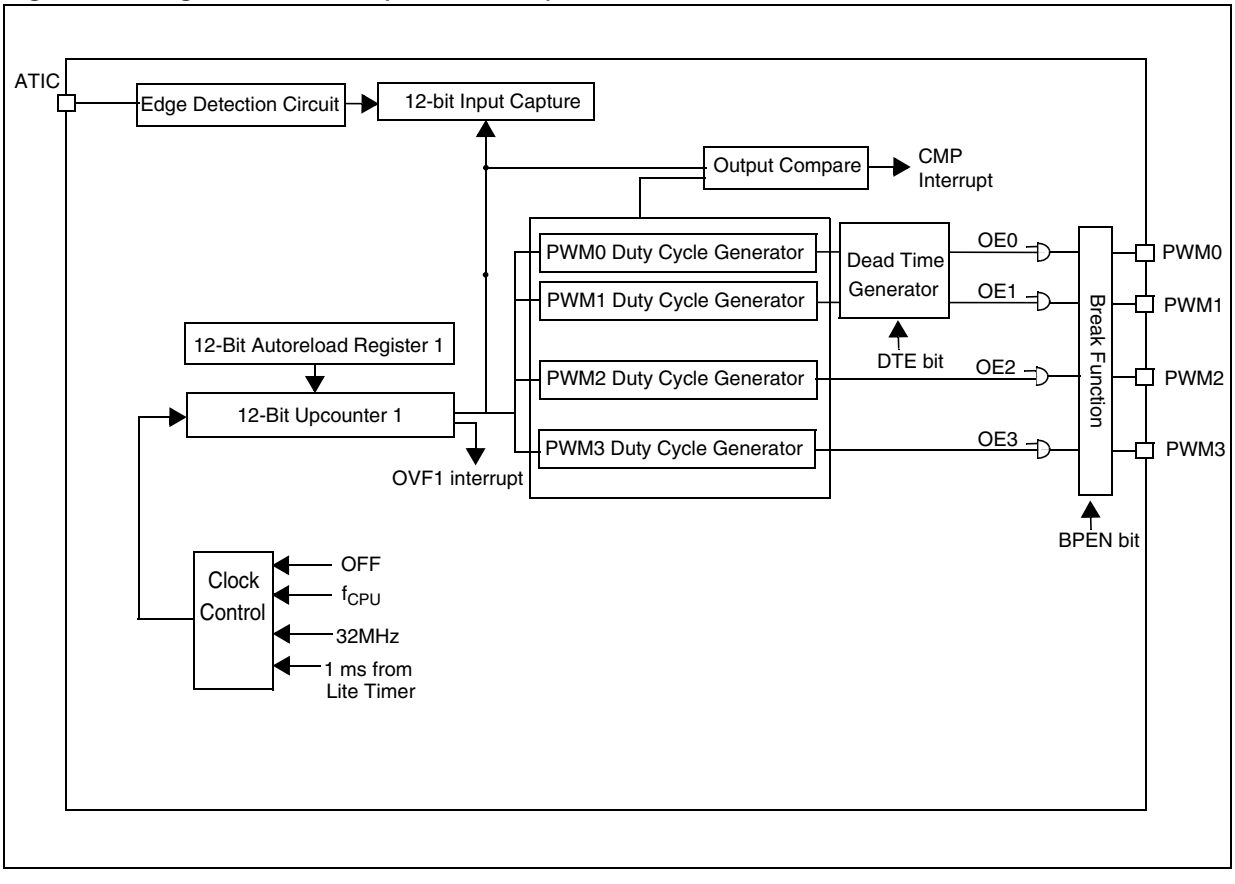
– ATIC/LTIC pins for the Input Capture function

– BREAK pin for forcing a break condition on the PWM outputs

11.2.2 Main Features

- Single Timer or Dual Timer mode with two 12-bit upcounters (CNTR1/CNTR2) and two 12-bit autoreload registers (ATR1/ATR2)
- Maskable overflow interrupts
- PWM mode
  - Generation of four independent PWMx signals
  - Dead time generation for Half bridge driving mode with programmable dead time
  - Frequency 2 kHz - 4 MHz (@ 8 MHz f_{CPU})
  - Programmable duty-cycles
  - Polarity control
  - Programmable output modes
- Output Compare Mode
- Input Capture Mode
  - 12-bit input capture register (ATICR)
  - Triggered by rising and falling edges
  - Maskable IC interrupt
  - Long range input capture
- Internal/External Break control
- Flexible Clock control
- One Pulse mode on PWM2/3
- Force Update

Figure 35. Single Timer Mode (ENCNTR2=0)



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.3.3 Break Function

The break function can be used to perform an emergency shutdown of the application being driven by the PWM signals.

The break function is activated by the external BREAK pin or internal comparator output. This can be selected by using the BRSEL bit in BREAKCR Register. In order to use the break function it must be previously enabled by software setting the BPEN bit in the BREAKCR register.

The Break active level can be programmed by the BREDGE bit in the BREAKCR register. When an active level is detected on the BREAK pin, the BA bit is set and the break function is activated. In this case, the PWM signals are forced to BREAK value if respective OEx bit is set in PWMCR register.

Software can set the BA bit to activate the break function without using the BREAK pin. The BREN1 and BREN2 bits in the BREAKEN Register are used to enable the break activation on the 2 counters respectively. In Dual Timer Mode, the break for PWM2 and PWM3 is enabled by the BREN2 bit. In Single Timer Mode, the BREN1 bit enables the break for all PWM channels.

When a break function is activated (BA bit =1 and BREN1/BREN2 =1):

– The break pattern (PWM[3:0] bits in the BREAKCR) is forced directly on the PWMx output pins if respective OEx is set. (after the inverter).

– The 12-bit PWM counter CNTR1 is put to its reset value, i.e. 00h (if BREN1 = 1).

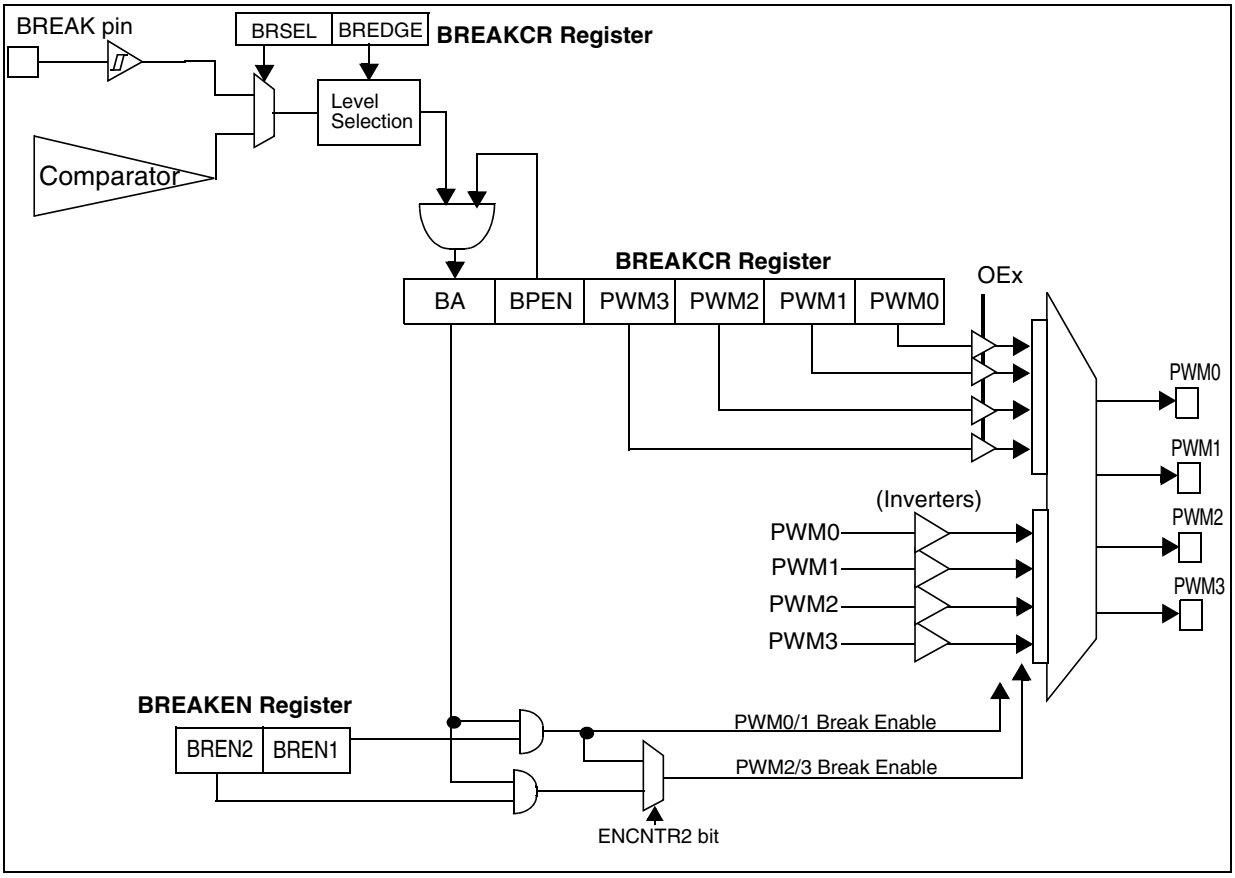
– The 12-bit PWM counter CNTR2 is put to its reset value,i.e. 00h (if BREN2 = 1).

– ATR1, ATR2, Preload and Active DCRx are put to their reset values.

– Counters stop counting.

When the break function is deactivated after applying the break (BA bit goes from 1 to 0 by software), Timer takes the control of PWM ports.

Figure 41. Block Diagram of Break Function



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

AUTORELOAD REGISTER (ATR1H)
Read / Write
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ATR11	ATR10	ATR9	ATR8

AUTORELOAD REGISTER (ATR1L)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

Bits 11:0 = **ATR1[11:0]** *Autoreload Register 1.*
This is a 12-bit register which is written by software. The ATR1 register value is automatically loaded into the upcounter CNTR1 when an overflow occurs. The register value is used to set the PWM frequency.

PWM OUTPUT CONTROL REGISTER (PWMCR)
Read/Write
Reset Value: 0000 0000 (00h)

7							0
0	OE3	0	OE2	0	OE1	0	OE0

Bits 7:0 = **OE[3:0]** *PWMx output enable*.
These bits are set and cleared by software and cleared by hardware after a reset.
0: PWM mode disabled. PWMx Output Alternate Function disabled (I/O pin free for general purpose I/O)
1: PWM mode enabled

PWMx CONTROL STATUS REGISTER (PWMxCSR)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	OP_EN	OPEDGE	OPx	CMPFx

Bits 7:4= Reserved, must be kept cleared.

Bit 3 = OP_EN *One Pulse Mode Enable*

This bit is read/write by software and cleared by hardware after a reset. This bit enables the One Pulse feature for PWM2 and PWM3. **(Only available for PWM3CSR)**

0: One Pulse mode disabled for PWM2/3.

1: One Pulse mode enabled for PWM2/3.

Bit 2 = OPEDGE *One Pulse Edge Selection.*

This bit is read/write by software and cleared by hardware after a reset. This bit selects the polarity of the LTIC signal for One Pulse feature. This bit will be effective only if OP_EN bit is set. **(Only available for PWM3CSR)**

0: Falling edge of LTIC is selected.

1: Rising edge of LTIC is selected.

Bit 1 = **OPx** *PWMx Output Polarity.*
This bit is read/write by software and cleared by hardware after a reset. This bit selects the polarity of the PWM signal.
0: The PWM signal is not inverted.
1: The PWM signal is inverted.

Bit 0 = **CMPFx** PWMx *Compare Flag.*
This bit is set by hardware and cleared by software by reading the PWMxCSR register. It indicates that the upcounter value matches the Active DCRx register value.
0: Upcounter value does not match DCRx value.
1: Upcounter value matches DCRx value.

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

Bit 1= **TRAN2** *Transfer enable2*
This bit is read/write by software, cleared by hardware after each completed transfer and set by hardware after reset. It controls the transfers on CNTR2.

It allows the value of the Preload DCRx registers to be transferred to the Active DCRx registers after the next overflow event.

The OPx bits are transferred to the shadow OPx bits in the same way.

Notes:

1. DCR2/3 transfer will be controlled using this bit if ENCNTR2 bit is set.
2. This bit must not be reset by software

Bit 0 = **TRAN1** *Transfer enable* 1
This bit is read/write by software, cleared by hardware after each completed transfer and set by hardware after reset. It controls the transfers on CNTR1. It allows the value of the Preload DCRx registers to be transferred to the Active DCRx registers after the next overflow event.

The OPx bits are transferred to the shadow OPx bits in the same way.

Notes:

1. DCR0,1 transfers are always controlled using this bit.

2. DCR2/3 transfer will be controlled using this bit if ENCNTR2 is reset.

3.This bit must not be reset by software

AUTORELOAD REGISTER2 (ATR2H)
Read / Write
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	ATR11	ATR10	ATR9	ATR8

AUTORELOAD REGISTER (ATR2L)
Read / Write
Reset Value: 0000 0000 (00h)

7							0
ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

Bits 11:0 = **ATR2[11:0]** *Autoreload Register 2.*
This is a 12-bit register which is written by software. The ATR2 register value is automatically loaded into the upcounter CNTR2 when an overflow of CNTR2 occurs. The register value is used to set the PWM2/PWM3 frequency when ENCNTR2 is set.

DEAD TIME GENERATOR REGISTER (DTGR)

Read/Write
Reset Value: 0000 0000 (00h)

7							0
DTE	DT6	DT5	DT4	DT3	DT2	DT1	DT0

Bit 7 = **DTE** *Dead Time Enable*
This bit is read/write by software. It enables a dead time generation on PWM0/PWM1.
0: No Dead time insertion.
1: Dead time insertion enabled.

Bits 6:0 = **DT[6:0]** *Dead Time Value*

These bits are read/write by software. They define the dead time inserted between PWM0/PWM1. Dead time is calculated as follows:

Dead Time = DT[6:0] x Tcounter1

Note:

1. If DTE is set and DT[6:0]=0, PWM output signals will be at their reset state.

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
21	**ATCSR2**	FORCE2	FORCE1	ICS	OVFIE2	OVF2	ENCNTR2	TRAN2	TRAN1
	Reset Value	0	0	0	0	0	0	1	1
22	**BREAKCR**	BRSEL	BREDGE	BA	BPEN	PWM3	PWM2	PWM1	PWM0
	Reset Value	0	0	0	0	0	0	0	0
23	**ATR2H**	0	0	0	0	ATR11	ATR10	ATR9	ATR8
	Reset Value					0	0	0	0
24	**ATR2L**	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
	Reset Value	0	0	0	0	0	0	0	0
25	**DTGR**	DTE	DT6	DT5	DT4	DT3	DT2	DT1	DT0
	Reset Value	0	0	0	0	0	0	0	0
26	**BREAKEN**	0	0	0	0	0	0	BREN2	BREN1
	Reset Value							1	1

ANALOG COMPARATOR (Cont'd)

11.6.4 Register Description

Internal Voltage Reference Register (VREFCR)

Read/Write

Reset Value : 0000 0000 (00h)

7							0
VCEXT	VCBGR	VR3	VR2	VR1	VR0	0	0

Bit 7 = **VCEXT** *External Voltage Reference for Comparator*
This bit is set or cleared by software. It is used to connect the external reference voltage to the VN comparator input.
0: External reference voltage not connected to VN
1: External reference voltage connected to VN

Bit 6 = **VCBGR** *Bandgap Voltage for Comparator*
This bit is set or cleared by software. It is used to connect the bandgap voltage of 1.2V to the VN comparator input.
0: Bandgap voltage not connected to VN
1: Bandgap voltage connected to VN

Bits 5:2 = **VR[3:0]** *Programmable Internal Voltage Reference Range Selection*
These bits are set or cleared by software. They are used to select one of 16 different voltages available from the internal voltage reference module and connect it to comparator input VN.

Refer to Table 20.

Table 20. Voltage Reference Programming

VCEXT bit	VCBGR bit	VR3 bit	VR2 bit	VR1 bit	VR0 bit	VN Voltage
1	x	x	x	x	x	VEXT
0	1	x	x	x	x	1.2 bandgap
0	0	1	1	1	1	3.2V
0	0	1	1	1	0	3V
0	0	1	1	0	1	2.8V
0	0	1	1	0	0	2.6V
0	0	1	0	1	1	2.4V
0	0	1	0	1	0	2.2V
0	0	1	0	0	1	2V
0	0	1	0	0	0	1.8V
0	0	0	1	1	1	1.6V
0	0	0	1	1	0	1.4V
0	0	0	1	0	1	1.2V
0	0	0	1	0	0	1V
0	0	0	0	1	1	0.8V
0	0	0	0	1	0	0.6V
0	0	0	0	0	1	0.4V
0	0	0	0	0	0	0.2V

Bits 1:0 = Reserved, Must be kept cleared.

Comparator Control Register (CMPCR)

Read/Write

Reset Value : 1000 0000 (80h)

7							0
CHY-ST	0	CINV	CMPIF	CMPIE	CMP	COUT	CMPON

Bit 7= **CHYST** *Comparator Hysteresis Enable*

This bit is set or cleared by software and set by hardware reset. When this bit is set, the comparator hysteresis is enabled.
0: Hysteresis disabled
1: Hysteresis enabled
Note: To avoid spurious toggling of the output of the comparator due to noise on the voltage reference, it is recommended to enable the hysteresis.

Bit 6 = Reserved, Must be kept cleared

Bit 5 = **CINV** *Comparator Output Inversion Select*

This bit is set or cleared by software and cleared by hardware reset. When this bit is set, the comparator output is inverted.

If interrupt enable bit CMPIE is set in the CMPCR register, the CINV bit is also used to select which type of level transition on the comparator output will generate the interrupt. When this bit is reset, interrupt will be generated at the rising edge of the comparator output change (COMP signal, refer to Figure 62 on page 101). When this bit is set, interrupt will be generated at the falling edge of comparator output change (COMP signal, refer to Figure 62 on page 101).
0: Comparator output not inverted and interrupt generated at the rising edge of COMP
1: Comparator output inverted and interrupt generated at the falling edge of COMP

ANALOG COMPARATOR (Cont'd)

Bit 4 = **CMPIF** *Comparator Interrupt Flag*

This bit is set by hardware when interrupt is generated at the rising edge (CINV = 0) or falling edge (CINV = 1) of comparator output. This bit is cleared by reading the CMPCR register. Writing to this bit does not change the value.
0 : Comparator interrupt flag cleared
1 : Comparator interrupt flag set and can generate interrupt if CMPIE is set.

Bit 3 : **CMPIE** *Comparator Interrupt Enable*

This bit is set or reset by software and cleared by hardware reset. This bit enables or disables the interrupt generation depending on interrupt flag
0: Interrupt not generated
1: Interrupt generated if interrupt flag is set

Note:

This bit should be set to enable interrupt only after the comparator has been switched ON, i.e. when CMPON is set.

Once CMPON bit is set, it is recommended to wait the specified stabilization time before setting CMPIE bit in order to avoid a spurious interrupt (see section 13.12 on page 143).

Bit 2 : **CMP** *Comparator Output*

This bit is set or reset by software and cleared by hardware reset. It stores the value of comparator output.

Bit 1 = **COUT** *Comparator Output Enable on Port*
This bit is set or cleared by software. When this bit is set, the comparator output is available on PA7 port.
0 : Comparator output not connected to PA7
1 : Comparator output connected to PA7

Bit 0 : **CMPON** *Comparator ON/OFF*
This bit is set or cleared by software and reset by hardware reset. This bit is used to switch ON/OFF the comparator, internal voltage reference and current bias which provides 4µA current to both.
0: Comparator, Internal Voltage Reference, Bias OFF (in power-down state).
1: Comparator, Internal Voltage Reference, Bias ON

Note: For the comparator interrupt generation, it takes 250ns delay from comparator output change to rising or falling edge of interrupt generated.

Table 21. Analog Comparator Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Ch	**VREFCR**	VCEXT	VCBGR	VR3	VR2	VR1	VR0	-	-
	Reset Value	0	0	0	0	0	0	0	0
002Dh	**CMPCR**	CHYST	-	CINV	CMPIF	CMPIE	CMP	COUT	CMPON
	Reset value	1	0	0	0	0	0	0	0

INSTRUCTION GROUPS (cont'd)

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
ADC	Add with Carry	A = A + M + C	A	M	H		N	Z	C
ADD	Addition	A = A + M	A	M	H		N	Z	C
AND	Logical And	A = A . M	A	M			N	Z	
BCP	Bit compare A, Memory	tst (A . M)	A	M			N	Z	
BRES	Bit Reset	bres Byte, #3	M						
BSET	Bit Set	bset Byte, #3	M						
BTJF	Jump if bit is false (0)	btjf Byte, #3, Jmp1	M						C
BTJT	Jump if bit is true (1)	btjt Byte, #3, Jmp1	M						C
CALL	Call subroutine								
CALLR	Call subroutine relative								
CLR	Clear		reg, M				0	1	
CP	Arithmetic Compare	tst(Reg - M)	reg	M			N	Z	C
CPL	One Complement	A = FFH-A	reg, M				N	Z	1
DEC	Decrement	dec Y	reg, M				N	Z	
HALT	Halt					0			
IRET	Interrupt routine return	Pop CC, A, X, PC			H	I	N	Z	C
INC	Increment	inc X	reg, M				N	Z	
JP	Absolute Jump	jp [TBL.w]							
JRA	Jump relative always								
JRT	Jump relative								
JRF	Never jump	jrf *							
JRIH	Jump if ext. interrupt = 1								
JRIL	Jump if ext. interrupt = 0								
JRH	Jump if H = 1	H = 1 ?							
JRNH	Jump if H = 0	H = 0 ?							
JRM	Jump if I = 1	I = 1 ?							
JRNM	Jump if I = 0	I = 0 ?							
JRMI	Jump if N = 1 (minus)	N = 1 ?							
JRPL	Jump if N = 0 (plus)	N = 0 ?							
JREQ	Jump if Z = 1 (equal)	Z = 1 ?							
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?							
JRC	Jump if C = 1	C = 1 ?							
JRNC	Jump if C = 0	C = 0 ?							
JRULT	Jump if C = 1	Unsigned <							
JRUGE	Jump if C = 0	Jmp if unsigned >=							
JRUGT	Jump if (C + Z = 0)	Unsigned >							

INSTRUCTION GROUPS (cont'd)

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
JRULE	Jump if (C + Z = 1)	Unsigned <=							
LD	Load	dst <= src	reg, M	M, reg			N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0				0
NEG	Negate (2's compl)	neg $10	reg, M				N	Z	C
NOP	No Operation								
OR	OR operation	A = A + M	A	M			N	Z	
POP	Pop from the Stack	pop reg	reg	M					
		pop CC	CC	M	H	I	N	Z	C
PUSH	Push onto the Stack	push Y	M	reg, CC					
RCF	Reset carry flag	C = 0							0
RET	Subroutine Return								
RIM	Enable Interrupts	I = 0				0			
RLC	Rotate left true C	C <= Dst <= C	reg, M				N	Z	C
RRC	Rotate right true C	C => Dst => C	reg, M				N	Z	C
RSP	Reset Stack Pointer	S = Max allowed							
SBC	Subtract with Carry	A = A - M - C	A	M			N	Z	C
SCF	Set carry flag	C = 1							1
SIM	Disable Interrupts	I = 1				1			
SLA	Shift left Arithmetic	C <= Dst <= 0	reg, M				N	Z	C
SLL	Shift left Logic	C <= Dst <= 0	reg, M				N	Z	C
SRL	Shift right Logic	0 => Dst => C	reg, M				0	Z	C
SRA	Shift right Arithmetic	Dst7 => Dst => C	reg, M				N	Z	C
SUB	Subtraction	A = A - M	A	M			N	Z	C
SWAP	SWAP nibbles	Dst[7..4] <=> Dst[3..0]	reg, M				N	Z	
TNZ	Test for Neg & Zero	tnz lbl1					N	Z	
TRAP	S/W trap	S/W interrupt				1			
WFI	Wait for Interrupt					0			
XOR	Exclusive OR	A = A XOR M	A	M			N	Z	

13 ELECTRICAL CHARACTERISTICS

13.1 PARAMETER CONDITIONS

Unless otherwise specified, all voltages are referred to V_{SS}.

13.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

13.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, V_{DD}=5V (for the 4.5V≤V_{DD}≤5.5V voltage range) and V_{DD}=3.3V (for the 3V≤V_{DD}≤3.6V voltage range). They are given only as design guidelines and are not tested.

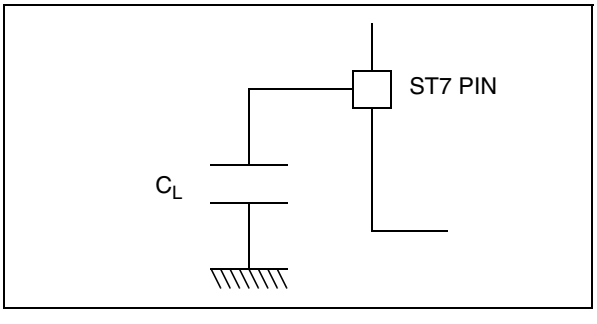
13.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

13.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 63.

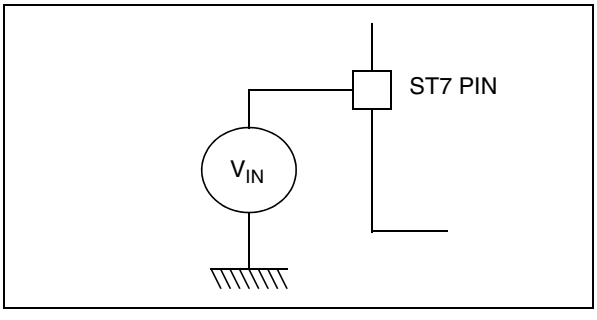
Figure 63. Pin loading conditions



13.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 64.

Figure 64. Pin input voltage



13.3 OPERATING CONDITIONS

13.3.1 General Operating Conditions: Suffix 6 Devices

T_A = -40 to +85°C unless otherwise specified.

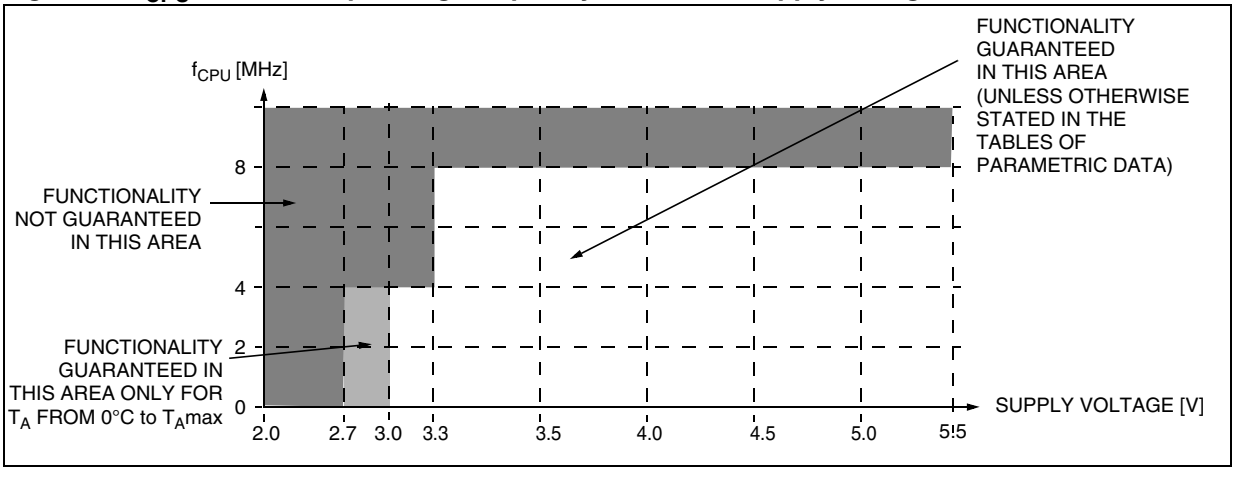
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	f_{CPU} = 4 MHz. max., T_A = 0 to 85°C	2.7	5.5	V
		f_{CPU} = 4 MHz. max.,T_A = -40 to 85°C	3.0	5.5	
		f_{CPU} = 8 MHz. max.	3.3	5.5	
f_{CPU}	CPU clock frequency	$V_{DD} \geq 3.3V$	up to 8		MHz
		$2.7V \leq V_{DD} < 3.3V$	up to 4		

13.3.2 General Operating Conditions: Suffix 3 Devices

T_A = -40 to +125°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	f_{CPU} = 4 MHz. max., T_A = 0 to 125°C	2.7	5.5	V
		f_{CPU} = 4 MHz. max.,T_A = -40 to 125°C	3.0	5.5	
		f_{CPU} = 8 MHz. max.	3.3	5.5	
f_{CPU}	CPU clock frequency	$V_{DD} \geq 3.3V$	up to 8		MHz
		$2.7V \leq V_{DD} < 3.3V$	up to 4		

Figure 65. f_{CPU} Maximum Operating Frequency Versus V_{DD} Supply Voltage



OPERATING CONDITIONS (Cont'd)

Figure 68. Typical accuracy with RCCR=RCCR1 vs V_{DD}= 3-3.6V and Temperature

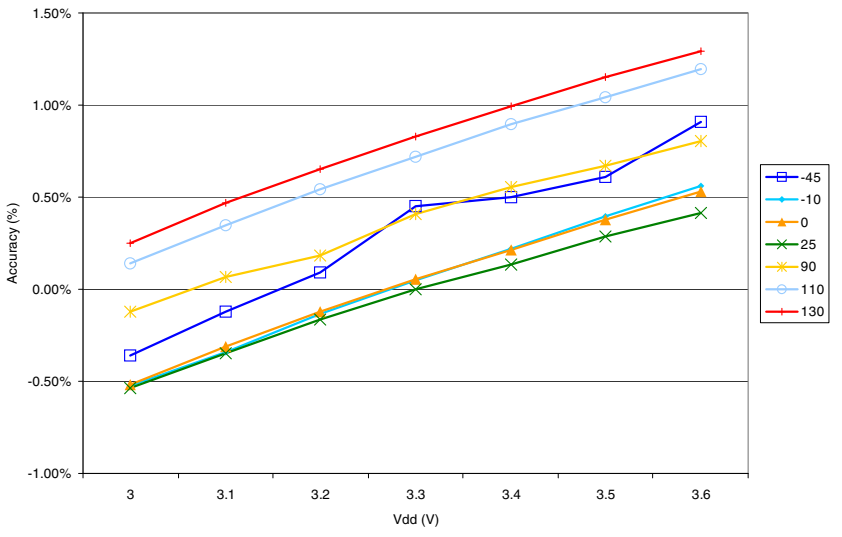
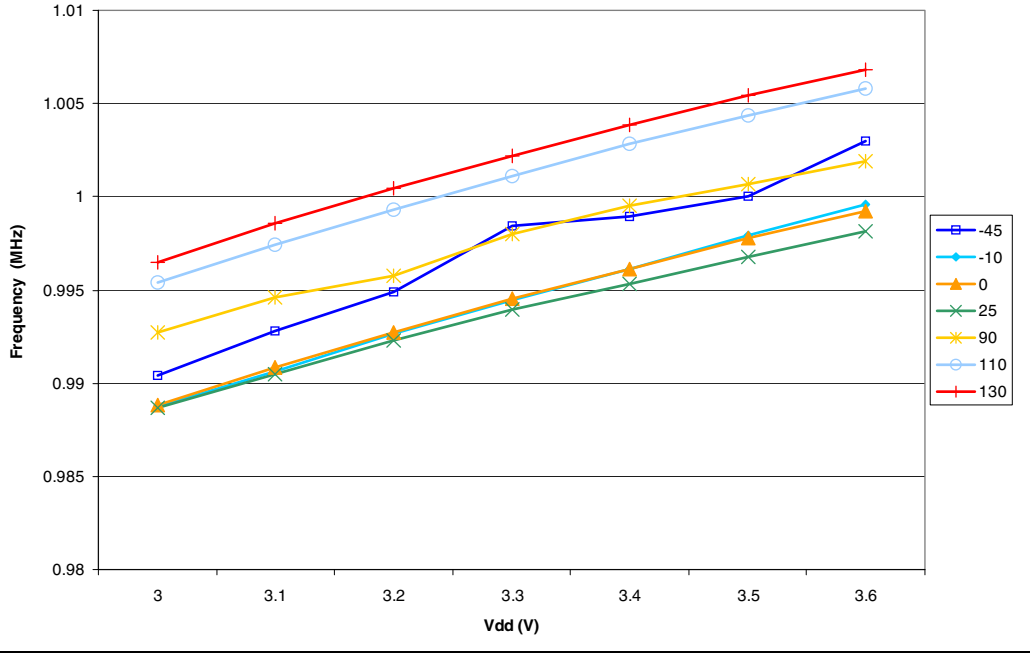


Figure 69. Typical RCCR1 vs V_{DD} and Temperature



13.9 CONTROL PIN CHARACTERISTICS

13.9.1 Asynchronous $\overline{\text{RESET}}$ Pin

T_A = -40°C to 125°C, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage [1]			V_{ss} - 0.3		0.3xV_{DD}	V
V_{IH}	Input high level voltage [1]			0.7xV_{DD}		V_{DD} + 0.3	
V_{hys}	Schmitt trigger voltage hysteresis [1]				2		V
V_{OL}	Output low level voltage [1][2]	V_{DD}=5V	I_{IO}=+5mA $T_A \leq 85°C$		0.5	1.0	V
			I_{IO}=+2mA $T_A \leq 85°C$		0.2	0.4	
R_{ON}	Pull-up equivalent resistor [3]	V_{DD}=5V		20	40	80	kΩ
		V_{DD}=3V [1]		40	70	120	
$t_{w(RSTL)out}$	Generated reset pulse duration	Internal reset sources			30		µs
$t_{h(RSTL)in}$	External reset pulse hold time [4]			20			µs
$t_{g(RSTL)in}$	Filtered glitch duration				200		ns

Notes:

1. Data based on characterization results, not tested in production.

2. The I_{IO} current sunk must always respect the absolute maximum rating specified in Section 13.2.2 and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.

3. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. Specified for voltages on $\overline{\text{RESET}}$ pin between V_{ILmax} and V_{DD}

4. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.

Table 29. ST7 Application Notes

IDENTIFICATION	DESCRIPTION
AN1947	ST7MC PMAC SINE WAVE MOTOR CONTROL SOFTWARE LIBRARY
GENERAL PURPOSE	
AN1476	LOW COST POWER SUPPLY FOR HOME APPLIANCES
AN1526	ST7FLITE0 QUICK REFERENCE NOTE
AN1709	EMC DESIGN FOR ST MICROCONTROLLERS
AN1752	ST72324 QUICK REFERENCE NOTE
PRODUCT EVALUATION	
AN 910	PERFORMANCE BENCHMARKING
AN 990	ST7 BENEFITS VERSUS INDUSTRY STANDARD
AN1077	OVERVIEW OF ENHANCED CAN CONTROLLERS FOR ST7 AND ST9 MCUS
AN1086	U435 CAN-DO SOLUTIONS FOR CAR MULTIPLEXING
AN1103	IMPROVED B-EMF DETECTION FOR LOW SPEED, LOW VOLTAGE WITH ST72141
AN1150	BENCHMARK ST72 VS PC16
AN1151	PERFORMANCE COMPARISON BETWEEN ST72254 & PC16F876
AN1278	LIN (LOCAL INTERCONNECT NETWORK) SOLUTIONS
PRODUCT MIGRATION	
AN1131	MIGRATING APPLICATIONS FROM ST72511/311/214/124 TO ST72521/321/324
AN1322	MIGRATING AN APPLICATION FROM ST7263 REV.B TO ST7263B
AN1365	GUIDELINES FOR MIGRATING ST72C254 APPLICATIONS TO ST72F264
AN1604	HOW TO USE ST7MDT1-TRAIN WITH ST72F264
AN2200	GUIDELINES FOR MIGRATING ST7LITE1X APPLICATIONS TO ST7FLITE1XB
PRODUCT OPTIMIZATION	
AN 982	USING ST7 WITH CERAMIC RESONATOR
AN1014	HOW TO MINIMIZE THE ST7 POWER CONSUMPTION
AN1015	SOFTWARE TECHNIQUES FOR IMPROVING MICROCONTROLLER EMC PERFORMANCE
AN1040	MONITORING THE VBUS SIGNAL FOR USB SELF-POWERED DEVICES
AN1070	ST7 CHECKSUM SELF-CHECKING CAPABILITY
AN1181	ELECTROSTATIC DISCHARGE SENSITIVE MEASUREMENT
AN1324	CALIBRATING THE RC OSCILLATOR OF THE ST7FLITE0 MCU USING THE MAINS
AN1502	EMULATED DATA EEPROM WITH ST7 HDFLASH MEMORY
AN1529	EXTENDING THE CURRENT & VOLTAGE CAPABILITY ON THE ST7265 VDDF SUPPLY
AN1530	ACCURATE TIMEBASE FOR LOW-COST ST7 APPLICATIONS WITH INTERNAL RC OSCILLATOR
AN1605	USING AN ACTIVE RC TO WAKEUP THE ST7LITE0 FROM POWER SAVING MODE
AN1636	UNDERSTANDING AND MINIMIZING ADC CONVERSION ERRORS
AN1828	PIR (PASSIVE INFRARED) DETECTOR USING THE ST7FLITE05/09/SUPERLITE
AN1946	SENSORLESS BLDC MOTOR CONTROL AND BEMF SAMPLING METHODS WITH ST7MC
AN1953	PFC FOR ST7MC STARTER KIT
AN1971	ST7LITE0 MICROCONTROLLED BALLAST
PROGRAMMING AND TOOLS	
AN 978	ST7 VISUAL DEVELOP SOFTWARE KEY DEBUGGING FEATURES
AN 983	KEY FEATURES OF THE COSMIC ST7 C-COMPILER PACKAGE
AN 985	EXECUTING CODE IN ST7 RAM
AN 986	USING THE INDIRECT ADDRESSING MODE WITH ST7
AN 987	ST7 SERIAL TEST CONTROLLER PROGRAMMING
AN 988	STARTING WITH ST7 ASSEMBLY TOOL CHAIN
AN 989	GETTING STARTED WITH THE ST7 HIWARE C TOOLCHAIN

Date	Revision	Main changes
27-Nov-06	4	Added QFN20 pinout with new mechanical data (Figure 3 on page 5 and Figure 117 on page 145) Added ST7FLI19BY1M3TR sales type in Table 1, “Supported Flash part numbers,” Modifed “DEVELOPMENT TOOLS” on page 153
23-April-07	5	Added note 1 to Table 1 on page 7 Modified note 1 in section 7.1 on page 23 Added caution to section 7.5.1 on page 28 Modified section 11.2.3.6 on page 67 Modified title of Figure 48 on page 68 and added note 1 Modified Figure 49 on page 69 Modified section 11.5.3.4 on page 97 and added section 11.5.3.5 on page 97 Modified EOC bit description in section 11.5.6 on page 98 Modified V_{FFTB} parameter in section 13.7.1 on page 127 Modified Table 28 on page 153
17-June-08	6	Modified first page Added note 2 in Table 1, “Device Pin Description,” on page 7 Modified WDGRF bit description in section 7.6.4 on page 35 Modified note 1 in section 11.2.3.6 on page 67 Added section 13.3.6 on page 120 Modified CLKSEL option bits description in section 15.1 on page 149 Modified section 15.2 on page 151 and option list