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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

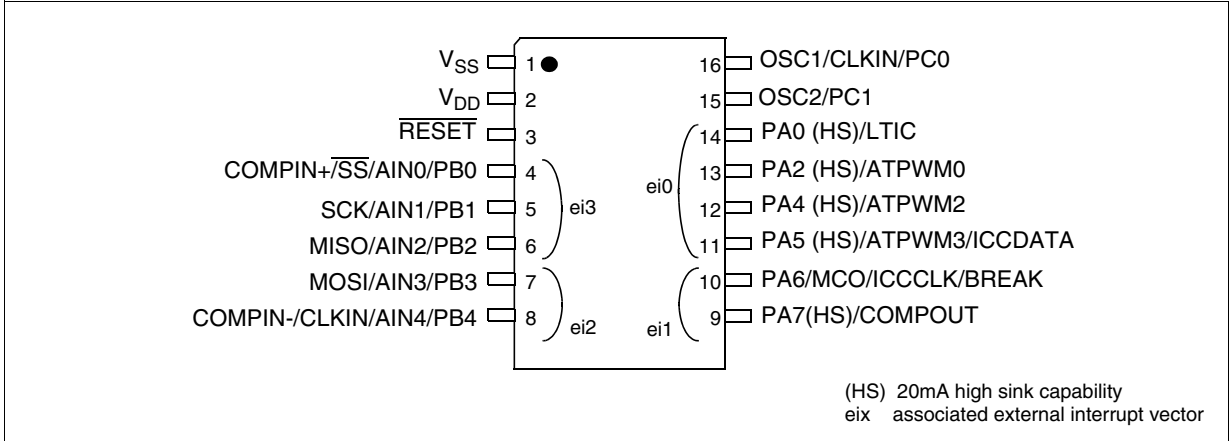
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Not For New Designs
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/st7flit19bf0m6">https://www.e-xfl.com/product-detail/stmicroelectronics/st7flit19bf0m6</a>

PIN DESCRIPTION (Cont'd)

Figure 4. 16-Pin SO and DIP Package Pinout



Pin No.			Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function	
SO20/DPI20	QFN20	SO16/DIP16			Input	Output	Input				Output				
							float	wpu	int	ana	OD	PP			
12	10	10	PA6 /MCO/ ICCCLK/BREAK	I/O	C <sub>T</sub>		X	ei1				X	X	Port A6	Main Clock Output or In Circuit Communication Clock or External BREAK  <b>Caution:</b> During normal operation this pin must be pulled- up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up
13	11	11	PA5 /ICCDATA/ ATPWM3	I/O	C <sub>T</sub>	HS	X	ei1			X	X	Port A5		In Circuit Communication Data or Auto-Reload Timer PWM3
14	12	12	PA4/ATPWM2	I/O	C <sub>T</sub>	HS	X				X	X	Port A4	Auto-Reload Timer PWM2	
15	13	-	PA3/ATPWM1	I/O	C <sub>T</sub>	HS	X				X	X	Port A3	Auto-Reload Timer PWM1	
16	14	13	PA2/ATPWM0	I/O	C <sub>T</sub>	HS	X				X	X	Port A2	Auto-Reload Timer PWM0	
17	15	-	PA1/ATIC	I/O	C <sub>T</sub>	HS	X				X	X	Port A1	Auto-Reload Timer Input Capture	
18	16	14	PA0/LTIC	I/O	C <sub>T</sub>	HS	X				X	X	Port A0	Lite Timer Input Capture	
19	17	15	OSC2/PC1	I/O			X					X	Port C1 <sup>3)</sup>	Resonator oscillator inverter output	
20	18	16	OSC1/CLKIN/PC0	I/O			X					X	Port C0 <sup>3)</sup>	Resonator oscillator inverter input or External clock input	

**Notes:**

1. It is mandatory to connect all available V<sub>DD</sub> and V<sub>DDA</sub> pins to the supply voltage and all V<sub>SS</sub> and V<sub>SSA</sub> pins to ground.
2. When the pin is configured as analog input, positive and negative current injections are not allowed.
3. PCOR not implemented but p-transistor always active in output mode (refer to Figure 32 on page 50).

## FLASH PROGRAM MEMORY (Cont'd)

## 4.4 ICC interface

ICP needs a minimum of 4 and up to 6 pins to be connected to the programming tool. These pins are:

- $\overline{\text{RESET}}$ : device reset
- $V_{SS}$ : device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input serial data pin
- OSC1: main clock input for external source (not required on devices without OSC1/OSC2 pins)
- $V_{DD}$ : application board power supply (optional, see Note 3)

**Notes:**

1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2. During the ICP session, the programming tool must control the  $\overline{\text{RESET}}$  pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor < 1K). A schottky diode can be used to isolate the application  $\overline{\text{RESET}}$  circuit in this case. When using a

classical RC network with  $R > 1K$  or a reset management IC with open drain output and pull-up resistor > 1K, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

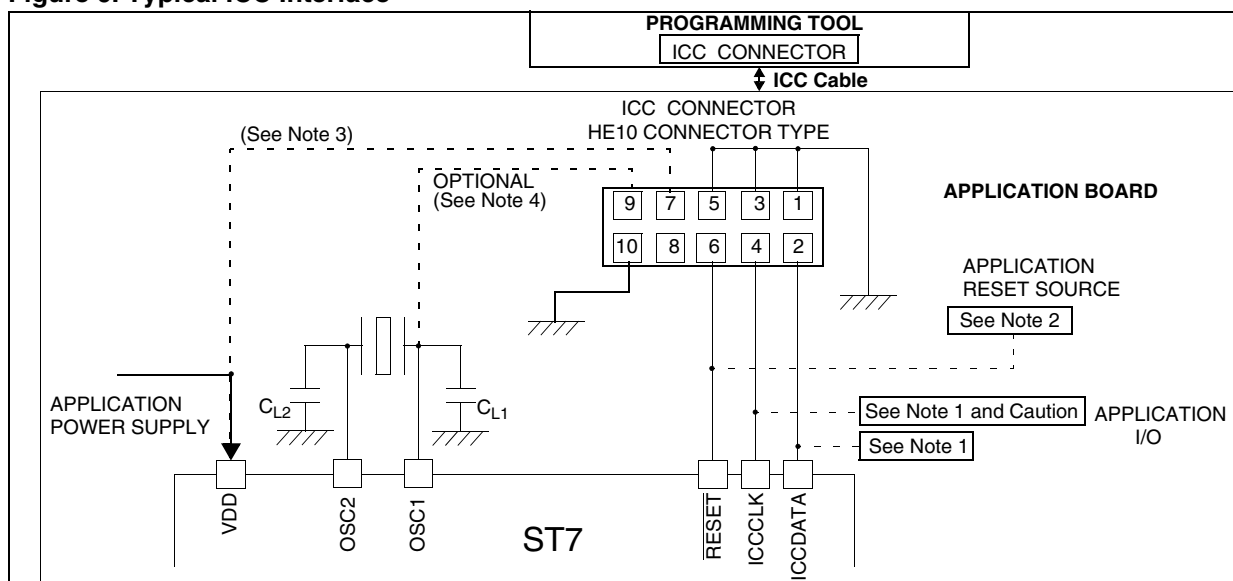
3. The use of pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4. Pin 9 has to be connected to the OSC1 pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC2 grounded in this case.

5. In 38-pulse ICC mode, the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. For ST7LITE10B devices which do not support the internal RC oscillator, the "option byte disabled" mode must be used (35-pulse ICC mode entry, clock provided by the tool).

**Caution:** During normal operation the ICCCLK pin must be pulled-up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

**Figure 6. Typical ICC Interface**



## DATA EEPROM (Cont'd)

## 5.3 MEMORY ACCESS

The Data EEPROM memory read/write access modes are controlled by the E2LAT bit of the EEPROM Control/Status register (EECSR). The flowchart in Figure 8 describes these different memory access modes.

**Read Operation (E2LAT=0)**

The EEPROM can be read as a normal ROM location when the E2LAT bit of the EECSR register is cleared.

On this device, Data EEPROM can also be used to execute machine code. Take care not to write to the Data EEPROM while executing from it. This would result in an unexpected code being executed.

**Write Operation (E2LAT=1)**

To access the write mode, the E2LAT bit has to be set by software (the E2PGM bit remains cleared). When a write access to the EEPROM area occurs,

the value is latched inside the 32 data latches according to its address.

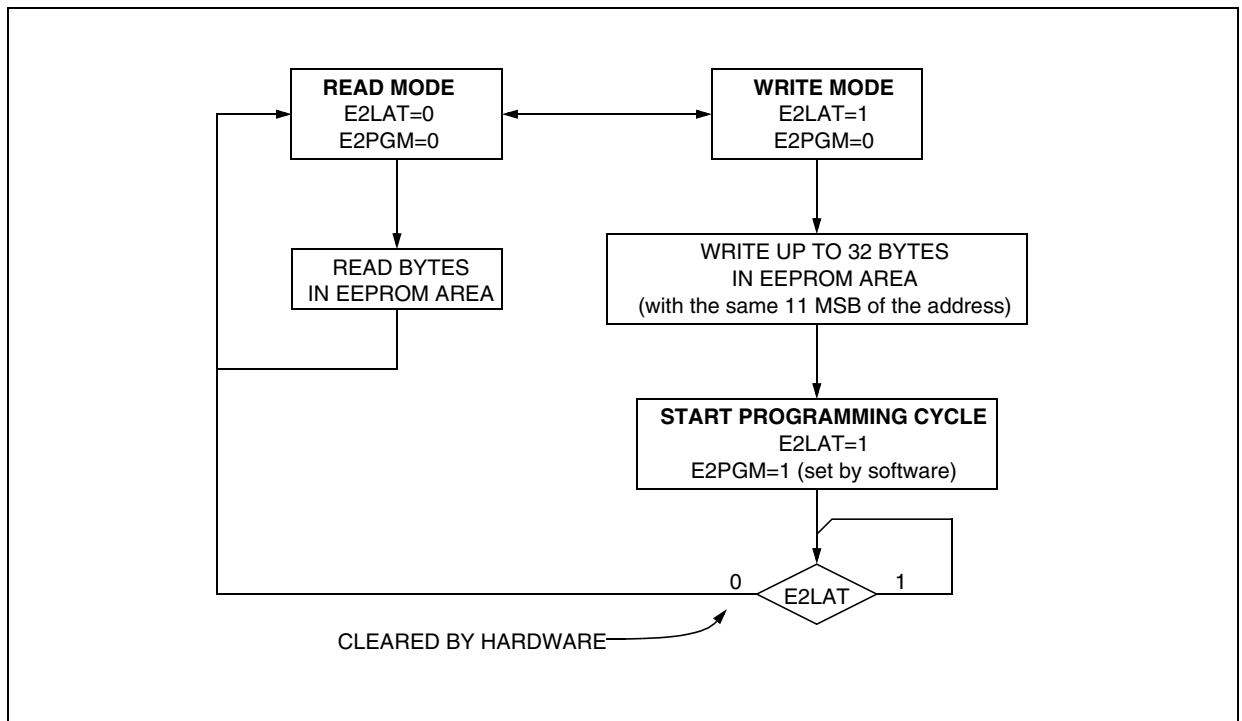
When PGM bit is set by the software, all the previous bytes written in the data latches (up to 32) are programmed in the EEPROM cells. The effective high address (row) is determined by the last EEPROM write sequence. To avoid wrong programming, the user must take care that all the bytes written between two programming sequences have the same high address: only the five Least Significant Bits of the address can change.

At the end of the programming cycle, the PGM and LAT bits are cleared simultaneously.

**Note:** Care should be taken during the programming cycle. Writing to the same memory location will over-program the memory (logical AND between the two write access data result) because the data latches are only cleared at the end of the programming cycle and by the falling edge of the E2LAT bit.

It is not possible to read the latched data. This note is illustrated by the Figure 10.

**Figure 8. Data EEPROM Programming Flowchart**



**CPU REGISTERS** (cont'd)**CONDITION CODE REGISTER (CC)**

Read/Write

Reset Value: 111x1xxx

7							0
1	1	1	H	I	N	Z	C

The 8-bit Condition Code register contains the interrupt mask and four flags representative of the result of the instruction just executed. This register can also be handled by the PUSH and POP instructions.

These bits can be individually tested and/or controlled by specific instructions.

**Bit 4 = H Half carry**

This bit is set by hardware when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. It is reset by hardware during the same instructions.

0: No half carry has occurred.

1: A half carry has occurred.

This bit is tested using the JRH or JRNH instruction. The H bit is useful in BCD arithmetic subroutines.

**Bit 3 = I Interrupt mask**

This bit is set by hardware when entering in interrupt or by software to disable all interrupts except the TRAP software interrupt. This bit is cleared by software.

0: Interrupts are enabled.

1: Interrupts are disabled.

This bit is controlled by the RIM, SIM and IRET instructions and is tested by the JRM and JRNM instructions.

**Note:** Interrupts requested while I is set are latched and can be processed when I is cleared. By default an interrupt routine is not interruptible

because the I bit is set by hardware at the start of the routine and reset by the IRET instruction at the end of the routine. If the I bit is cleared by software in the interrupt routine, pending interrupts are serviced regardless of the priority level of the current interrupt routine.

**Bit 2 = N Negative**

This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It is a copy of the 7<sup>th</sup> bit of the result.

0: The result of the last operation is positive or null.

1: The result of the last operation is negative (that is, the most significant bit is a logic 1).

This bit is accessed by the JRMI and JRPL instructions.

**Bit 1 = Z Zero**

This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

0: The result of the last operation is different from zero.

1: The result of the last operation is zero.

This bit is accessed by the JREQ and JRNE test instructions.

**Bit 0 = C Carry/borrow**

This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.

0: No overflow or underflow has occurred.

1: An overflow or underflow has occurred.

This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the "bit test and branch", shift and rotate instructions.

## 8 INTERRUPTS

The ST7 core may be interrupted by one of two different methods: Maskable hardware interrupts as listed in the “interrupt mapping” table and a non-maskable software interrupt (TRAP). The Interrupt processing flowchart is shown in Figure 1.

The maskable interrupts must be enabled by clearing the I bit in order to be serviced. However, disabled interrupts may be latched and processed when they are enabled (see external interrupts subsection).

**Note:** After reset, all interrupts are disabled.

When an interrupt has to be serviced:

- Normal processing is suspended at the end of the current instruction execution.
- The PC, X, A and CC registers are saved onto the stack.
- The I bit of the CC register is set to prevent additional interrupts.
- The PC is then loaded with the interrupt vector of the interrupt to service and the first instruction of the interrupt service routine is fetched (refer to the Interrupt Mapping table for vector addresses).

The interrupt service routine should finish with the IRET instruction which causes the contents of the saved registers to be recovered from the stack.

**Note:** As a consequence of the IRET instruction, the I bit is cleared and the main program resumes.

### Priority Management

By default, a servicing interrupt cannot be interrupted because the I bit is set by hardware entering in interrupt routine.

In the case when several interrupts are simultaneously pending, an hardware priority defines which one will be serviced first (see the Interrupt Mapping table).

### Interrupts and Low Power Mode

All interrupts allow the processor to leave the WAIT low power mode. Only external and specifically mentioned interrupts allow the processor to leave the HALT low power mode (refer to the “Exit from HALT” column in the Interrupt Mapping table).

### 8.1 NON MASKABLE SOFTWARE INTERRUPT

This interrupt is entered when the TRAP instruction is executed regardless of the state of the I bit. It is serviced according to the flowchart in Figure 1.

### 8.2 EXTERNAL INTERRUPTS

External interrupt vectors can be loaded into the PC register if the corresponding external interrupt occurred and if the I bit is cleared. These interrupts allow the processor to leave the HALT low power mode.

The external interrupt polarity is selected through the miscellaneous register or interrupt register (if available).

An external interrupt triggered on edge will be latched and the interrupt request automatically cleared upon entering the interrupt service routine.

**Caution:** The type of sensitivity defined in the Miscellaneous or Interrupt register (if available) applies to the ei source. In case of a NAnDED source (as described in the I/O ports section), a low level on an I/O pin, configured as input with interrupt, masks the interrupt request even in case of rising-edge sensitivity.

### 8.3 PERIPHERAL INTERRUPTS

Different peripheral interrupt flags in the status register are able to cause an interrupt when they are active if both:

- The I bit of the CC register is cleared.
- The corresponding enable bit is set in the control register.

If any of these two conditions is false, the interrupt is latched and thus remains pending.

Clearing an interrupt request is done by:

- Writing “0” to the corresponding bit in the status register or
- Access to the status register while the flag is set followed by a read or write of an associated register.

**Note:** The clearing sequence resets the internal latch. A pending interrupt (that is, waiting for being enabled) will therefore be lost if the clear sequence is executed.

I/O PORTS (Cont'd)

Figure 32. I/O Port General Block Diagram

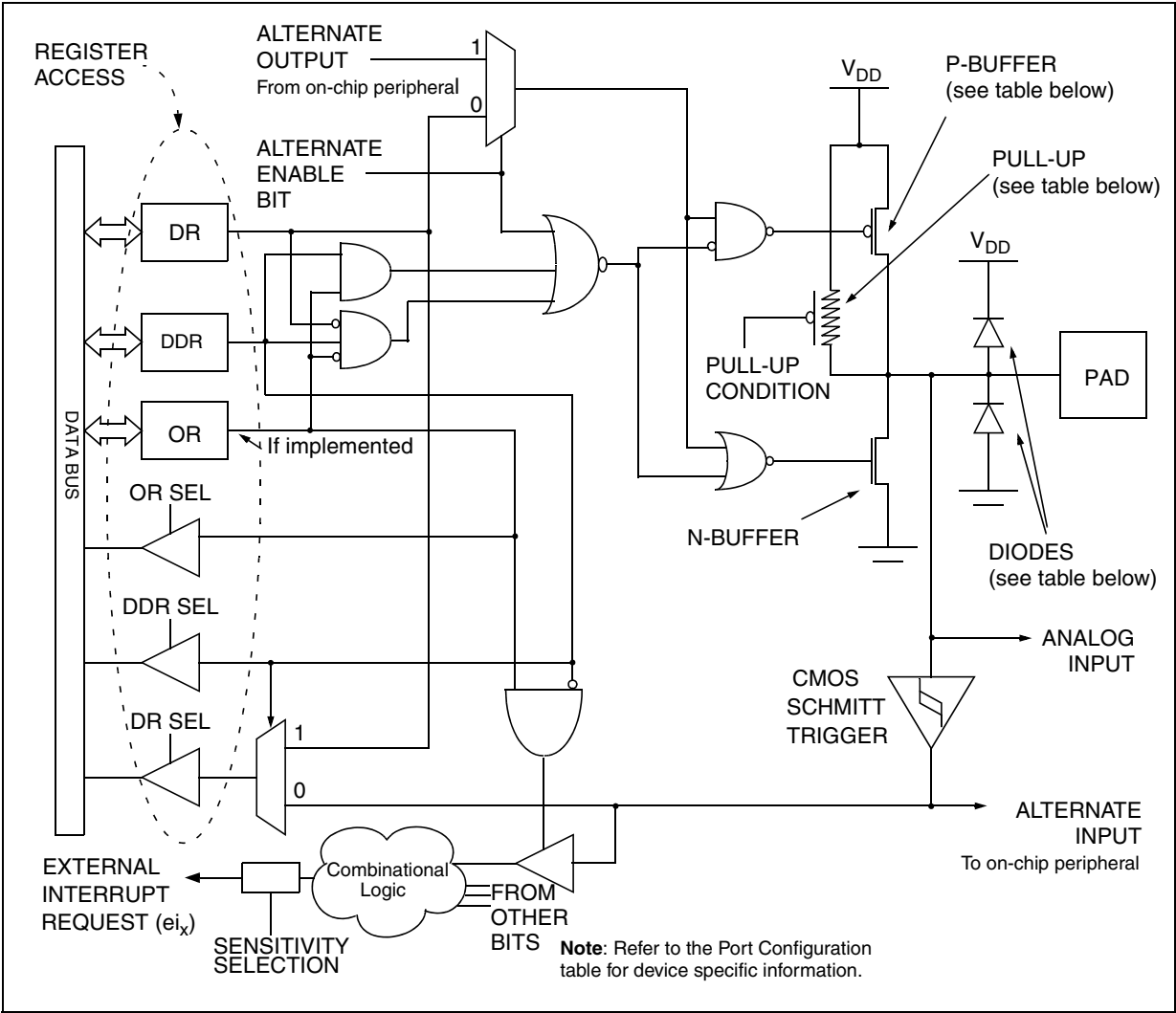


Table 8. I/O Port Mode Options

Configuration Mode		Pull-Up	P-Buffer	Diodes	
				to V <sub>DD</sub>	to V <sub>SS</sub>
Input	Floating with/without Interrupt	Off	Off	On	On
	Pull-up with/without Interrupt	On			
Output	Push-pull	Off	On		
	Open Drain (logic level)		Off		

**Legend:** Off - implemented not activated  
On - implemented and activated



## I/O PORTS (Cont'd)

## 10.7 DEVICE-SPECIFIC I/O PORT CONFIGURATION

The I/O port register configurations are summarised as follows.

## Standard Ports

## PA7:0, PB6:0

MODE	DDR	OR
floating input	0	0
pull-up input	0	1
open drain output	1	0
push-pull output	1	1

## Interrupt Ports

Ports where the external interrupt capability is selected using the EISR register

MODE	DDR	OR
floating input	0	0
pull-up interrupt input	0	1
open drain output	1	0
push-pull output	1	1

## PC1:0 (multiplexed with OSC1,OSC2)

MODE	DDR
floating input	0
push-pull output	1

The selection between OSC1 or PC0 and OSC2 or PC1 is done by option byte. Refer to section 15.1 on page 149. Interrupt capability is not available on PC1:0.

**Note:** PCOR not implemented but p-transistor always active in output mode (refer to Figure 32 on page 50)

Table 10. Port Configuration (Standard ports)

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	floating	pull-up	open drain	push-pull
Port B	PB6:0	floating	pull-up	open drain	push-pull

**Note:** On ports where the external interrupt capability is selected using the EISR register, the configuration will be as follows:

Port	Pin name	Input		Output	
		OR = 0	OR = 1	OR = 0	OR = 1
Port A	PA7:0	floating	pull-up interrupt	open drain	push-pull
Port B	PB6:0	floating	pull-up interrupt	open drain	push-pull

Table 11. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0000h	PADR Reset Value	MSB 1	1	1	1	1	1	1	LSB 1
0001h	PADDR Reset Value	MSB 0	0	0	0	0	0	0	LSB 0

**DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)****11.2.3.4 Output Compare Mode**

To use this function, load a 12-bit value in the Preload DCRxH and DCRxL registers.

When the 12-bit upcounter CNTR1 reaches the value stored in the Active DCRxH and DCRxL registers, the CMPF<sub>x</sub> bit in the PWMxCSR register is set and an interrupt request is generated if the CMPIE bit is set.

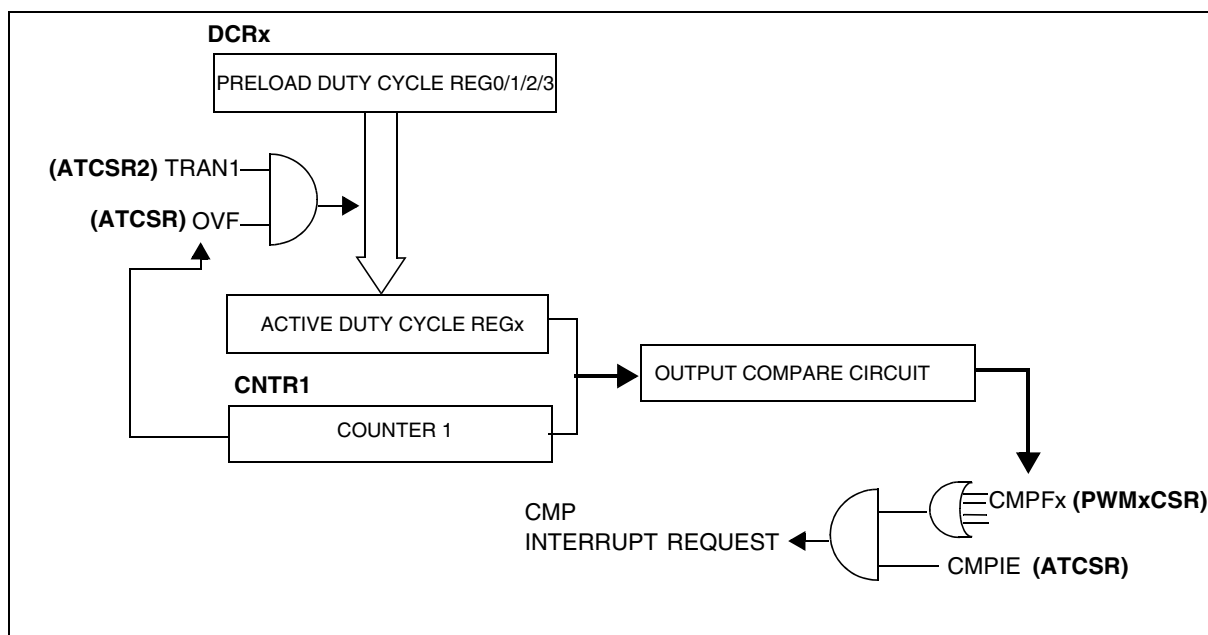
In single Timer mode the output compare function is performed only on CNTR1. The difference between both the modes is that, in Single Timer mode, CNTR1 can be compared with any of the four DCR registers, and in Dual Timer mode,

CNTR1 is compared with DCR0 or DCR1 and CNTR2 is compared with DCR2 or DCR3.

**Notes:**

1. The output compare function is only available for DCR<sub>x</sub> values other than 0 (reset value).
2. Duty cycle registers are buffered internally. The CPU writes in Preload Duty Cycle Registers and these values are transferred in Active Duty Cycle Registers after an overflow event if the corresponding transfer bit (TRAN<sub>x</sub> bit) is set. Output compare is done by comparing these active DCR<sub>x</sub> values with the counters.

**Figure 42. Block Diagram of Output Compare Mode (single timer)**



## DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

### 11.2.4 Low Power Modes

Mode	Description
WAIT	No effect on AT timer
HALT	AT timer halted.

### 11.2.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt	Exit from Active-Halt
Overflow Event	OVF1	OVIE1	Yes	No	Yes
AT4 IC Event	ICF	ICIE	Yes	No	No
CMP Event	CMPPFx	CMPIE	Yes	No	No
Overflow Event2	OVF2	OVIE2	Yes	No	No

**Note:** The CMP and AT4 IC events are connected to the same interrupt vector.  
The OVF event is mapped on a separate vector (see Interrupts chapter).

They generate an interrupt if the enable bit is set in the ATCSR register and the interrupt mask in the CC register is reset (RIM instruction).

## ON-CHIP PERIPHERALS (cont'd)

## 11.4 SERIAL PERIPHERAL INTERFACE (SPI)

## 11.4.1 Introduction

The Serial Peripheral Interface (SPI) allows full-duplex, synchronous, serial communication with external devices. An SPI system may consist of a master and one or more slaves or a system in which devices may be either masters or slaves.

## 11.4.2 Main Features

- Full duplex synchronous transfers (on three lines)
- Simplex synchronous transfers (on two lines)
- Master or slave operation
- 6 master mode frequencies ( $f_{CPU}/4$  max.)
- $f_{CPU}/2$  max. slave mode frequency (see note)
- $\overline{SS}$  Management by software or hardware
- Programmable clock polarity and phase
- End of transfer interrupt flag
- Write collision, Master Mode Fault and Overrun flags

**Note:** In slave mode, continuous transmission is not possible at maximum frequency due to the software overhead for clearing status flags and to initiate the next transmission sequence.

## 11.4.3 General Description

Figure 1 on page 3 shows the serial peripheral interface (SPI) block diagram. There are three registers:

- SPI Control Register (SPICR)
- SPI Control/Status Register (SPICSR)
- SPI Data Register (SPIDR)

The SPI is connected to external devices through four pins:

- MISO: Master In / Slave Out data
- MOSI: Master Out / Slave In data
- SCK: Serial Clock out by SPI masters and input by SPI slaves
- $\overline{SS}$ : Slave select:

This input signal acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave  $\overline{SS}$  inputs can be driven by standard I/O ports on the master Device.

**SERIAL PERIPHERAL INTERFACE (cont'd)****11.4.5 Error Flags****11.4.5.1 Master Mode Fault (MODF)**

Master mode fault occurs when the master device's  $\overline{SS}$  pin is pulled low.

When a Master mode fault occurs:

- The MODF bit is set and an SPI interrupt request is generated if the SPIE bit is set.
- The SPE bit is reset. This blocks all output from the device and disables the SPI peripheral.
- The MSTR bit is reset, thus forcing the device into slave mode.

Clearing the MODF bit is done through a software sequence:

1. A read access to the SPICSR register while the MODF bit is set.
2. A write to the SPICR register.

**Notes:** To avoid any conflicts in an application with multiple slaves, the  $\overline{SS}$  pin must be pulled high during the MODF bit clearing sequence. The SPE and MSTR bits may be restored to their original state during or after this clearing sequence.

Hardware does not allow the user to set the SPE and MSTR bits while the MODF bit is set except in the MODF bit clearing sequence.

In a slave device, the MODF bit can not be set, but in a multimaster configuration the device can be in slave mode with the MODF bit set.

The MODF bit indicates that there might have been a multimaster conflict and allows software to handle this using an interrupt routine and either perform a reset or return to an application default state.

**11.4.5.2 Overrun Condition (OVR)**

An overrun condition occurs when the master device has sent a data byte and the slave device has not cleared the SPIF bit issued from the previously transmitted byte.

When an Overrun occurs:

- The OVR bit is set and an interrupt request is generated if the SPIE bit is set.

In this case, the receiver buffer contains the byte sent after the SPIF bit was last cleared. A read to the SPIDR register returns this byte. All other bytes are lost.

The OVR bit is cleared by reading the SPICSR register.

**11.4.5.3 Write Collision Error (WCOL)**

A write collision occurs when the software tries to write to the SPIDR register while a data transfer is taking place with an external device. When this happens, the transfer continues uninterrupted and the software write will be unsuccessful.

Write collisions can occur both in master and slave mode. See also Section 0.1.3.2 Slave Select Management.

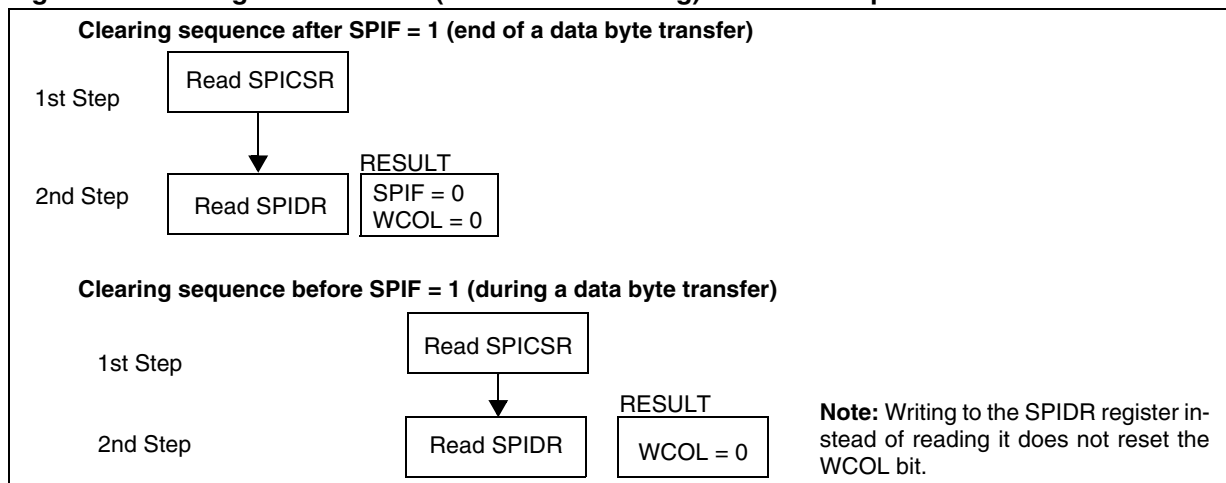
**Note:** A "read collision" will never occur since the received data byte is placed in a buffer in which access is always synchronous with the CPU operation.

The WCOL bit in the SPICSR register is set if a write collision occurs.

No SPI interrupt is generated when the WCOL bit is set (the WCOL bit is a status flag only).

Clearing the WCOL bit is done through a software sequence (see Figure 6).

**Figure 58. Clearing the WCOL Bit (Write Collision Flag) Software Sequence**



**SERIAL PERIPHERAL INTERFACE** (cont'd)**11.4.6 Low Power Modes**

Mode	Description
WAIT	No effect on SPI. SPI interrupt events cause the device to exit from WAIT mode.
HALT	SPI registers are frozen. In HALT mode, the SPI is inactive. SPI operation resumes when the device is woken up by an interrupt with “exit from HALT mode” capability. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetching). If several data are received before the wake-up event, then an overrun error is generated. This error can be detected after the fetch of the interrupt routine that woke up the Device.

**11.4.6.1 Using the SPI to wake up the device from Halt mode**

In slave configuration, the SPI is able to wake up the device from HALT mode through a SPIF interrupt. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetch). If multiple data transfers have been performed before software clears the SPIF bit, then the OVR bit is set by hardware.

**Note:** When waking up from HALT mode, if the SPI remains in Slave mode, it is recommended to perform an extra communications cycle to bring

the SPI from HALT mode state to normal state. If the SPI exits from Slave mode, it returns to normal state immediately.

**Caution:** The SPI can wake up the device from HALT mode only if the Slave Select signal (external  $\overline{SS}$  pin or the SSI bit in the SPICSR register) is low when the device enters HALT mode. So, if Slave selection is configured as external (see Section 0.1.3.2), make sure the master drives a low level on the  $\overline{SS}$  pin when the slave enters HALT mode.

**11.4.7 Interrupts**

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
SPI End of Transfer Event	SPIF	SPIE	Yes	Yes
Master Mode Fault Event	MODF			No
Overrun Error	OVR			No

**Note:** The SPI interrupt events are connected to the same interrupt vector (see Interrupts chapter). They generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

## SERIAL PERIPHERAL INTERFACE (Cont'd)

Table 17. SPI Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0031h	<b>SPIDR</b> Reset Value	MSB x	x	x	x	x	x	x	LSB x
0032h	<b>SPICR</b> Reset Value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0033h	<b>SPICSR</b> Reset Value	SPIF 0	WCOL 0	OVR 0	MODF 0	0	SOD 0	SSM 0	SSI 0

## 11.5 10-BIT A/D CONVERTER (ADC)

### 11.5.1 Introduction

The on-chip Analog to Digital Converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 7 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 7 different sources.

The result of the conversion is stored in a 10-bit Data Register. The A/D converter is controlled through a Control/Status Register.

### 11.5.2 Main Features

- 10-bit conversion
- Up to 7 channels with multiplexed input
- Linear successive approximation

- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in Figure 60.

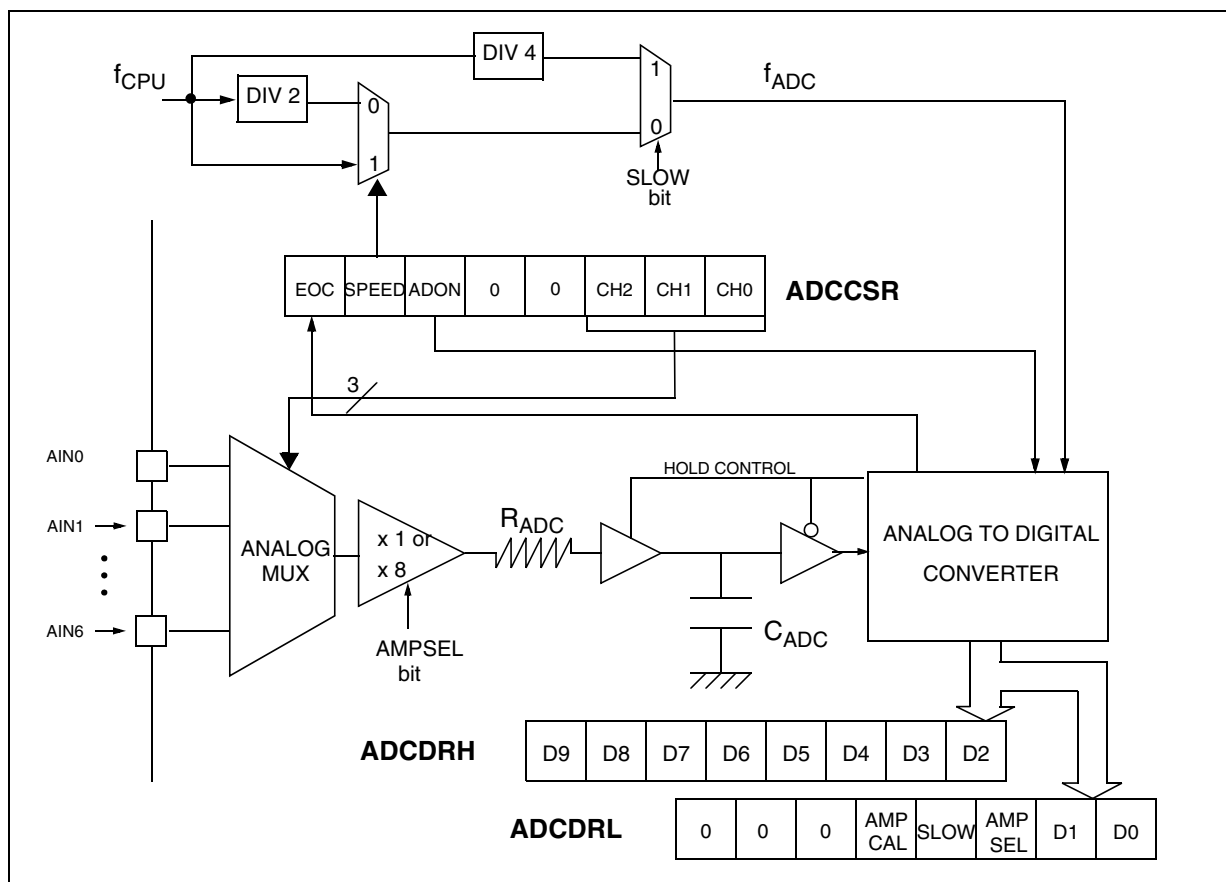
### 11.5.3 Functional Description

#### 11.5.3.1 Analog Power Supply

$V_{DDA}$  and  $V_{SSA}$  are the high and low level reference voltage pins. In some devices (refer to device pin out description) they are internally connected to the  $V_{DD}$  and  $V_{SS}$  pins.

Conversion accuracy may therefore be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines.

Figure 60. ADC Block Diagram





**10-BIT A/D CONVERTER (ADC)** (Cont'd)

Bit 2 = **AMPSEL** *Amplifier Selection Bit*

This bit is set and cleared by software.

0: Amplifier is not selected

1: Amplifier is selected

**Note:** When AMPSEL=1 it is mandatory that  $f_{ADC}$  be less than or equal to 2 MHz.

Bits 1:0 = **D[1:0]** *LSB of Analog Converted Value*

**Table 18. ADC Register Map and Reset Values**

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
0034h	<b>ADCCSR</b> Reset Value	EOC 0	SPEED 0	ADON 0	0 0	0 0	CH2 0	CH1 0	CH0 0
0035h	<b>ADCDRH</b> Reset Value	D9 x	D8 x	D7 x	D6 x	D5 x	D4 x	D3 x	D2 x
0036h	<b>ADCRL</b> Reset Value	0 0	0 0	0 0	AMPCAL 0	SLOW 0	AMPSEL 0	D1 x	D0 x

## 12 INSTRUCTION SET

### 12.1 ST7 ADDRESSING MODES

The ST7 Core features 17 different addressing modes which can be classified in seven main groups:

Addressing Mode	Example
Inherent	nop
Immediate	ld A,#\$55
Direct	ld A,\$55
Indexed	ld A,(\$55,X)
Indirect	ld A,([\$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The ST7 Instruction set is designed to minimize the number of bytes required per instruction: To do so, most of the addressing modes may be subdivided in two submodes called long and short:

- Long addressing mode is more powerful because it can use the full 64 Kbyte address space, however it uses more bytes and more CPU cycles.
- Short addressing mode is less powerful because it can generally only access page zero (0000h - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions use short addressing modes only (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

The ST7 Assembler optimizes the use of long and short addressing modes.

**Table 22. ST7 Addressing Mode Overview**

Mode			Syntax	Destination/ Source	Pointer Address (Hex.)	Pointer Size (Hex.)	Length (Bytes)
Inherent			nop				+ 0
Immediate			ld A,#\$55				+ 1
Short	Direct		ld A,\$10	00..FF			+ 1
Long	Direct		ld A,\$1000	0000..FFFF			+ 2
No Offset	Direct	Indexed	ld A,(X)	00..FF			+ 0 (with X register) + 1 (with Y register)
Short	Direct	Indexed	ld A,(\$10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,(\$1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[\$10]	00..FF	00..FF	byte	+ 2
Long	Indirect		ld A,[\$10.w]	0000..FFFF	00..FF	word	+ 2
Short	Indirect	Indexed	ld A,([\$10],X)	00..1FE	00..FF	byte	+ 2
Long	Indirect	Indexed	ld A,([\$10.w],X)	0000..FFFF	00..FF	word	+ 2
Relative	Direct		jrne loop	PC-128/PC+127 <sup>1)</sup>			+ 1
Relative	Indirect		jrne [\$10]	PC-128/PC+127 <sup>1)</sup>	00..FF	byte	+ 2
Bit	Direct		bset \$10,#7	00..FF			+ 1
Bit	Indirect		bset [\$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt \$10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [\$10],#7,skip	00..FF	00..FF	byte	+ 3

**Note:**

1. At the time the instruction is executed, the Program Counter (PC) points to the instruction following JRxx.

## INSTRUCTION GROUPS (cont'd)

Mnemo	Description	Function/Example	Dst	Src	H	I	N	Z	C
JRULE	Jump if (C + Z = 1)	Unsigned <=							
LD	Load	dst <= src	reg, M	M, reg			N	Z	
MUL	Multiply	X,A = X * A	A, X, Y	X, Y, A	0				0
NEG	Negate (2's compl)	neg \$10	reg, M				N	Z	C
NOP	No Operation								
OR	OR operation	A = A + M	A	M			N	Z	
POP	Pop from the Stack	pop reg pop CC	reg CC	M M					
PUSH	Push onto the Stack	push Y	M	reg, CC	H	I	N	Z	C
RCF	Reset carry flag	C = 0							0
RET	Subroutine Return								
RIM	Enable Interrupts	I = 0				0			
RLC	Rotate left true C	C <= Dst <= C	reg, M				N	Z	C
RRC	Rotate right true C	C => Dst => C	reg, M				N	Z	C
RSP	Reset Stack Pointer	S = Max allowed							
SBC	Subtract with Carry	A = A - M - C	A	M			N	Z	C
SCF	Set carry flag	C = 1							1
SIM	Disable Interrupts	I = 1				1			
SLA	Shift left Arithmetic	C <= Dst <= 0	reg, M				N	Z	C
SLL	Shift left Logic	C <= Dst <= 0	reg, M				N	Z	C
SRL	Shift right Logic	0 => Dst => C	reg, M				0	Z	C
SRA	Shift right Arithmetic	Dst7 => Dst => C	reg, M				N	Z	C
SUB	Subtraction	A = A - M	A	M			N	Z	C
SWAP	SWAP nibbles	Dst[7..4] <=> Dst[3..0]	reg, M				N	Z	
TNZ	Test for Neg & Zero	tnz lbl1					N	Z	
TRAP	S/W trap	S/W interrupt				1			
WFI	Wait for Interrupt					0			
XOR	Exclusive OR	A = A XOR M	A	M			N	Z	

## 13.2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 13.2.1 Voltage Characteristics

Symbol	Ratings	Maximum value	Unit
V <sub>DD</sub> - V <sub>SS</sub>	Supply voltage	7.0	V
V <sub>IN</sub>	Input voltage on any pin <sup>1)</sup> & <sup>2)</sup>	V <sub>SS</sub> -0.3 to V <sub>DD</sub> +0.3	
V <sub>ESD(HBM)</sub>	Electrostatic discharge voltage (Human Body Model)	see section 13.7.3 on page 128	
V <sub>ESD(MM)</sub>	Electrostatic discharge voltage (Machine Model)		

### 13.2.2 Current Characteristics

Symbol	Ratings	Maximum value	Unit
$I_{VDD}$	Total current into $V_{DD}$ power lines (source) <sup>3)</sup>	75	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>3)</sup>	150	
$I_{IO}$	Output current sunk by any standard I/O and control pin	20	
	Output current sunk by any high sink I/O pin	40	
	Output current source by any I/Os and control pin	- 25	
$I_{INJ(PIN)}^{2) \& 4)}$	Injected current on ISPSEL pin	$\pm 5$	
	Injected current on $\overline{RESET}$ pin	$\pm 5$	
	Injected current on OSC1 and OSC2 pins	$\pm 5$	
	Injected current on PB0 pin <sup>5)</sup>	+5	
	Injected current on any other pin <sup>6)</sup>	$\pm 5$	
$\Sigma I_{INJ(PIN)}^{2)}$	Total injected current (sum of all I/O and control pins) <sup>6)</sup>	$\pm 20$	

### 13.2.3 Thermal Characteristics

Symbol	Ratings	Value	Unit
$T_{STG}$	Storage temperature range	-65 to +150	°C
$T_J$	Maximum junction temperature (see Table 24, “THERMAL CHARACTERISTICS,” on page 147)		

#### Notes:

1. Directly connecting the  $\overline{RESET}$  and I/O pins to  $V_{DD}$  or  $V_{SS}$  could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 4.7k $\Omega$  for  $\overline{RESET}$ , 10k $\Omega$  for I/Os). Unused I/O pins must be tied in the same way to  $V_{DD}$  or  $V_{SS}$  according to their reset configuration.
2.  $I_{INJ(PIN)}$  must never be exceeded. This is implicitly insured if  $V_{IN}$  maximum is respected. If  $V_{IN}$  maximum cannot be respected, the injection current must be limited externally to the  $I_{INJ(PIN)}$  value. A positive injection is induced by  $V_{IN} > V_{DD}$  while a negative injection is induced by  $V_{IN} < V_{SS}$ . For true open-drain pads, there is no positive injection current, and the corresponding  $V_{IN}$  maximum must always be respected.
3. All power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) lines must always be connected to the external supply.
4. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
  - Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
  - Pure digital pins must have a negative injection less than 1.6mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.
5. No negative current injection allowed on PB0 pin.
6. When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterisation with  $\Sigma I_{INJ(PIN)}$  maximum current injection on four I/O port pins of the device.

## 15.2 DEVICE ORDERING INFORMATION

Figure 118. Ordering information scheme

Example:	ST7	F	LIT1xB	F	0	M	3	TR
<b>Family</b> ST7 Microcontroller Family								
<b>Memory type</b> F: Flash P: FASTROM								
<b>Version</b> 10B, 15B or 19B								
<b>No. of pins</b> F = 20 Y = 16								
<b>Memory size</b> 0 = 2K 1 = 4K								
<b>Package</b> B = DIP M = SO U = VFQFPN								
<b>Temperature range</b> 6 = -40 °C to 85 °C 3 = -40 °C to 125 °C								
<b>Shipping Option</b> TR = Tape & Reel packing Blank = Tube (DIP or SO) or Tray (VFQFPN)								
For a list of available options (e.g. data EEPROM, package) and orderable part numbers or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.								