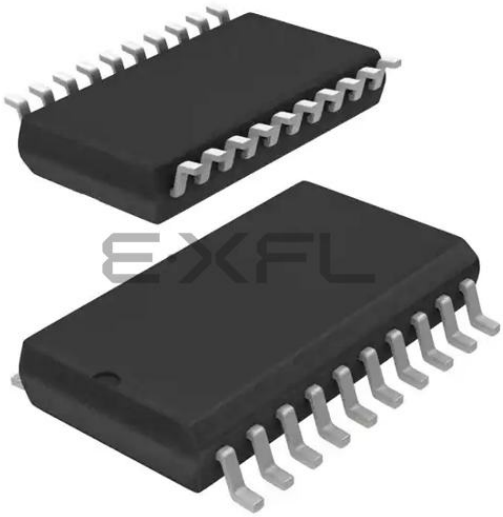

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SO
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flit19bf1m3

PIN DESCRIPTION (Cont'd)

Legend / Abbreviations for Table 1:

Type: I = input, O = output, S = supply

In/Output level: C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration:

– Input: float = floating, wpu = weak pull-up, int = interrupt, ana = analog

– Output: OD = open drain, PP = push-pull

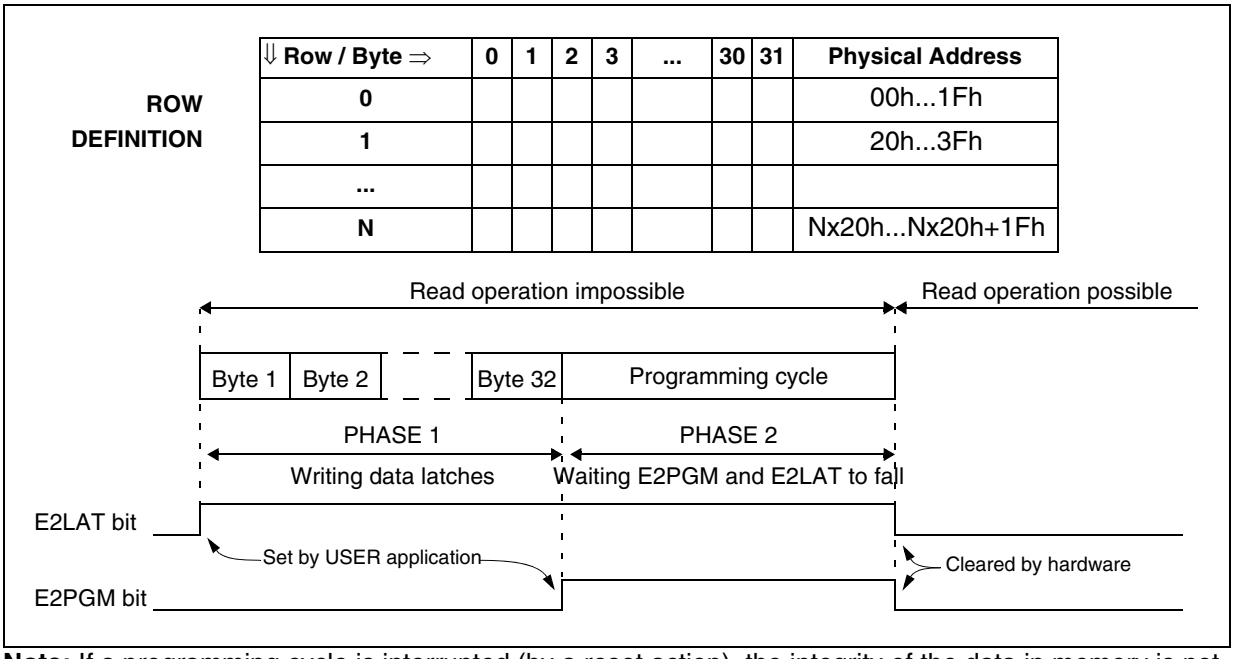
The RESET configuration of each pin is shown in bold which is valid as long as the device is in reset state.

Table 1. Device Pin Description

Pin No.			Pin Name	Type	Level		Port / Control						Main Function (after reset)	Alternate Function
							Input				Output			
SO20/DPI20	QFN20	SO16/DIP16			Input	Output	float	wpu	int	ana	OD	PP		
1	19	1	V_{SS} [1]	S									Ground	
2	20	2	V_{DD} [1]	S									Main power supply	
3	1	3	$\overline{RESET}$	I/O	C_T			**X**			X		Top priority non maskable interrupt (active low)	
4	2	4	PB0/COMPIN+/ AIN0/$\overline{SS}$	I/O	C_T		**X**	ei3		X	X	X	**Port B0**	ADC Analog Input 0 [2] or SPI Slave Select (active low) or Analog Comparator Input **Caution:** No negative current injection allowed on this pin.
5	3	5	PB1/AIN1/SCK	I/O	C_T		**X**			X	X	X	**Port B1**	ADC Analog Input 1 [2] or SPI Serial Clock
6	4	6	PB2/AIN2/MISO	I/O	C_T		**X**			X	X	X	**Port B2**	ADC Analog Input 2 [2] or SPI Master In/ Slave Out Data
7	5	7	PB3/AIN3/MOSI	I/O	C_T		**X**	ei2		X	X	X	**Port B3**	ADC Analog Input 3 [2] or SPI Master Out / Slave In Data
8	6	8	PB4/AIN4/CLKIN/ COMPIN-	I/O	C_T		**X**			X	X	X	**Port B4**	ADC Analog Input 4 [2] or External clock input or Analog Comparator External Reference Input
9	7	-	PB5/AIN5	I/O	C_T		**X**			X	X	X	**Port B5**	ADC Analog Input 5 [2]
10	8	-	PB6/AIN6	I/O	C_T		**X**			X	X	X	**Port B6**	ADC Analog Input 6 [2]
11	9	9	PA7/COMPOUT	I/O	C_T	HS	**X**	ei1			X	X	**Port A7**	Analog Comparator Output

DATA EEPROM (Cont'd)

Figure 9. Data E^2PROM Write Operation



Note: If a programming cycle is interrupted (by a reset action), the integrity of the data in memory is not guaranteed.

6 CENTRAL PROCESSING UNIT

6.1 INTRODUCTION

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

6.2 MAIN FEATURES

- 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes
- Two 8-bit index registers
- 16-bit stack pointer
- Low power modes
- Maskable hardware interrupts
- Non-maskable software interrupt

6.3 CPU REGISTERS

The six CPU registers shown in Figure 1 are not present in the memory mapping and are accessed by specific instructions.

Accumulator (A)

The Accumulator is an 8-bit general purpose register used to hold operands and the results of the arithmetic and logic calculations and to manipulate data.

Index Registers (X and Y)

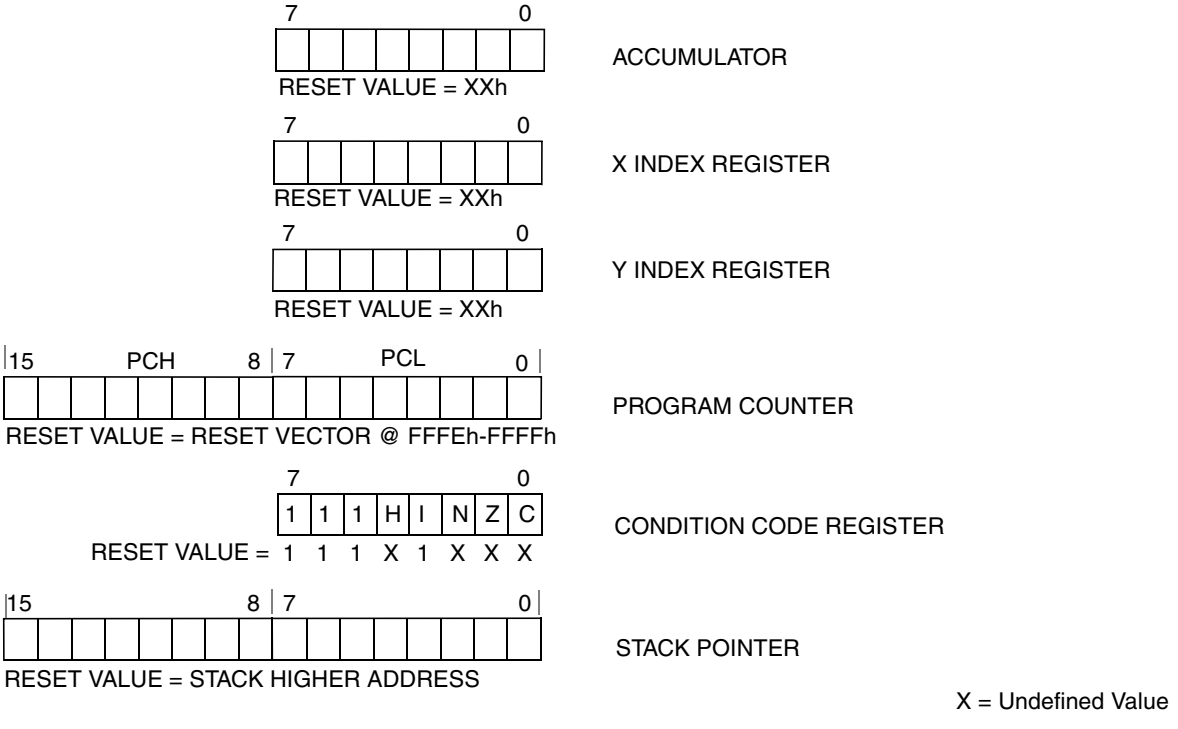
In indexed addressing modes, these 8-bit registers are used to create either effective addresses or temporary storage areas for data manipulation. (The Cross-Assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register.)

The Y register is not affected by the interrupt automatic procedures (not pushed to and popped from the stack).

Program Counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (Program Counter Low which is the LSB) and PCH (Program Counter High which is the MSB).

Figure 11. CPU Registers



7 SUPPLY, RESET AND CLOCK MANAGEMENT

The device includes a range of utility features for securing the application in critical situations (for example in case of a power brown-out), and reducing the number of external components.

Main features

- Clock Management
  - 1 MHz internal RC oscillator (enabled by option byte, available on ST7LITE15B and ST7LITE19B devices only)
  - 1 to 16 MHz External crystal/ceramic resonator (selected by option byte)
  - External Clock Input (enabled by option byte)
  - PLL for multiplying the frequency by 8 or 4 (enabled by option byte)
  - For clock ART counter only: PLL32 for multiplying the 8 MHz frequency by 4 (enabled by option byte). The 8 MHz input frequency is mandatory and can be obtained in the following ways:
    - –1 MHz RC + PLLx8
    - –16 MHz external clock (internally divided by 2)
    - –2 MHz. external clock (internally divided by 2) + PLLx8
    - –Crystal oscillator with 16 MHz output frequency (internally divided by 2)
- Reset Sequence Manager (RSM)
- System Integrity Management (SI)
  - Main supply Low voltage detection (LVD) with reset generation (enabled by option byte)
  - Auxiliary Voltage detector (AVD) with interrupt capability for monitoring the main supply (enabled by option byte)

7.1 INTERNAL RC OSCILLATOR ADJUSTMENT

The device contains an internal RC oscillator with an accuracy of 1% for a given device, temperature and voltage range (4.5V-5.5V). It must be calibrated to obtain the frequency required in the application. This is done by software writing a 10-bit calibration value in the RCCR (RC Control Register) and in the bits 6:5 in the SICSR (SI Control Status Register).

Whenever the microcontroller is reset, the RCCR returns to its default value (FFh), i.e. each time the device is reset, the calibration value must be loaded in the RCCR. Predefined calibration values are stored in EEPROM for 3 and 5V V_{DD} supply voltages at 25°C, as shown in the following table.

RCCR	Conditions	ST7LITE1xB Address
RCCRH0	V_{DD}=5V T_A=25°C f_{RC}=1MHz	DEE0h [1] (CR[9:2])
RCCRL0		DEE1h [1] (CR[1:0])
RCCRH1	V_{DD}=3.3V T_A=25°C f_{RC}=1MHz	DEE2h [1] (CR[9:2])
RCCRL1		DEE3h [1] (CR[1:0])

1. DEE0h, DEE1h, DEE2h and DEE3h addresses are located in a reserved area of non-volatile memory. They are read-only bytes for the application code. This area cannot be erased or programmed by any ICC operation.

For compatibility reasons with the SICSR register, CR[1:0] bits are stored in the 5th and 6th position of DEE1 and DEE3 addresses.

Notes:

– In 38-pulse ICC mode, the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. For ST7LITE10B devices which do not support the internal RC oscillator, the “option byte disabled” mode must be used (35-pulse ICC mode entry, clock provided by the tool).

– See “ELECTRICAL CHARACTERISTICS” on page 110. for more information on the frequency and accuracy of the RC oscillator.

– To improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

– These bytes are systematically programmed by ST, including on FASTROM devices.

Caution: If the voltage or temperature conditions change in the application, the frequency may need to be recalibrated.

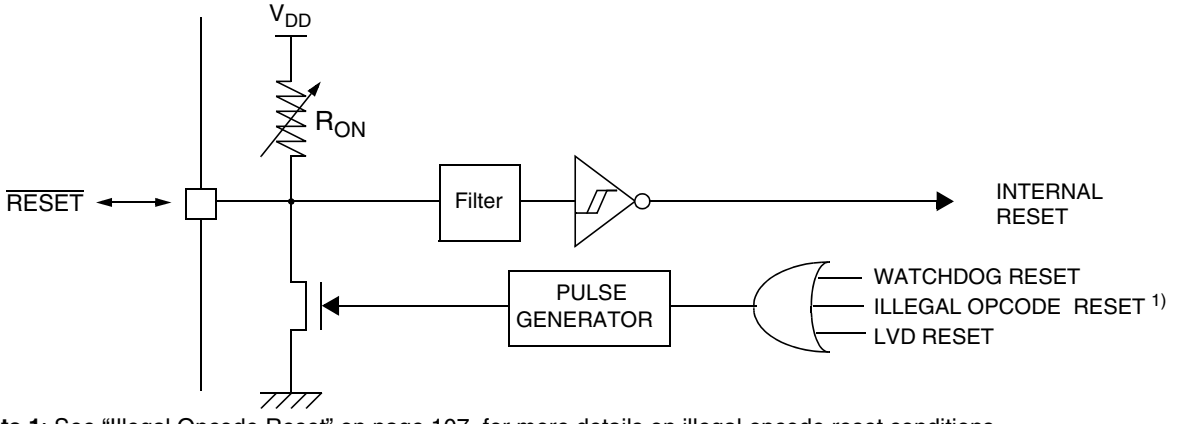
Refer to application note AN1324 for information on how to calibrate the RC frequency using an external reference signal.

7.2 PHASE LOCKED LOOP

The PLL can be used to multiply a 1MHz frequency from the RC oscillator or the external clock by 4 or 8 to obtain f_{OSC} of 4 or 8 MHz. The PLL is enabled and the multiplication factor of 4 or 8 is selected by 2 option bits.

– The x4 PLL is intended for operation with V_{DD} in the 2.7V to 3.3V range

Figure 16. Reset Block Diagram



Note 1: See “Illegal Opcode Reset” on page 107. for more details on illegal opcode reset conditions.

SYSTEM INTEGRITY MANAGEMENT (Cont'd)

7.6.3 Low Power Modes

Mode	Description
WAIT	No effect on SI. AVD interrupts cause the device to exit from Wait mode.
HALT	The SICSR register is frozen. The AVD remains active.

7.6.3.1 Interrupts

The AVD interrupt event generates an interrupt if the corresponding Enable Control Bit (AVDIE) is set and the interrupt mask in the CC register is reset (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
AVD event	AVDF	AVDIE	Yes	No

POWER SAVING MODES (Cont'd)

9.4 HALT MODE

The HALT mode is the lowest power consumption mode of the MCU. It is entered by executing the 'HALT' instruction when ACTIVE-HALT is disabled (see section 9.5 on page 43 for more details) and when the AWUEN bit in the AWUCSR register is cleared.

The MCU can exit HALT mode on reception of either a specific interrupt (see Table 5, "Interrupt Mapping," on page 37) or a RESET. When exiting HALT mode by means of a RESET or an interrupt, the oscillator is immediately turned on and the 256 or 4096 CPU cycle delay is used to stabilize the oscillator. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see Figure 26).

When entering HALT mode, the I bit in the CC register is forced to 0 to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

In HALT mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. All peripherals are not clocked except the ones which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of Watchdog operation with HALT mode is configured by the "WDGHALT" option bit of the option byte. The HALT instruction when executed while the Watchdog system is enabled, can generate a Watchdog RESET (see section 15.1 on page 149 for more details).

Figure 25. HALT Timing Overview

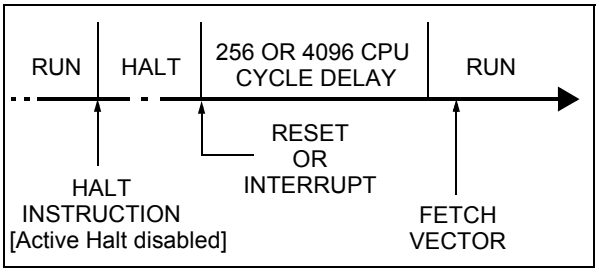
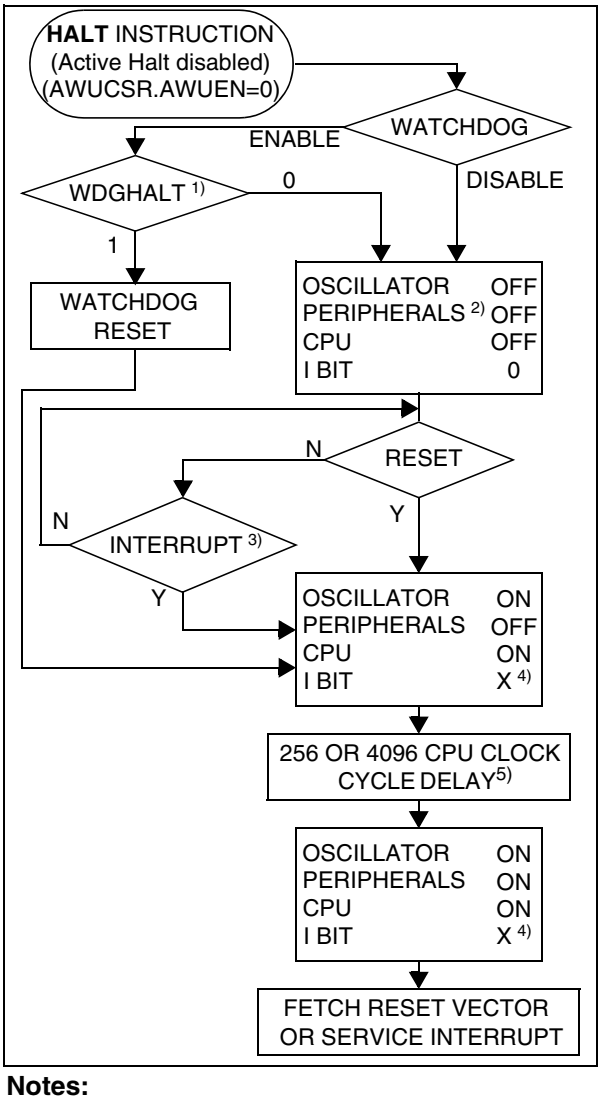


Figure 26. HALT Mode Flow-chart



Notes:

1. WDGHALT is an option bit. See option byte section for more details.

2. Peripheral clocked with an external clock source can still be active.

3. Only some specific interrupts can exit the MCU from HALT mode (such as external interrupt). Refer to Table 5 Interrupt Mapping for more details.

4. Before servicing an interrupt, the CC register is pushed on the stack. The I bit of the CC register is set during the interrupt routine and cleared when the CC register is popped.

5. If the PLL is enabled by option byte, it outputs the clock after a delay of $t_{STARTUP}$ (see Figure 13).

11 ON-CHIP PERIPHERALS

11.1 WATCHDOG TIMER (WDG)

11.1.1 Introduction

The Watchdog timer is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The Watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before the T6 bit becomes cleared.

11.1.2 Main Features

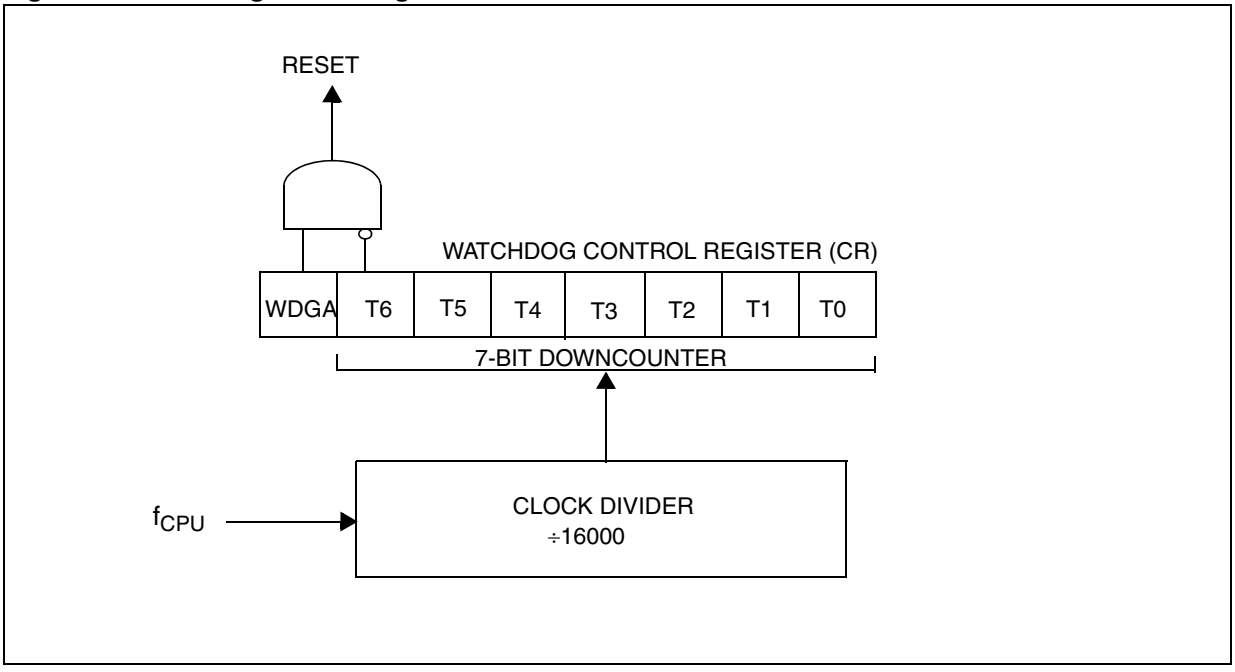
- Programmable free-running downcounter (64 increments of 16000 CPU cycles)
- Programmable reset
- Reset (if watchdog activated) when the T6 bit reaches zero
- Optional reset on HALT instruction (configurable by option byte)
- Hardware Watchdog selectable by option byte

11.1.3 Functional Description

The counter value stored in the CR register (bits T[6:0]), is decremented every 16000 machine cycles, and the length of the timeout period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T[6:0]) rolls over from 40h to 3Fh (T6 becomes cleared), it initiates a reset cycle pulling low the reset pin for typically 30µs.

Figure 34. Watchdog Block Diagram



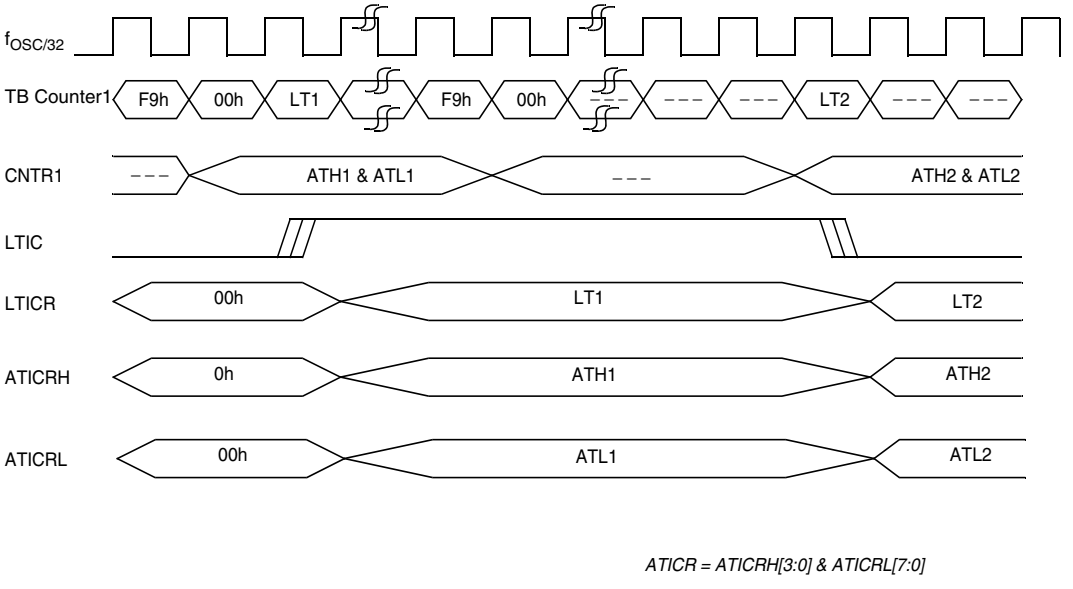
DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

– At the second input capture on the falling edge of the pulse, we assume that the values in the registers are as follows:
LTICR = LT2
ATICRH = ATH2
ATICRL = ATL2
Hence ATICR2 [11:0] = ATH2 & ATL2

Now pulse width P between first capture and second capture will be:

P = decimal (F9 – LT1 + LT2 + 1) * 0.004ms + decimal ((FFF * N) + N + ATICR2 - ATICR1 – 1) * 1ms where N = No of overflows of 12-bit CNTR1.

Figure 46. Long Range Input Capture Timing Diagram



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.4 Low Power Modes

Mode	Description
WAIT	No effect on AT timer
HALT	AT timer halted.

11.2.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt	Exit from Active-Halt
Overflow Event	OVF1	OVIE1	Yes	No	Yes
AT4 IC Event	ICF	ICIE	Yes	No	No
CMP Event	CMPFx	CMPIE	Yes	No	No
Overflow Event2	OVF2	OVIE2	Yes	No	No

Note: The CMP and AT4 IC events are connected to the same interrupt vector.
The OVF event is mapped on a separate vector (see Interrupts chapter).
They generate an interrupt if the enable bit is set in the ATCSR register and the interrupt mask in the CC register is reset (RIM instruction).

SERIAL PERIPHERAL INTERFACE (cont'd)

11.4.5.4 Single Master and Multimaster Configurations

There are two types of SPI systems:

– Single Master System

– Multimaster System

Single Master System

A typical single master system may be configured using a device as the master and four devices as slaves (see Figure 7).

The master device selects the individual slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins of the slave devices.

The $\overline{SS}$ pins are pulled high during reset since the master device ports will be forced to be inputs at that time, thus disabling the slave devices.

Note: To prevent a bus conflict on the MISO line, the master allows only one active slave device during a transmission.

For more security, the slave device may respond to the master with the received data byte. Then the master will receive the previous byte back from the slave device if all MISO and MOSI pins are connected and the slave has not written to its SPIDR register.

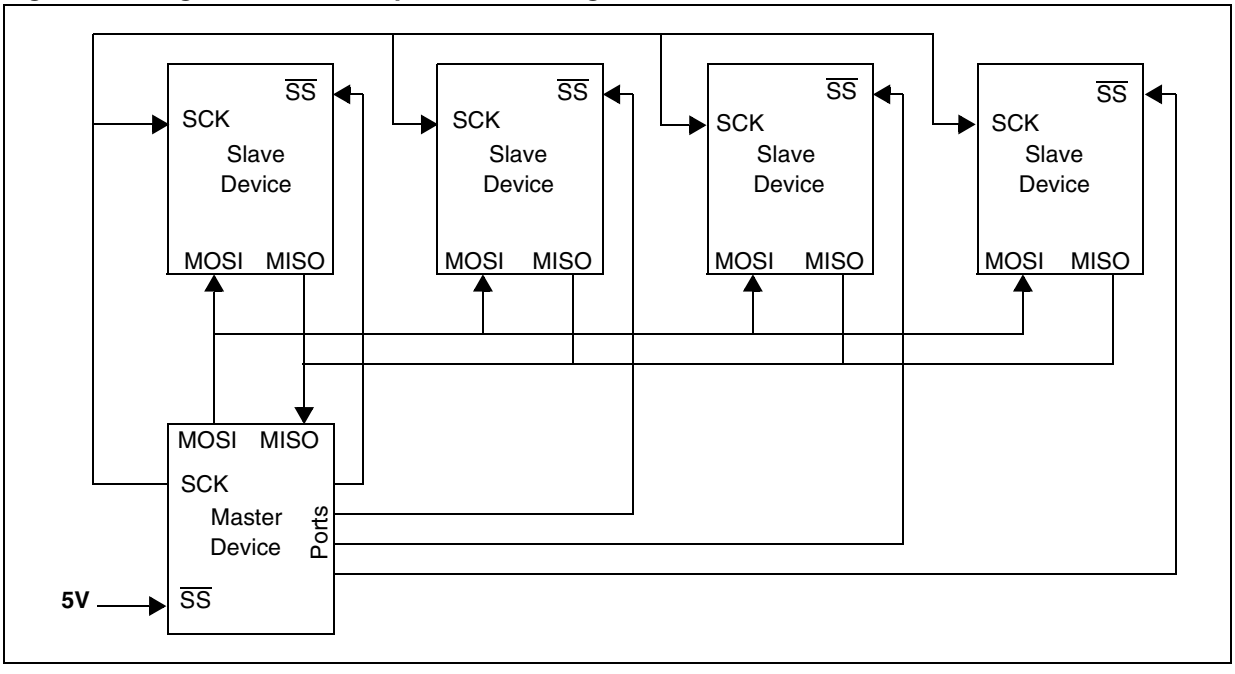
Other transmission security methods can use ports for handshake lines or data bytes with command fields.

Multimaster System

A multimaster system may also be configured by the user. Transfer of master control could be implemented using a handshake method through the I/O ports or by an exchange of code messages through the serial peripheral interface system.

The multimaster system is principally handled by the MSTR bit in the SPICR register and the MODF bit in the SPICSR register.

Figure 59. Single Master / Multiple Slave Configuration



SERIAL PERIPHERAL INTERFACE (cont'd)

11.4.6 Low Power Modes

Mode	Description
WAIT	No effect on SPI. SPI interrupt events cause the device to exit from WAIT mode.
HALT	SPI registers are frozen. In HALT mode, the SPI is inactive. SPI operation resumes when the device is woken up by an interrupt with "exit from HALT mode" capability. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetching). If several data are received before the wake-up event, then an overrun error is generated. This error can be detected after the fetch of the interrupt routine that woke up the Device.

11.4.6.1 Using the SPI to wake up the device from Halt mode

In slave configuration, the SPI is able to wake up the device from HALT mode through a SPIF interrupt. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetch). If multiple data transfers have been performed before software clears the SPIF bit, then the OVR bit is set by hardware.

Note: When waking up from HALT mode, if the SPI remains in Slave mode, it is recommended to perform an extra communications cycle to bring the SPI from HALT mode state to normal state. If the SPI exits from Slave mode, it returns to normal state immediately.

Caution: The SPI can wake up the device from HALT mode only if the Slave Select signal (external $\overline{SS}$ pin or the SSI bit in the SPICSR register) is low when the device enters HALT mode. So, if Slave selection is configured as external (see Section 0.1.3.2), make sure the master drives a low level on the $\overline{SS}$ pin when the slave enters HALT mode.

11.4.7 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
SPI End of Transfer Event	SPIF	SPIE	Yes	Yes
Master Mode Fault Event	MODF			No
Overrun Error	OVR			

Note: The SPI interrupt events are connected to the same interrupt vector (see Interrupts chapter). They generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in the CC register is reset (RIM instruction).

10-BIT A/D CONVERTER (ADC) (Cont'd)

11.5.6 Register Description

CONTROL/STATUS REGISTER (ADCCSR)

Read/Write (Except bit 7 read only)

Reset Value: 0000 0000 (00h)

7							0
EOC	SPEED	ADON	0	0	CH2	CH1	CH0

Bit 7 = **EOC** *End of Conversion*
This bit is set by hardware. It is cleared by hardware when software reads the ADCDRH register or writes to any bit of the ADCCSR register.
0: Conversion is not complete
1: Conversion complete

Bit 6 = **SPEED** *ADC clock selection*
This bit is set and cleared by software. It is used together with the SLOW bit to configure the ADC clock speed. Refer to the table in the SLOW bit description (ADCDRL register).

Bit 5 = **ADON** *A/D Converter on*
This bit is set and cleared by software.
0: A/D converter and amplifier are switched off
1: A/D converter and amplifier are switched on

Bits 4:3 = **Reserved.** Must be kept cleared.

Bits 2:0 = **CH[2:0]** *Channel Selection*
These bits are set and cleared by software. They select the analog input to convert.

Channel Pin*	CH2	CH1	CH0
AIN0	0	0	0
AIN1	0	0	1
AIN2	0	1	0
AIN3	0	1	1
AIN4	1	0	0
AIN5	1	0	1
AIN6	1	1	0

*The number of channels is device dependent. Refer to the device pinout description.

DATA REGISTER HIGH (ADCDRH)

Read Only

Reset Value: xxxx xxxx (xxh)

7							0
D9	D8	D7	D6	D5	D4	D3	D2

Bits 7:0 = **D[9:2]** *MSB of Analog Converted Value*

AMP CONTROL/DATA REGISTER LOW (ADCDRL)

Read/Write

Reset Value: 0000 00xx (0xh)

7							0
0	0	0	AMP CAL	SLOW	AMP-SEL	D1	D0

Bits 7:5 = Reserved. Forced by hardware to 0.

Bit 4 = **AMPCAL** *Amplifier Calibration Bit*
This bit is set and cleared by software. It is advised to use this bit to calibrate the ADC when amplifier is ON. Setting this bit internally connects amplifier input to 0V. Hence, corresponding ADC output can be used in software to eliminate amplifier-offset error.
0: Calibration off
1: Calibration on. (The input voltage of the amplifier is set to 0V)

Bit 3 = **SLOW** *Slow mode*
This bit is set and cleared by software. It is used together with the SPEED bit in the ADCCSR register to configure the ADC clock speed as shown on the table below.

f_{ADC}	SLOW	SPEED
$f_{CPU}/2$	0	0
f_{CPU}	0	1
$f_{CPU}/4$	1	x

Note: max f_{ADC} allowed = 4MHz (see section 13.11 on page 139)

11.6 ANALOG COMPARATOR (CMP)

11.6.1 Introduction

The CMP block consists of an analog comparator and an internal voltage reference. The voltage reference can be external or internal, selectable under program control. The comparator input pins COMPIN+ and COMPIN- are also connected to the A/D converter (ADC).

11.6.2 Main Features

11.6.2.1 On-chip Analog Comparator

The analog comparator compares the voltage at two input pins COMPIN+ and COMPIN- which are connected to VP and VN at the comparator input. When the analog input at COMPIN+ is less than the analog input at COMPIN-, the output of the comparator is 0. When the analog input at COMPIN+ is greater than the analog input at COMPIN-, the output of the comparator is 1.

The result of the comparison as 0 or 1 at COMPOUT is shown in Figure 62 on page 101.

Note:

To obtain a stable result, the comparator requires a stabilization time of 500ns. Please refer to section 13.12 on page 143.

Table 19. Comparison Result

CINV	Input Conditions	COMPOUT
0	VP > VN	1
	VN > VP	0
1	VP > VN	0
	VN > VP	1

11.6.2.2 Programmable External/Internal Voltage Reference

The voltage reference module can be configured to connect the comparator pin COMPIN- to one of the following:

- Fixed internal voltage bandgap
- Programmable internal reference voltage
- External voltage reference

1) Fixed Internal Voltage Bandgap
   The voltage reference module can generate a fixed voltage reference of 1.2V on the VN input. This is done by setting the VCBGR bit in the VREFCR register.

2) Programmable Internal Voltage Reference
   The internal voltage reference module can provide 16 distinct internally generated voltage levels from 3.2V to 0.2V each at a step of 0.2V on comparator pin VN. The voltage is selected through the VR[3:0] bits in the VREFCR register.

3) External Reference Voltage
   If a reference voltage other than that generated by the internal voltage reference module is required, COMPIN- can be connected to an external voltage source. This configuration can be selected by setting the VCEXT bit in the VREFCR register.

11.6.3 Functional Description

To make an analog comparison, the CMPON bit in the CMPCR register must be set to power-on the comparator and internal voltage reference module.

The VP comparator input is mapped on PB0 and is also connected to ADC channel 0.

The VN comparator input is mapped on PB4 for external voltage input, and is also connected to ADC channel 4.

The internal voltage reference can provide a range of different voltages to the comparator VN input, selected by several bits in the VREFCR register, as described in Table 20.

To select pins PB0 and PB4 for A/D conversion, (default reset state), channel 0 or 4 must be selected through the channel selection bits in the ADCCSR register (refer to Section 11.5.6)

The comparator output is connected to pin PA7 when the COUT bit in the CMPCR register is set.

The comparator output is also connected internally to the break function of the 12-bit Autoreload Timer (refer to Section 11.2)

When the Comparator is OFF, the output value of comparator is ‘1’.

Important note: To avoid spurious toggling of the output of the comparator due to noise on the voltage reference, it is recommended to enable the hysteresis through the CHYST bit in the CMPCR register.

ANALOG COMPARATOR (Cont'd)

Bit 4 = **CMPIF** *Comparator Interrupt Flag*

This bit is set by hardware when interrupt is generated at the rising edge (CINV = 0) or falling edge (CINV = 1) of comparator output. This bit is cleared by reading the CMPCR register. Writing to this bit does not change the value.
0 : Comparator interrupt flag cleared
1 : Comparator interrupt flag set and can generate interrupt if CMPIE is set.

Bit 3 : **CMPIE** *Comparator Interrupt Enable*

This bit is set or reset by software and cleared by hardware reset. This bit enables or disables the interrupt generation depending on interrupt flag
0: Interrupt not generated
1: Interrupt generated if interrupt flag is set

Note:

This bit should be set to enable interrupt only after the comparator has been switched ON, i.e. when CMPON is set.

Once CMPON bit is set, it is recommended to wait the specified stabilization time before setting CMPIE bit in order to avoid a spurious interrupt (see section 13.12 on page 143).

Bit 2 : **CMP** *Comparator Output*

This bit is set or reset by software and cleared by hardware reset. It stores the value of comparator output.

Bit 1 = **COUT** *Comparator Output Enable on Port*
This bit is set or cleared by software. When this bit is set, the comparator output is available on PA7 port.
0 : Comparator output not connected to PA7
1 : Comparator output connected to PA7

Bit 0 : **CMPON** *Comparator ON/OFF*
This bit is set or cleared by software and reset by hardware reset. This bit is used to switch ON/OFF the comparator, internal voltage reference and current bias which provides 4µA current to both.
0: Comparator, Internal Voltage Reference, Bias OFF (in power-down state).
1: Comparator, Internal Voltage Reference, Bias ON

Note: For the comparator interrupt generation, it takes 250ns delay from comparator output change to rising or falling edge of interrupt generated.

Table 21. Analog Comparator Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Ch	**VREFCR**	VCEXT	VCBGR	VR3	VR2	VR1	VR0	-	-
	Reset Value	0	0	0	0	0	0	0	0
002Dh	**CMPCR**	CHYST	-	CINV	CMPIF	CMPIE	CMP	COUT	CMPON
	Reset value	1	0	0	0	0	0	0	0

13 ELECTRICAL CHARACTERISTICS

13.1 PARAMETER CONDITIONS

Unless otherwise specified, all voltages are referred to V_{SS}.

13.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A=25°C and T_A=$T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

13.1.2 Typical values

Unless otherwise specified, typical data are based on T_A=25°C, V_{DD}=5V (for the 4.5V≤V_{DD}≤5.5V voltage range) and V_{DD}=3.3V (for the 3V≤V_{DD}≤3.6V voltage range). They are given only as design guidelines and are not tested.

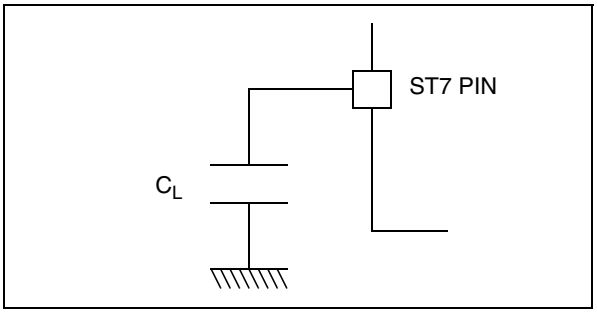
13.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

13.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 63.

Figure 63. Pin loading conditions



13.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 64.

Figure 64. Pin input voltage

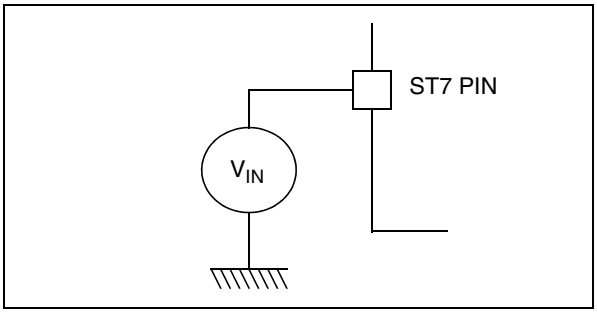
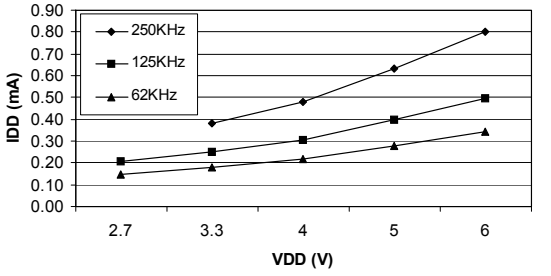
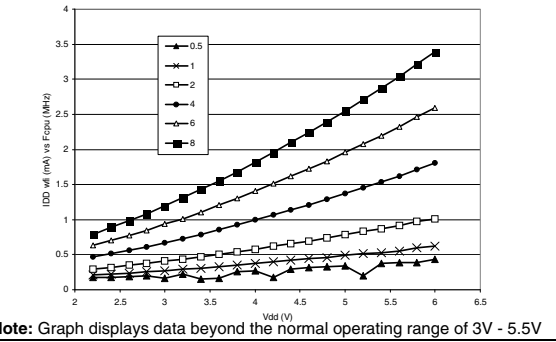


Figure 73. Typical I_{DD} in SLOW vs. f_{CPU}



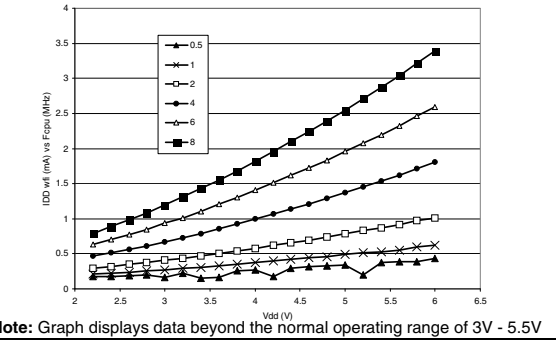
Note: Graph displays data beyond the normal operating range of 3V - 5.5V

Figure 74. Typical I_{DD} in WAIT vs. f_{CPU}



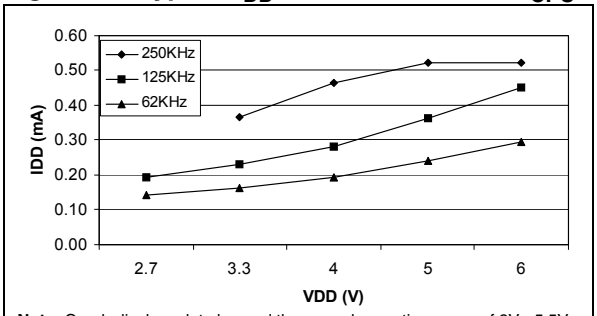
Note: Graph displays data beyond the normal operating range of 3V - 5.5V

Figure 75. Typical I_{DD} in WAIT at f_{CPU}= 8MHz



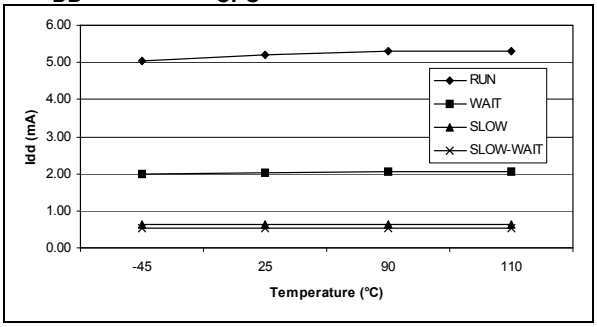
Note: Graph displays data beyond the normal operating range of 3V - 5.5V

Figure 76. Typical I_{DD} in SLOW-WAIT vs. f_{CPU}



Note: Graph displays data beyond the normal operating range of 3V - 5.5V

Figure 77. Typical I_{DD} vs. Temperature at V_{DD} = 5V and f_{CPU} = 8MHz



13.8 I/O PORT PIN CHARACTERISTICS

13.8.1 General Characteristics

Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage			V_{SS} - 0.3		0.3xV_{DD}	V
V_{IH}	Input high level voltage			0.7xV_{DD}		V_{DD} + 0.3	
V_{hys}	Schmitt trigger voltage hysteresis [1]				400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$				±1	µA
I_S	Static current consumption induced by each floating input pin [2]	Floating input mode			400		
R_{PU}	Weak pull-up equivalent resistor [3]	$V_{IN}=V_{SS}$	V_{DD}=5V	50	120	250	kΩ
			V_{DD}=3V		160		
C_{IO}	I/O pin capacitance				5		pF
$t_{f(IO)out}$	Output high to low level fall time [1]	C_L=50pF Between 10% and 90%			25		ns
$t_{r(IO)out}$	Output low to high level rise time [1]				25		
$t_{w(IT)in}$	External interrupt pulse time [4]			1			t_{CPU}

Notes:

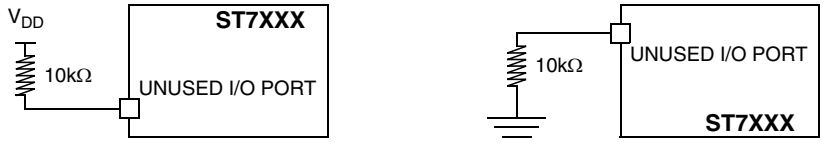
1. Data based on validation/design results.

2. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see Figure 80). Static peak current value taken at a fixed V_{IN} value, based on design simulation and technology characteristics, not tested in production. This value depends on V_{DD} and temperature values.

3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor.

4. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 80. Two typical Applications with unused I/O Pin



Caution: During normal operation the ICCCLK pin must be pulled-up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset.
Note: I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

I/O PORT PIN CHARACTERISTICS (Cont'd)

Figure 99. Typical V_{DD}-V_{OH} at V_{DD}=2.7V (Port C)

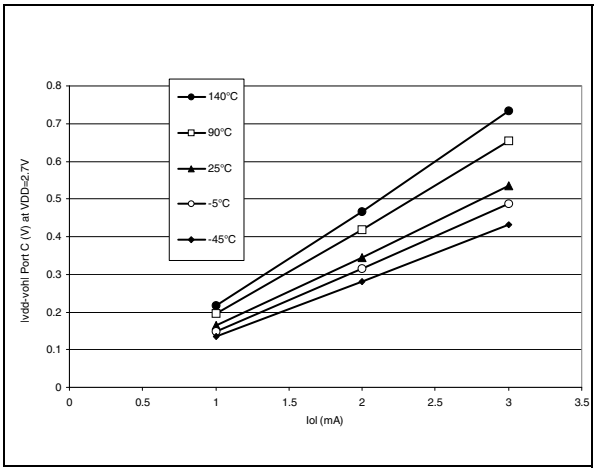


Figure 100. Typical V_{DD}-V_{OH} at V_{DD}=3.3V (Port C)

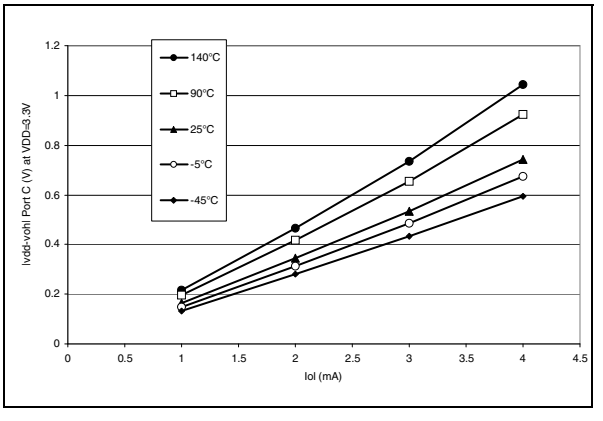


Figure 101. Typical V_{DD}-V_{OH} at V_{DD}=5V (Port C)

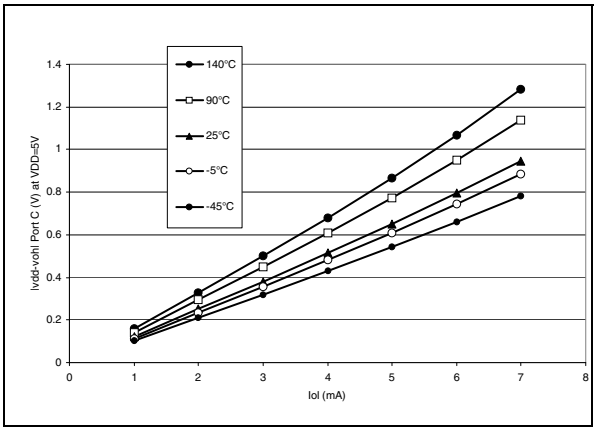


Figure 102. Typical V_{DD}-V_{OH} vs. V_{DD} (Standard)

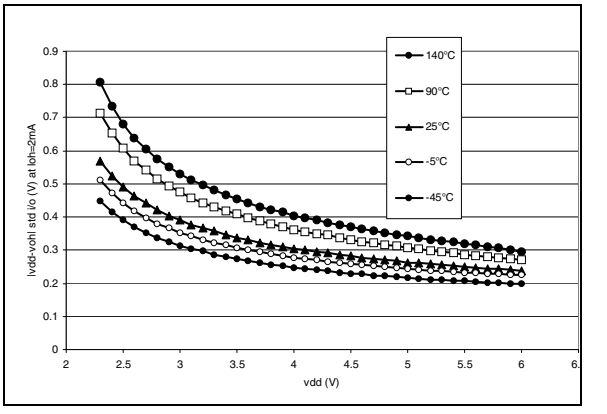


Figure 103. Typical V_{DD}-V_{OH} vs. V_{DD} (High Sink)

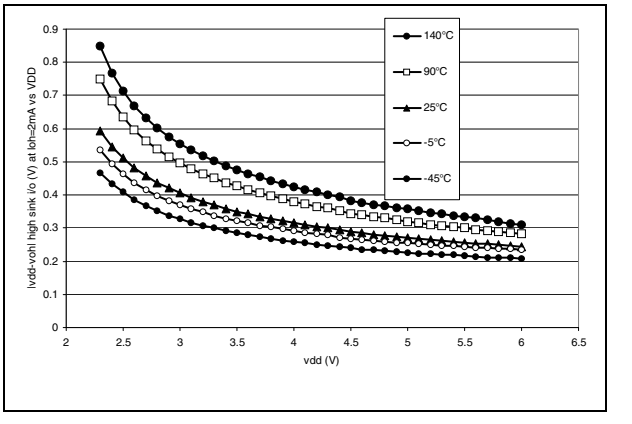
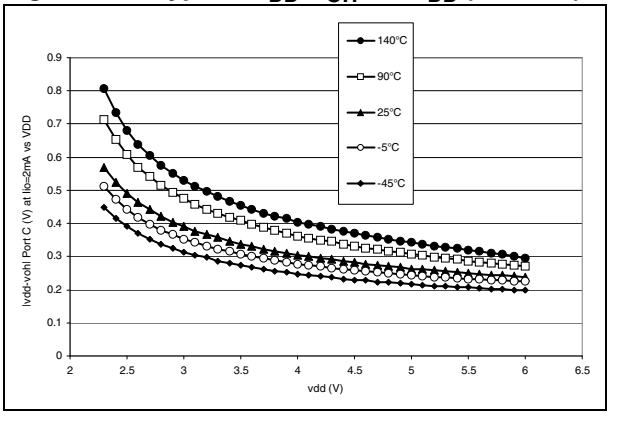
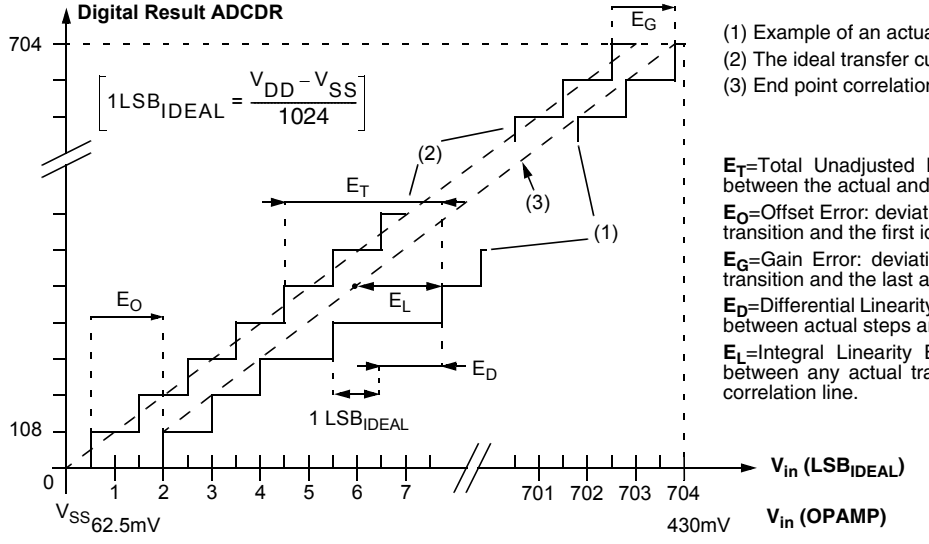


Figure 104. Typical V_{DD}-V_{OH} vs. V_{DD} (PORT C)



ADC CHARACTERISTICS (Cont'd)

Figure 112. ADC Accuracy Characteristics with amplifier enabled



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.

E_O=Offset Error: deviation between the first actual transition and the first ideal one.

E_G=Gain Error: deviation between the last ideal transition and the last actual one.

E_D=Differential Linearity Error: maximum deviation between actual steps and the ideal one.

E_L=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Note:

1. When the AMPSEL bit in the ADCDRL register is set, it is mandatory that f_{ADC} be less than or equal to 2 MHz. (if f_{CPU}=8MHz. then SPEED=0, SLOW=1).