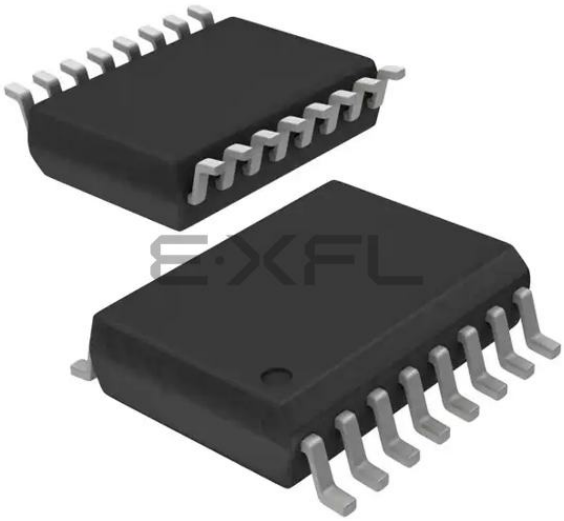

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	11
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st7flit19by1m3

FLASH PROGRAM MEMORY (Cont'd)

4.4 ICC interface

ICP needs a minimum of 4 and up to 6 pins to be connected to the programming tool. These pins are:

- $\overline{\text{RESET}}$: device reset
- V_{SS}: device power supply ground
- ICCCLK: ICC output serial clock pin
- ICCDATA: ICC input serial data pin
- OSC1: main clock input for external source (not required on devices without OSC1/OSC2 pins)
- V_{DD}: application board power supply (optional, see Note 3)

Notes:

1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the Programming Tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the Programming Tool documentation for recommended resistor values.

2. During the ICP session, the programming tool must control the $\overline{\text{RESET}}$ pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor<1K). A schottky diode can be used to isolate the application RESET circuit in this case. When using a classical RC network with R>1K or a reset management IC with open drain output and pull-up resistor>1K, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.

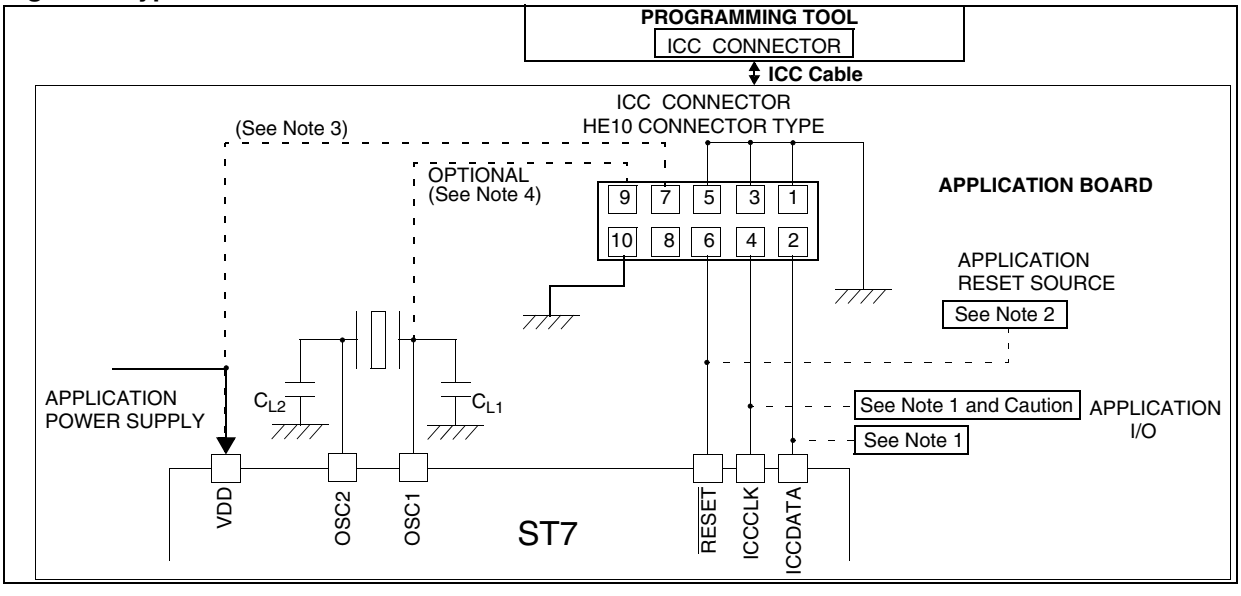
3. The use of pin 7 of the ICC connector depends on the Programming Tool architecture. This pin must be connected when using most ST Programming Tools (it is used to monitor the application power supply). Please refer to the Programming Tool manual.

4. Pin 9 has to be connected to the OSC1 pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability need to have OSC2 grounded in this case.

5. In 38-pulse ICC mode, the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte. For ST7LITE10B devices which do not support the internal RC oscillator, the "option byte disabled" mode must be used (35-pulse ICC mode entry, clock provided by the tool).

Caution: During normal operation the ICCCLK pin must be pulled- up, internally or externally (external pull-up of 10k mandatory in noisy environment). This is to avoid entering ICC mode unexpectedly during a reset. In the application, even if the pin is configured as output, any reset will put it back in input pull-up.

Figure 6. Typical ICC Interface



7.4 MULTI-OSCILLATOR (MO)

The main clock of the ST7 can be generated by four different source types coming from the multi-oscillator block (1 to 16MHz):

- an external source
- 5 different configurations for crystal or ceramic resonator oscillators
- an internal high frequency RC oscillator

Each oscillator is optimized for a given frequency range in terms of consumption and is selectable through the option byte. The associated hardware configurations are shown in Table 4. Refer to the electrical characteristics section for more details.

External Clock Source

In this external clock mode, a clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC1 pin while the OSC2 pin is tied to ground.

Note: when the Multi-Oscillator is not used, PB4 is selected by default as external clock.

Crystal/Ceramic Oscillators

In this mode, with a self-controlled gain feature, oscillator of any frequency from 1 to 16MHz can be placed on OSC1 and OSC2 pins. This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

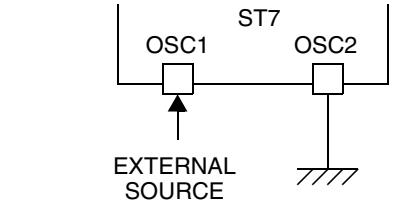
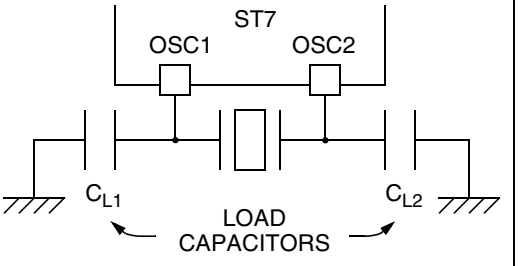
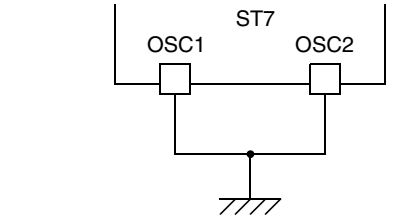
These oscillators are not stopped during the RESET phase to avoid losing time in the oscillator start-up phase.

Internal RC Oscillator

In this mode, the tunable 1%RC oscillator is used as main clock source. The two oscillator pins have to be tied to ground if dedicately using for oscillator else can be found as general purpose IO.

The calibration is done through the RCCR[7:0] and SICSR[6:5] registers.

Table 4. ST7 Clock Sources

	Hardware Configuration
External Clock	
Crystal/Ceramic Resonators	
Internal RC Oscillator	

SYSTEM INTEGRITY MANAGEMENT (Cont'd)

7.6.2 Auxiliary Voltage Detector (AVD)

The Voltage Detector function (AVD) is based on an analog comparison between a $V_{IT-(AVD)}$ and $V_{IT+(AVD)}$ reference value and the V_{DD} main supply voltage (V_{AVD}). The $V_{IT-(AVD)}$ reference value for falling voltage is lower than the $V_{IT+(AVD)}$ reference value for rising voltage in order to avoid parasitic detection (hysteresis).

The output of the AVD comparator is directly readable by the application software through a real time status bit (AVDF) in the SICSR register. This bit is read only.

Caution: The AVD functions only if the LVD is enabled through the option byte.

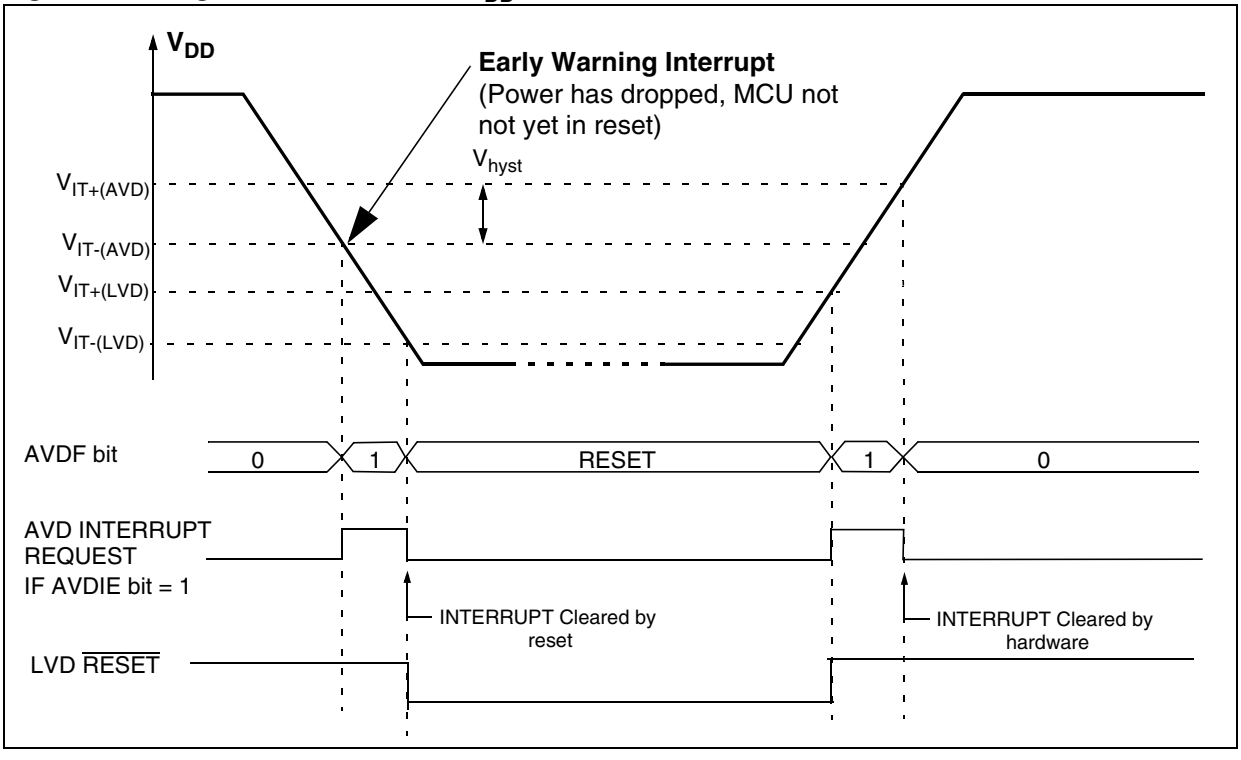
7.6.2.1 Monitoring the V_{DD} Main Supply

The AVD voltage threshold value is relative to the selected LVD threshold configured by option byte (see section 15.1 on page 149).

If the AVD interrupt is enabled, an interrupt is generated when the voltage crosses the $V_{IT+(LVD)}$ or $V_{IT-(AVD)}$ threshold (AVDF bit is set).

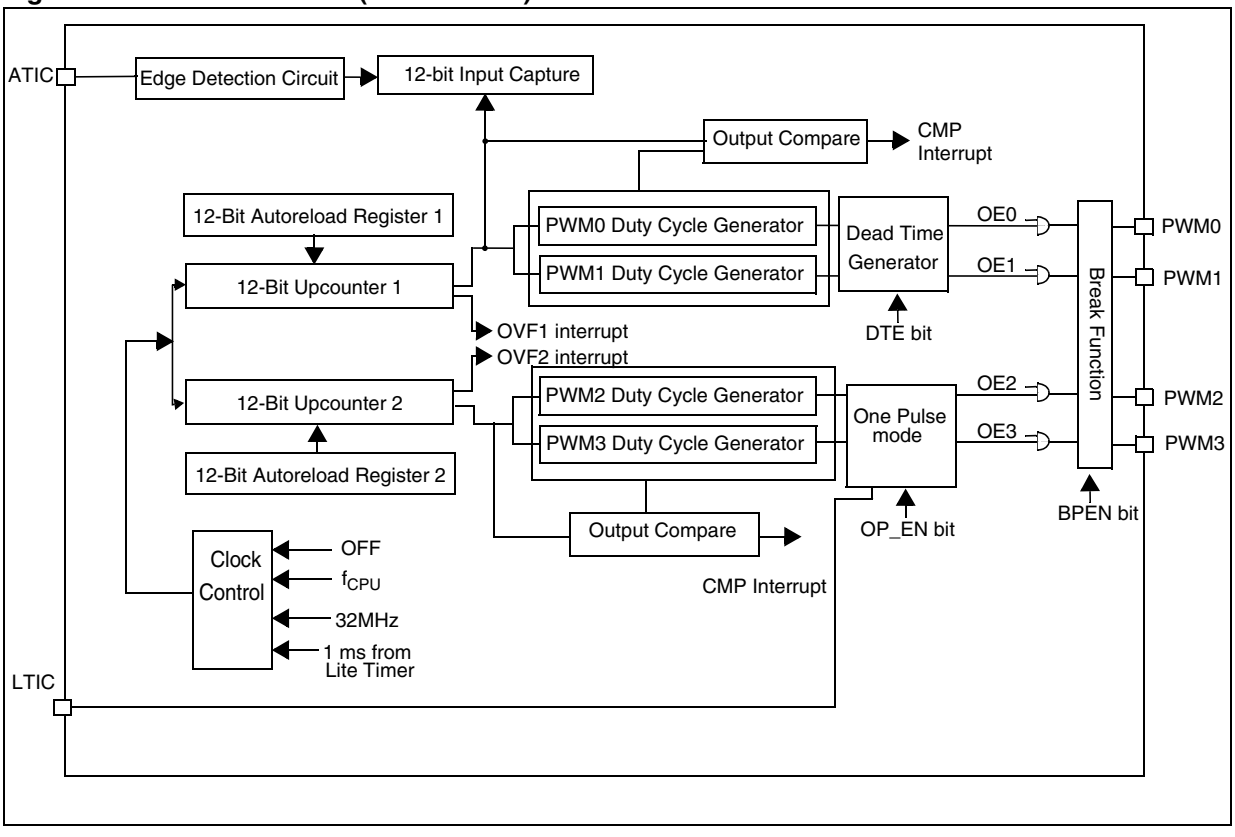
In the case of a drop in voltage, the AVD interrupt acts as an early warning, allowing software to shut down safely before the LVD resets the microcontroller. See Figure 20.

Figure 20. Using the AVD to Monitor V_{DD}



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

Figure 36. Dual Timer Mode (ENCNTR2=1)



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

Figure 38. PWM Function

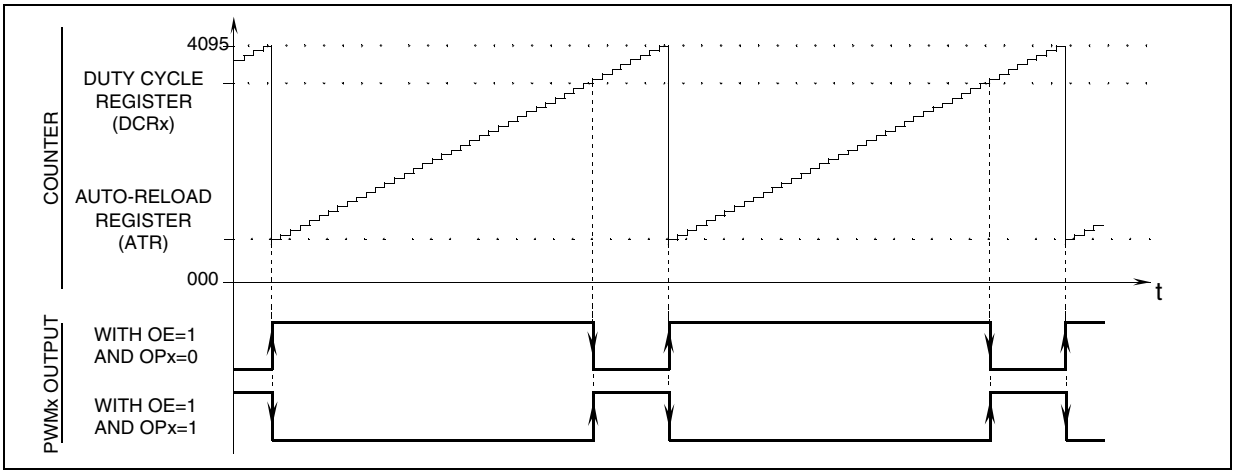
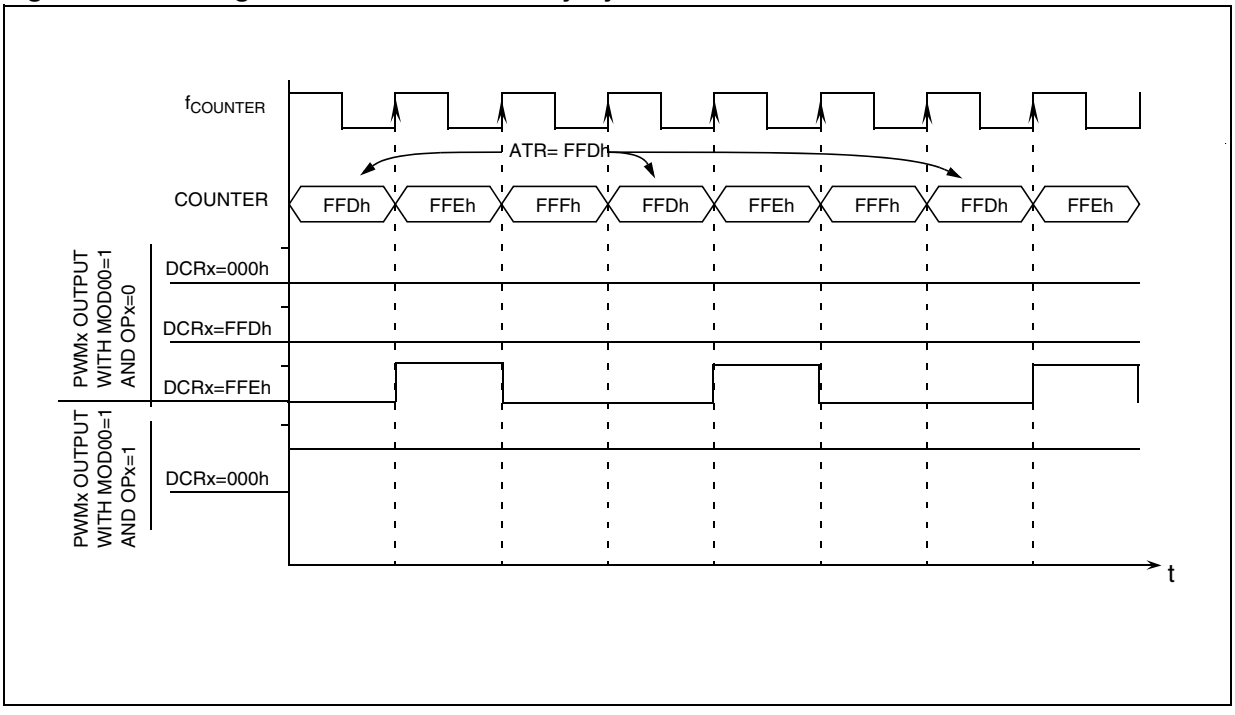


Figure 39. PWM Signal from 0% to 100% Duty Cycle



DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.3.6 One Pulse Mode

One Pulse Mode can be used to control PWM2/3 signal with an external LTIC pin. This mode is available only in dual timer mode i.e. only for CNTR2, when the OP_EN bit in PWM3CSR register is set.

One Pulse Mode is activated by the external LTIC input. The active edge of the LTIC pin is selected by the OPEDGE bit in the PWM3CSR register.

After getting the active edge of the LTIC pin, CNTR2 is reset (000h) and PWM3 is set to high. CNTR2 starts counting from 000h, when it reaches the active DCR3 value then the PWM3 output goes low. Till this time, any further transitions on the LTIC signal will have no effect. If there are LTIC transitions after CNTR2 reaches the DCR3 value, CNTR2 is reset again and the PWM3 output goes high.

If there is no LTIC active edge then CNTR2 will count till it reaches the ATR2 value, and then it will be reset again and the PWM3 output is set to high. The counter again starts counting from 000h, when it reaches the active DCR3 value the PWM3 output goes low, the counter counts till it reaches the ATR2 value, it resets and the PWM3 output is set to high and it goes on the same way.

The same operation applies for the PWM2 output, but in this case the comparison is done on the DCR2 value.

The OP_EN and OPEDGE bits take effect on the fly and are not synchronized with the CNTR2 overflow.

The OP2/3 bits can be used to inverse the polarity of the PWM2/3 outputs in one-pulse mode. The update of these bits (OP2/3) is synchronized with the CNTR2 overflow, they will be updated if the TRAN2 bit is set.

Notes:

1. If CNTR2 is running at 32 MHz, the time taken from activation of LTIC input and CNTR2 reset is between 2 and 3 t_{CNTR2} cycles, i.e. 66 ns to 99 ns (with 8 MHz f_{cpu}).

2. The Lite Timer input capture interrupt must be disabled while 12-bit ARTimer is in One Pulse Mode. This is to avoid spurious interrupts.

3. The priority of various events affecting PWM3 is as follows:

– Break (Highest priority)

– One-pulse mode with active LTIC edge

– Forced overflow (by FORCE2 bit)

– One-pulse mode without active LTIC edge

– Normal PWM operation. (Lowest priority)

4. It is possible to synchronize the update of DCR2/3 registers and OP2/3 bits with the CNTR2 reset. This is managed by the overflow interrupt which is generated if CNTR2 is reset either due to an ATR match or an active pulse on the LTIC pin.

5. Updating the DCR2/3 registers and OP2/3 bits in one-pulse mode is done dynamically by software using force update (FORCE2 bit in the ATCSR2 register).

6. DCR3 update in this mode is not synchronized with any event. Consequently the next PWM3 cycle just after the change may be longer than expected (refer to Figure 15).

7. In One Pulse Mode the ATR2 value must be greater than the DCR2/3 value for the PWM2/3 outputs. (contrary to normal PWM mode)

8. If there is an active edge on the LTIC pin after the CNTR2 has reset due to an ATR2 match, then the timer gets reset again. The duty cycle may be modified depending on whether the new DCR value is less than or more than the previous value.

9. The TRAN2 bit must be set simultaneously with the FORCE2 bit in the same instruction after a write to the DCR register.

10. The ATR2 value should be changed after an overflow in one pulse mode to avoid an irregular PWM cycle.

11. When exiting from one pulse mode, the OP_EN bit in the PWM3CSR register must be reset first and then the ENCNTR2 bit (if CNTR2 is to be stopped).

How to Enter One Pulse Mode:

1. Load the ATR2H/ATR2L registers with required value.

2. Load the DCR3H/DCR3L registers for PWM3 output. The ATR2 value must be greater than DCR3.

3. Set the OP3 bit in the PWM3CSR register if polarity change is required.

4. Start the CNTR2 counter by setting the ENCNTR2 bit in the ATCSR2 register.

5. Set TRAN2 bit in ATCSR2 to enable transfer.

6. Wait for an overflow event by polling the OVF2 flag in the ATCSR2 register.

7. Select the counter clock using the CK[1:0] bits in the ATCSR register.

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.4 Low Power Modes

Mode	Description
WAIT	No effect on AT timer
HALT	AT timer halted.

11.2.5 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt	Exit from Active-Halt
Overflow Event	OVF1	OVIE1	Yes	No	Yes
AT4 IC Event	ICF	ICIE	Yes	No	No
CMP Event	CMPFx	CMPIE	Yes	No	No
Overflow Event2	OVF2	OVIE2	Yes	No	No

Note: The CMP and AT4 IC events are connected to the same interrupt vector.
The OVF event is mapped on a separate vector (see Interrupts chapter).
They generate an interrupt if the enable bit is set in the ATCSR register and the interrupt mask in the CC register is reset (RIM instruction).

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

11.2.6 Register Description

TIMER CONTROL STATUS REGISTER (ATCSR)
Read / Write
Reset Value: 0x00 0000 (x0h)

7							0
0	ICF	ICIE	CK1	CK0	OVF1	OVFIE1	CMPIE

Bit 7 = Reserved.

Bit 6 = **ICF** *Input Capture Flag.*
This bit is set by hardware and cleared by software by reading the ATICR register (a read access to ATICRH or ATICRL will clear this flag). Writing to this bit does not change the bit value.
0: No input capture
1: An input capture has occurred

Bit 5 = **ICIE** *IC Interrupt Enable.*
This bit is set and cleared by software.
0: Input capture interrupt disabled
1: Input capture interrupt enabled

Bits 4:3 = **CK[1:0]** *Counter Clock Selection.*
These bits are set and cleared by software and cleared by hardware after a reset. They select the clock frequency of the counter.

Counter Clock Selection	CK1	CK0
OFF	0	0
32 MHz	1	1
f_{LTIMER} (1 ms timebase @ 8 MHz)	0	1
f_{CPU}	1	0

Bit 2 = **OVF1** *Overflow Flag.*
This bit is set by hardware and cleared by software by reading the ATCSR register. It indicates the transition of the counter1 CNTR1 from FFFh to ATR1 value.
0: No counter overflow occurred
1: Counter overflow occurred

Bit 1 = **OVFIE1** *Overflow Interrupt Enable.*
This bit is read/write by software and cleared by hardware after a reset.
0: Overflow interrupt disabled.
1: Overflow interrupt enabled.

Bit 0 = **CMPIE** *Compare Interrupt Enable*.
This bit is read/write by software and cleared by hardware after a reset. It can be used to mask the interrupt generated when any of the CMPFx bit is set.
0: Output compare interrupt disabled.
1: Output Compare interrupt enabled.

COUNTER REGISTER 1 HIGH (CNTR1H)
Read only
Reset Value: 0000 0000 (00h)

15							8
0	0	0	0	CNTR1_11	CNTR1_10	CNTR1_9	CNTR1_8

COUNTER REGISTER 1 LOW (CNTR1L)
Read only
Reset Value: 0000 0000 (00h)

7							0
CNTR1_7	CNTR1_6	CNTR1_5	CNTR1_4	CNTR1_3	CNTR1_2	CNTR1_1	CNTR1_0

Bits 15:12 = Reserved.

Bits 11:0 = **CNTR1[11:0]** *Counter Value*.
This 12-bit register is read by software and cleared by hardware after a reset. The counter CNTR1 increments continuously as soon as a counter clock is selected. To obtain the 12-bit value, software should read the counter value in two consecutive read operations. As there is no latch, it is recommended to read LSB first. In this case, CNTR1H can be incremented between the two read operations and to have an accurate result when $f_{timer}=f_{CPU}$, special care must be taken when CNTR1L values close to FFh are read.
When a counter overflow occurs, the counter restarts from the value specified in the ATR1 register.

DUAL 12-BIT AUTORELOAD TIMER 4 (Cont'd)

Bits 11:0 = **ICR[11:0]** *Input Capture Data*.
This is a 12-bit register which is readable by software and cleared by hardware after a reset. The ATICR register contains captured the value of the 12-bit CNTR1 register when a rising or falling edge occurs on the ATIC or LTIC pin (depending on

ICS). Capture will only be performed when the ICF flag is cleared.

BREAK ENABLE REGISTER (BREAKEN)

Read/Write
Reset Value: 0000 0011 (03h)

7							0
0	0	0	0	0	0	BREN2	BREN1

Bits 7:2 = Reserved, must be kept cleared.

Bit 1 = **BREN2** *Break Enable for Counter 2*
This bit is read/write by software. It enables the break functionality for Counter2 if BA bit is set in BREAKCR. It controls PWM2/3 if ENCNTR2 bit is set.
0: No Break applied for CNTR2
1: Break applied for CNTR2

Bit 0 = **BREN1** *Break Enable for Counter 1*
This bit is read/write by software. It enables the break functionality for Counter1. If BA bit is set, it controls PWM0/1 by default, and controls PWM2/3 also if ENCNTR2 bit is reset.
0: No Break applied for CNTR1
1: Break applied for CNTR1

TIMER CONTROL REGISTER2 (ATCSR2)
Read/Write
Reset Value: 0000 0011 (03h)

7							0
FORCE 2	FORCE 1	ICS	OVFIE2	OVF2	ENCNT R2	TRAN2	TRAN1

Bit 7 = **FORCE2** *Force Counter 2 Overflow*
This bit is read/set by software. When set, it loads FFFh in the CNTR2 register. It is reset by hardware one CPU clock cycle after counter 2 overflow has occurred.

0 : No effect on CNTR2
1 : Loads FFFh in CNTR2

Note: This bit must not be reset by software

Bit 6 = **FORCE1** *Force Counter 1 Overflow*
This bit is read/set by software. When set, it loads FFFh in CNTR1 register. It is reset by hardware one CPU clock cycle after counter 1 overflow has occurred.

0 : No effect on CNTR1
1 : Loads FFFh in CNTR1

Note: This bit must not be reset by software

Bit 5 = **ICS** *Input Capture Shorted*
This bit is read/write by software. It allows the AT-timer CNTR1 to use the LTIC pin for long input capture.
0 : ATIC for CNTR1 input capture
1 : LTIC for CNTR1 input capture

Bit 4 = **OVFIE2** *Overflow interrupt 2 enable*
This bit is read/write by software and controls the overflow interrupt of counter2.
0: Overflow interrupt disabled.
1: Overflow interrupt enabled.

Bit 3 = **OVF2** *Overflow Flag.*
This bit is set by hardware and cleared by software by reading the ATCSR2 register. It indicates the transition of the counter2 from FFFh to ATR2 value.
0: No counter overflow occurred
1: Counter overflow occurred

Bit 2 = **ENCNTR2** *Enable counter2* for PWM2/3

This bit is read/write by software and switches the PWM2/3 operation to the CNTR2 counter. If this bit is set, PWM2/3 will be generated using CNTR2.
0: PWM2/3 is generated using CNTR1.
1: PWM2/3 is generated using CNTR2.

Note: Counter 2 gets frozen when the ENCNTR2 bit is reset. When ENCNTR2 is set again, the counter will restart from the last value.

LITE TIMER (Cont'd)

Bit 6 = **ICF** *Input Capture Flag*
This bit is set by hardware and cleared by software by reading the LTICR register. Writing to this bit does not change the bit value.
0: No input capture
1: An input capture has occurred

Note: After an MCU reset, software must initialize the ICF bit by reading the LTICR register

Bit 5 = **TB** *Timebase period selection*
This bit is set and cleared by software.
0: Timebase period = t_{OSC} * 8000 (1ms @ 8 MHz)
1: Timebase period = t_{OSC} * 16000 (2ms @ 8 MHz)

Bit 4 = **TB1IE** *Timebase Interrupt enable*
This bit is set and cleared by software.
0: Timebase (TB1) interrupt disabled
1: Timebase (TB1) interrupt enabled

Bit 3 = **TB1F** *Timebase Interrupt Flag*
This bit is set by hardware and cleared by software reading the LTCSR register. Writing to this bit has no effect.
0: No counter overflow
1: A counter overflow has occurred

Bits 2:0 = Reserved

LITE TIMER INPUT CAPTURE REGISTER (LTICR)
Read only
Reset Value: 0000 0000 (00h)

7							0
ICR7	ICR6	ICR5	ICR4	ICR3	ICR2	ICR1	ICR0

Bits 7:0 = **ICR[7:0]** *Input Capture Value*
These bits are read by software and cleared by hardware after a reset. If the ICF bit in the LTCSR is cleared, the value of the 8-bit up-counter will be captured when a rising or falling edge occurs on the LTIC pin.

LITE TIMER (Cont'd)

Table 15. Lite Timer Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
08	**LTCSR2** Reset Value	0	0	0	0	0	0	TB2IE 0	TB2F 0
09	**LTARR** Reset Value	AR7 0	AR6 0	AR5 0	AR4 0	AR3 0	AR2 0	AR1 0	AR0 0
0A	**LTCNTR** Reset Value	CNT7 0	CNT6 0	CNT5 0	CNT4 0	CNT3 0	CNT2 0	CNT1 0	CNT0 0
0B	**LTCSR1** Reset Value	ICIE 0	ICF x	TB 0	TB1IE 0	TB1F 0	0	0	0
0C	**LTICR** Reset Value	ICR7 0	ICR6 0	ICR5 0	ICR4 0	ICR3 0	ICR2 0	ICR1 0	ICR0 0

ON-CHIP PERIPHERALS (cont'd)

11.4 SERIAL PERIPHERAL INTERFACE (SPI)

11.4.1 Introduction

The Serial Peripheral Interface (SPI) allows full-duplex, synchronous, serial communication with external devices. An SPI system may consist of a master and one or more slaves or a system in which devices may be either masters or slaves.

11.4.2 Main Features

- Full duplex synchronous transfers (on three lines)
- Simplex synchronous transfers (on two lines)
- Master or slave operation
- 6 master mode frequencies (f_{CPU}/4 max.)
- f_{CPU}/2 max. slave mode frequency (see note)
- $\overline{SS}$ Management by software or hardware
- Programmable clock polarity and phase
- End of transfer interrupt flag
- Write collision, Master Mode Fault and Overrun flags

Note: In slave mode, continuous transmission is not possible at maximum frequency due to the software overhead for clearing status flags and to initiate the next transmission sequence.

11.4.3 General Description

Figure 1 on page 3 shows the serial peripheral interface (SPI) block diagram. There are three registers:

- SPI Control Register (SPICR)
- SPI Control/Status Register (SPICSR)
- SPI Data Register (SPIDR)

The SPI is connected to external devices through four pins:

- MISO: Master In / Slave Out data
- MOSI: Master Out / Slave In data
- SCK: Serial Clock out by SPI masters and input by SPI slaves
- $\overline{SS}$: Slave select:
  This input signal acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave $\overline{SS}$ inputs can be driven by standard I/O ports on the master Device.

ANALOG COMPARATOR (Cont'd)

Bit 4 = **CMPIF** *Comparator Interrupt Flag*

This bit is set by hardware when interrupt is generated at the rising edge (CINV = 0) or falling edge (CINV = 1) of comparator output. This bit is cleared by reading the CMPCR register. Writing to this bit does not change the value.
0 : Comparator interrupt flag cleared
1 : Comparator interrupt flag set and can generate interrupt if CMPIE is set.

Bit 3 : **CMPIE** *Comparator Interrupt Enable*

This bit is set or reset by software and cleared by hardware reset. This bit enables or disables the interrupt generation depending on interrupt flag
0: Interrupt not generated
1: Interrupt generated if interrupt flag is set

Note:

This bit should be set to enable interrupt only after the comparator has been switched ON, i.e. when CMPON is set.

Once CMPON bit is set, it is recommended to wait the specified stabilization time before setting CMPIE bit in order to avoid a spurious interrupt (see section 13.12 on page 143).

Bit 2 : **CMP** *Comparator Output*

This bit is set or reset by software and cleared by hardware reset. It stores the value of comparator output.

Bit 1 = **COUT** *Comparator Output Enable on Port*
This bit is set or cleared by software. When this bit is set, the comparator output is available on PA7 port.
0 : Comparator output not connected to PA7
1 : Comparator output connected to PA7

Bit 0 : **CMPON** *Comparator ON/OFF*
This bit is set or cleared by software and reset by hardware reset. This bit is used to switch ON/OFF the comparator, internal voltage reference and current bias which provides 4µA current to both.
0: Comparator, Internal Voltage Reference, Bias OFF (in power-down state).
1: Comparator, Internal Voltage Reference, Bias ON

Note: For the comparator interrupt generation, it takes 250ns delay from comparator output change to rising or falling edge of interrupt generated.

Table 21. Analog Comparator Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
002Ch	**VREFCR**	VCEXT	VCBGR	VR3	VR2	VR1	VR0	-	-
	Reset Value	0	0	0	0	0	0	0	0
002Dh	**CMPCR**	CHYST	-	CINV	CMPIF	CMPIE	CMP	COUT	CMPON
	Reset value	1	0	0	0	0	0	0	0

13.3 OPERATING CONDITIONS

13.3.1 General Operating Conditions: Suffix 6 Devices

T_A = -40 to +85°C unless otherwise specified.

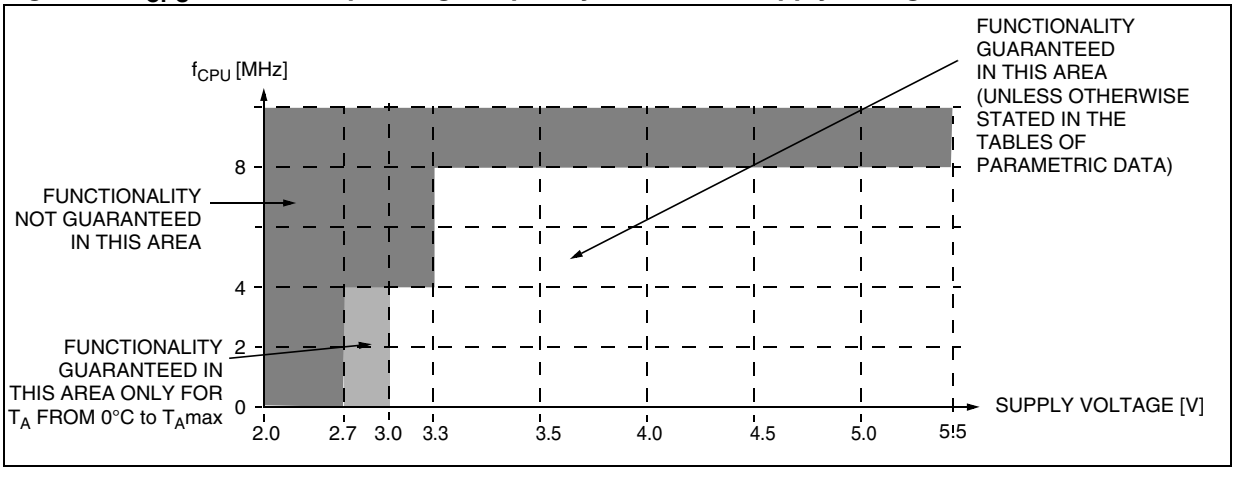
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	f_{CPU} = 4 MHz. max., T_A = 0 to 85°C	2.7	5.5	V
		f_{CPU} = 4 MHz. max.,T_A = -40 to 85°C	3.0	5.5	
		f_{CPU} = 8 MHz. max.	3.3	5.5	
f_{CPU}	CPU clock frequency	$V_{DD} \geq 3.3V$	up to 8		MHz
		$2.7V \leq V_{DD} < 3.3V$	up to 4		

13.3.2 General Operating Conditions: Suffix 3 Devices

T_A = -40 to +125°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage	f_{CPU} = 4 MHz. max., T_A = 0 to 125°C	2.7	5.5	V
		f_{CPU} = 4 MHz. max.,T_A = -40 to 125°C	3.0	5.5	
		f_{CPU} = 8 MHz. max.	3.3	5.5	
f_{CPU}	CPU clock frequency	$V_{DD} \geq 3.3V$	up to 8		MHz
		$2.7V \leq V_{DD} < 3.3V$	up to 4		

Figure 65. f_{CPU} Maximum Operating Frequency Versus V_{DD} Supply Voltage



EMC CHARACTERISTICS (Cont'd)

13.7.3 Absolute Maximum Ratings (Electrical Sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

13.7.3.1 Electro-Static Discharge (ESD)

Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: Human Body Model and Machine Model. This test conforms to the JESD22-A114A/A115A standard.

Absolute Maximum Ratings

Symbol	Ratings	Conditions	Maximum value [1]	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	8000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)	T_A=+25°C	400	

Note:

1. Data based on characterization results, not tested in production.

13.7.3.2 Static Latch-Up

- **LU**: 3 complementary static tests are required on 6 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Electrical Sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A=+25°C T_A=+85°C	A A

COMMUNICATION INTERFACE CHARACTERISTICS (Cont'd)

Figure 108. SPI Slave Timing Diagram with CPHA=1 [1)]

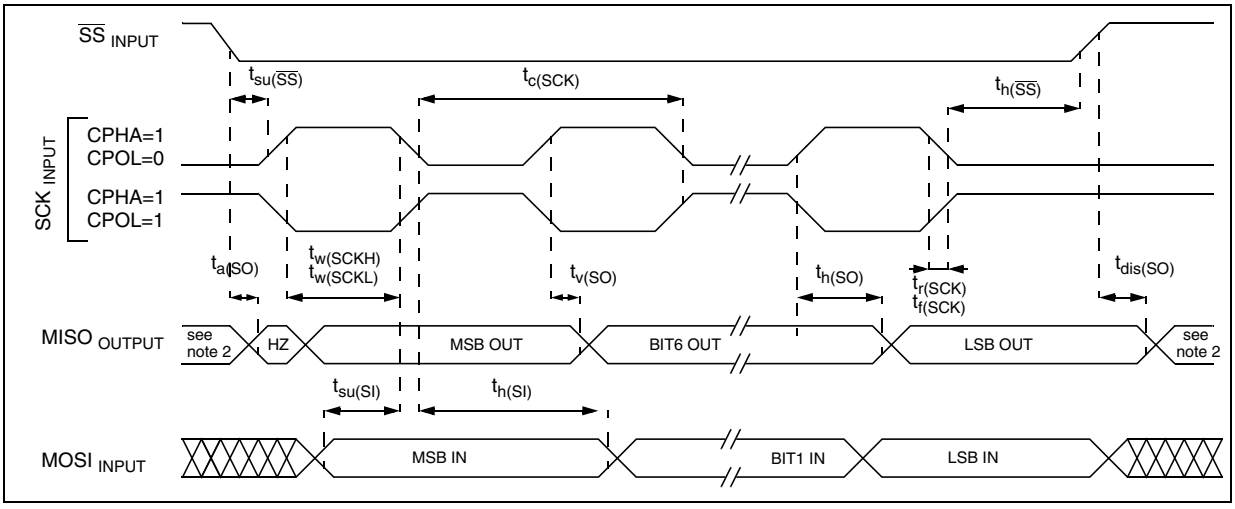
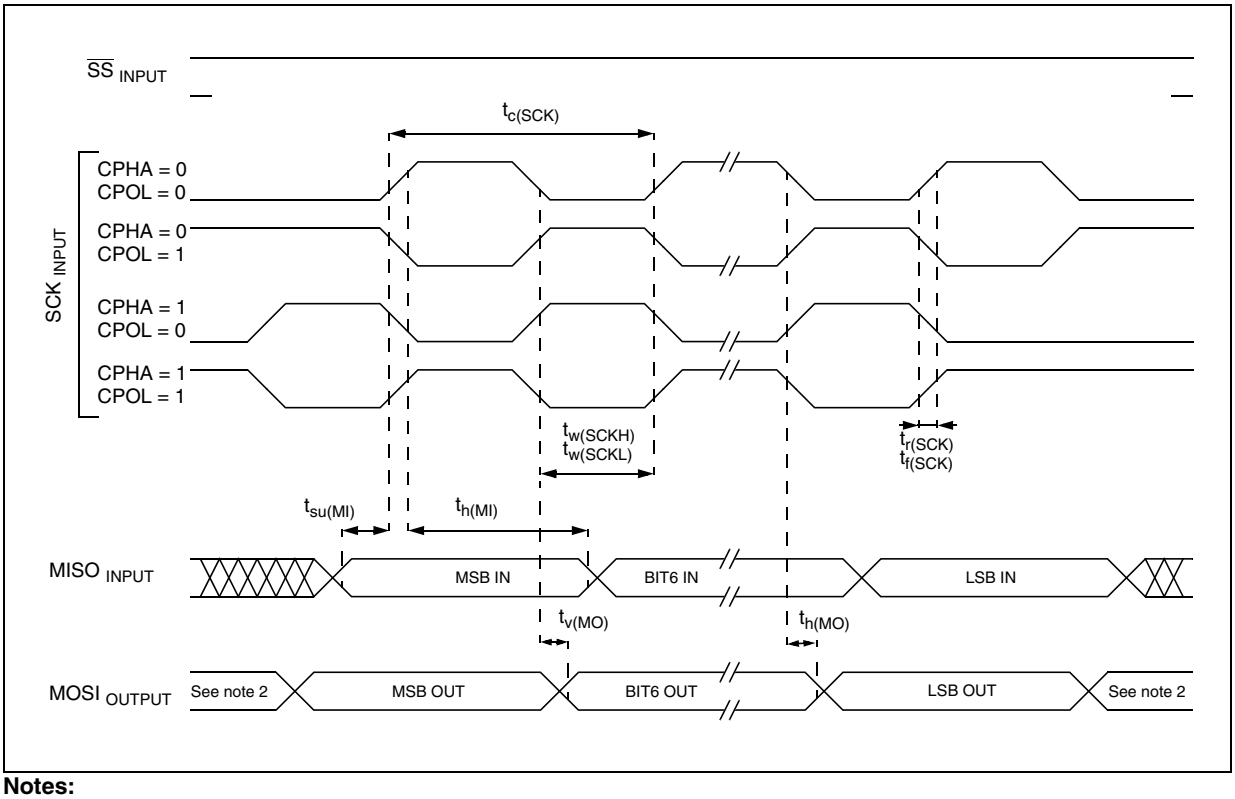


Figure 109. SPI Master Timing Diagram [1)]



Notes:

1. Measurement points are done at CMOS levels: $0.3xV_{DD}$ and $0.7xV_{DD}$.

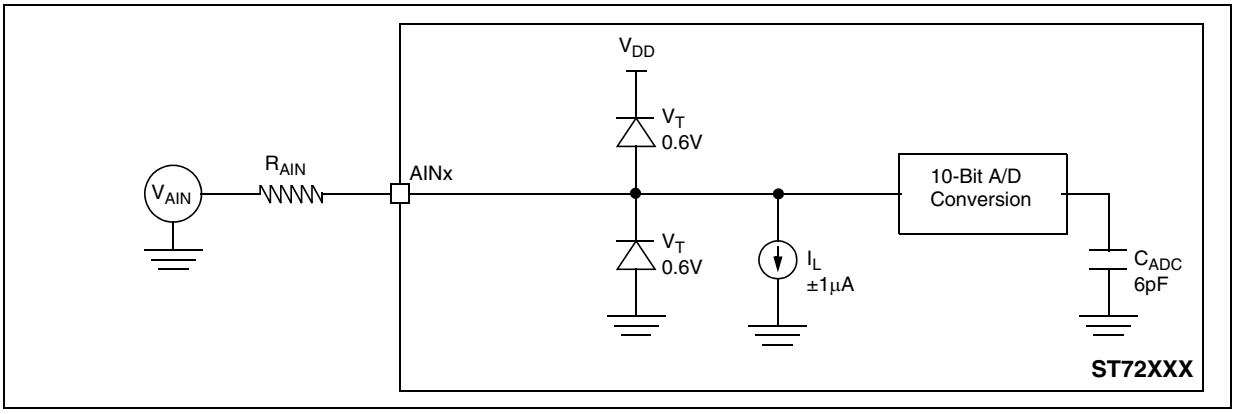
2. When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends of the I/O port configuration.

13.11 10-BIT ADC CHARACTERISTICS

Subject to general operating condition for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
f_{ADC}	ADC clock frequency				4	MHz
V_{AIN}	Conversion voltage range [2]		V_{SSA}		V_{DDA}	V
R_{AIN}	External input resistor				10 [3]	kΩ
C_{ADC}	Internal sample and hold capacitor			6		pF
t_{STAB}	Stabilization time after ADC enable	f_{CPU}=8MHz, f_{ADC}=4MHz	0 [4]			µs
t_{ADC}	Conversion time (Sample+Hold)		3.5			
	- Sample capacitor loading time - Hold conversion time		4 10			$1/f_{ADC}$
I_{ADC}	Analog Part			1		mA
	Digital Part			0.2		

Figure 110. Typical Application with ADC



Notes:

1. Unless otherwise specified, typical data are based on T_A=25°C and V_{DD}-V_{SS}=5V. They are given only as design guidelines and are not tested.

2. When V_{DDA} and V_{SSA} pins are not available on the pinout, the ADC refers to V_{DD} and V_{SS}.

3. Any added external serial resistor will downgrade the ADC accuracy (especially for resistance greater than 10kΩ). Data based on characterization results, not tested in production.

4. The stabilization time of the AD converter is masked by the first t_{LOAD}. The first conversion after the enable is then always valid.

Related application notes:

Understanding and minimizing ADC conversion errors (AN1636)

Software techniques for compensating ST7 ADC errors (AN1711)

OPTION BYTES (Cont'd)

OPTION BYTE 1

OPT7 = **PLLx4x8** *PLL Factor selection.*
0: PLLx4
1: PLLx8

OPT6 = **PLLOFF** *PLL disable.*
0: PLL enabled
1: PLL disabled (by-passed)

OPT5 = **PLL32OFF** *32MHz PLL disable.*
0: PLL32 enabled
1: PLL32 disabled (by-passed)

OPT4 = **OSC** *RC Oscillator selection*
0: RC oscillator on
1: RC oscillator off

Notes:

– 1% RC oscillator available on ST7LITE15B and ST7LITE19B devices only

– If the RC oscillator is selected, then to improve clock stability and frequency accuracy, it is recommended to place a decoupling capacitor, typically 100nF, between the V_{DD} and V_{SS} pins as close as possible to the ST7 device.

OPT3:2 = **LVD[1:0]** *Low voltage detection selection*
These option bits enable the LVD block with a selected threshold as shown in Table 26.

Table 26. LVD Threshold Configuration

Configuration	LVD1	LVD0
LVD Off	1	1
Highest Voltage Threshold (~4.1V)	1	0
Medium Voltage Threshold (~3.5V)	0	1
Lowest Voltage Threshold (~2.8V)	0	0

OPT1 = **WDG SW** *Hardware or Software Watchdog*
This option bit selects the watchdog type.
0: Hardware (watchdog always enabled)
1: Software (watchdog to be enabled by software)

OPT0 = **WDG HALT** *Watchdog Reset on Halt*
This option bit determines if a RESET is generated when entering HALT mode while the Watchdog is active.
0: No Reset generation when entering Halt mode
1: Reset generation when entering Halt mode

Table 27. List of valid option combinations

Operating conditions				Option Bits		
V_{DD} range	Clock Source	PLL	Typ f_{CPU}	OSC	PLLOFF	PLLx4x8
2.7V - 3.3V	Internal RC 1%[1)]	off	1MHz @3.3V	0	1	1
		x4	4MHz @3.3V	0	0	0
		x8	-	-	-	-
	External clock	off	0-4MHz	1	1	1
		x4	4MHz	1	0	0
		x8	-	-	-	-
3.3V - 5.5V	Internal RC 1% [1)]	off	1MHz @5V	0	1	1
		x4	-	-	-	-
		x8	8MHz @5V	0	0	1
	External clock	off	0-8MHz	1	1	1
		x4	-	-	-	-
		x8	8 MHz	1	0	1

Note 1: Configuration available on ST7LITE15B and ST7LITE19B devices only

Note: see Clock Management Block diagram in Figure 14

ST7LITE1xB FASTROM microcontroller option list

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .
Reference/FASTROM Code*: . . . . . .
*FASTROM code name is assigned by STMicroelectronics.
FASTROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device Type/Memory Size/Package (check only one option):

FASTROM DEVICE:	2K	4K
VFQFPN20:	[ ] ST7PLIT19BF0Ux	[ ] ST7PLIT19BF1Ux
SO20:	[ ] ST7PLIT19BF0Mx	[ ] ST7PLIT19BF1Mx
PDIP20:	[ ] ST7PLIT19BF0Bx	[ ] ST7PLIT19BF1Bx
SO16:	[ ] ST7PLIT19BY0Mx	[ ] ST7PLIT19BY1Mx
PDIP16:	[ ] ST7PLIT19BY0Bx	[ ] ST7PLIT19BY1Bx

Warning: Addresses DEE0h, DEE1h, DEE2h and DEE3h are reserved areas for ST to program RCCR0 and RCCR1 (see section 7.1 on page 23).

Conditioning (check only one option, do not specify for DIP package) :

VFQFPN	[ ] Tape & Reel	[ ] Tray
SO	[ ] Tape & Reel	[ ] Tube

Special marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ "
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Maximum character count: 8 char. max _ _ _ _ _ _ _ _

Temperature range: [ ] -40°C to +85°C [ ] -40°C to +125°C

Watchdog selection (WDG_SW): [ ] Software activation [ ] Hardware activation

Watchdog reset on Halt (WDG_HALT): [ ] Reset [ ] No Reset

LVD reset (LVD): [ ] Disabled [ ] Enabled
[ ] Highest threshold
[ ] Medium threshold
[ ] Lowest threshold

Sector 0 size (SEC): [ ] 0.5K [ ] 1K [ ] 2K [ ] 4K

Readout protection (FMP_R): [ ] Disabled [ ] Enabled

Flash write protection (FMP_W): [ ] Disabled [ ] Enabled

RC oscillator (OSC) : [ ] Disabled [ ] Enabled

Clock source selection (CKSEL):
(if OSC disabled) [ ] External crystal / ceramic resonator:
[ ] External Clock on PB4
[ ] External Clock on PC0

PLL (PLLOFF): [ ] Disabled [ ] Enabled

PLL factor (PLLx4x8): [ ] PLLx4 [ ] PLLx8

PLL32 (PLL32OFF): [ ] Disabled [ ] Enabled

Comments : . . . . . .
Supply operating range in the application : . . . . . .
Notes . . . . . .
Date : . . . . . .
Signature : . . . . . .

Important note : Not all configurations are available. See Table 27 on page 150 for authorized option byte combinations.

16 REVISION HISTORY

Date	Revision	Main changes
20-Dec-05	1	Initial release on internet
20-July-06	2	Added reset default state in bold for RESET, PC0 and PC1 in Table 1, “Device Pin Description,” on page 7 Changed note below Figure 9 on page 17 and the last paragraph of “ACCESS ERROR HANDLING” on page 18 Modified note 3 in Table 2, “Hardware Register Map,” on page 10, changed LTICR reset value and replaced h by b for LTCSR1, ATCSR and SICSR reset values Added note to Figure 14 on page 26 Modified caution in section 7.2 on page 23 Added note 2 in “EXTERNAL INTERRUPT CONTROL REGISTER (EICR)” on page 38 and changed “External Interrupt Function” on page 48 Removed references to true open drain in Table 8 on page 50, Table 9 on page 51 and notes Replaced Auto reload timer 3 by Auto reload timer 4 in section 11.2 on page 57 Modified the BA bit description in the BREAKCR register in section 11.2.6 on page 70 Changed order of Section 11.3.3.2 and section 11.3.3.3 on page 80 and removed two paragraphs before section 11.3.4 on page 81 Modified Section 11.3.3.2 Modified bit names in the description of LTARR and LTCNTR registers in section 11.3.6 on page 81 Added important note in section 11.6.3 on page 100 and added note to CHYST bit description in section 11.6.4 on page 102 Modified CINV bit description in section 11.6.4 on page 102 and Figure 62 on page 101 Changed LTCSR2 reset values in Table 2 on page 10 and in section 11.3.6 on page 81 Modified section 13.2.2 on page 111 (I_{IO} values) Modified Section 13.3.1 and section 13.3.2 on page 112 Removed Vt_{POR} min value in section 13.3.3.1 on page 113 Modified section 13.3.4 on page 114 Modified section 13.3.5 on page 114 Modified section 13.3.5.1 on page 115 and section 13.3.5.2 on page 117 Modified temperature range in section 13.3.5.3 on page 119 Modified section 13.4.1 on page 121 Added note in section 13.5.3 on page 124 Removed figures “PLLx4 and PLLx8 Output vs CLKIN frequency” Updated section 13.5.4 on page 125 Modified section 13.6 on page 126 Modified Section 13.7.1 and section 13.7.2 on page 127 Modified section 13.10.1 on page 137 ($t_{su(\overline{SS})}$, $t_{v(MO)}$ and $t_{h(MO)}$) Modified Figure 108 (CPHA=1) and Figure 109 on page 138 ($t_{v(MO)}$, $t_{h(MO)}$) Removed empty figure “Typical I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$” in section 13.8.1 on page 129 and modified note 3 Modified temperature range in section 13.8.2 on page 130 Modified section 13.9.1 on page 135 Added “related Application notes” in section 13.11 on page 139 Removed EMC protection circuitry in Figure 106 on page 136 (device works correctly without these components) Modified ADC accuracy table in section 13.11 on page 139 Modified temperature range in Section 13.12, Section 13.13 and section 13.14 on page 143 Modified Table 27 on page 150 Added note 3 to E_D and E_L in Table “ADC Accuracy with VDD=5.0V” on page 140 Modified section 14.2 on page 148 Modified section 15.2 on page 151 (part numbers in QFN20 package) Updated section 15.3 on page 153
15-Sept-06	3	Removed QFN20 pinout and mechanical data. Modified description of CNTR[11:0] bits in section 11.2.6 on page 72 Added “External Clock Source” on page 124 and Figure 78 on page 124 Modified Table 1.