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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c240093-24ltxi

PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The Core
- Analog System
- System Resources (including a full-speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Depending on the PSoC package, up to 36 GPIO are included in the CY8C24x93 PSoC device. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

Analog system

The analog system is composed of an ADC, two comparators and an IDAC. It has an internal 0.8 V, 1 V or 1.2 V analog reference. All the pins can be configured to connect to the analog system.

ADC

The ADC in the CY8C24x93 device is an incremental analog-to-digital converter with a range of 8 to 10 bits supporting signed and unsigned data formats. The input to the ADC can be from any pin.

IDAC

The IDAC can provide current source up to 512 µA to any GPIO pin. In the CY8C24x93 family of devices 4 ranges of current source can be implemented that can vary in 255 steps, and are connected to analog mux bus.

Table 1. IDAC Ranges

Range	Full Scale Range in µA
1x	64
2x	128
4x	256
8x	512

Comparator

The CY8C24x93 family has two high-speed, low-power comparators. The comparators have three voltage references, 0.8 V, 1.0 V and 1.2 V. Comparator inputs can be connected from any pin through the analog mux bus. The comparator output can be read in firmware for processing or routed out via specific pins (P1_0 or P1_4).

The output of the two comparators can be combined with 2-input logic functions. The combinatorial output can be optionally combined with a latched value and routed to a pin output or to the interrupt controller. The input multiplexers and the comparator are controller through the CMP User Module.

Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin and can be internally connected to the ADC, Comprators or the IDAC.

Other multiplexer applications include:

- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Additional System Resources

System resources provide additional capability, such as configurable USB and I2C slave, SPI master/slave communication interface, three 16-bit programmable timers, software 8-bit PWM, low voltage detect, power on reset, and various system resets supported by the M8C.

The merits of each system resource are listed here:

- The I^2C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- A register-controlled bypass mode allows the user to disable the LDO regulator.
- An 8-bit Software PWM is provided for applications like buzzer control or lighting control. A 16-bit Timer acts as the input clock to the PWM. The ISR increments a software counter (8-bit), checks for PWM compare condition and toggles a GPIO accordingly. PWM Output is available on all GPIOs.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

10. Select user modules.
11. Configure user modules.
12. Organize and connect.
13. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

Pinouts

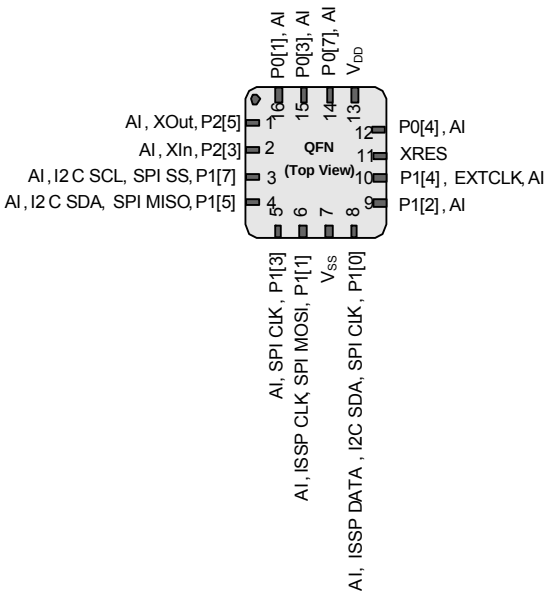
16-pin QFN (13 GPIOs) [2]

Table 2. Pin Definitions – CY8C24093 [3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I^2C SCL, SPI SS
4	IOHR	I	P1[5]	I^2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK[4], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	IOHR	I	P1[0]	ISSP DATA[4], I^2C SDA, SPI CLK[5]
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	IOH	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	
16	IOH	I	P0[1]	

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C24093 Device



Notes
2. No center pad.
3. 13 GPIOs.
4. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
5. Alternate SPI clock.

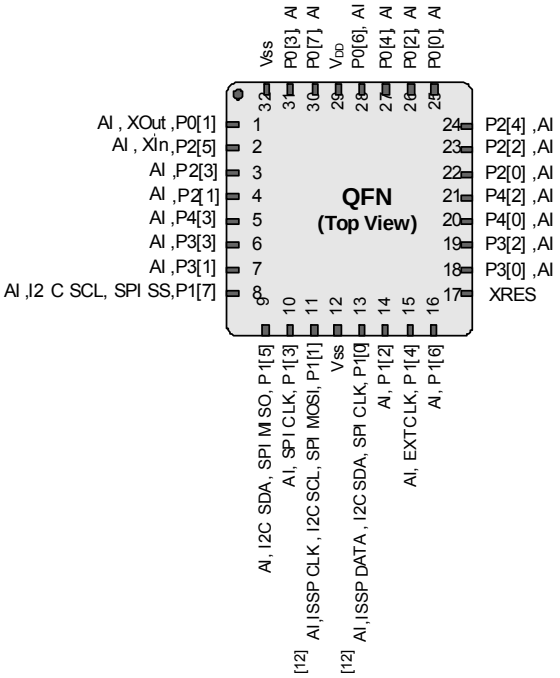
32-pin QFN (28 GPIOs) [10]

Table 4. Pin Definitions – CY8C24293 [11]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[1]	
2	I/O	I	P2[5]	Crystal output (XOut)
3	I/O	I	P2[3]	Crystal input (XIn)
4	I/O	I	P2[1]	
5	I/O	I	P4[3]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK [12], I^2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection
13	IOHR	I	P1[0]	ISSP DATA[12], I^2C SDA, SPI CLK[13]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P4[0]	
21	I/O	I	P4[2]	
22	I/O	I	P2[0]	
23	I/O	I	P2[2]	
24	I/O	I	P2[4]	
25	IOH	I	P0[0]	
26	IOH	I	P0[2]	
27	IOH	I	P0[4]	
28	IOH	I	P0[6]	
29	Power		V_{DD}	
30	IOH	I	P0[7]	
31	IOH	I	P0[3]	
32	Power		V_{SS}	Ground connection
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 4. CY8C24293 Device



Notes

10. 28 GPIOs.
11. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
12. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
13. Alternate SPI clock.

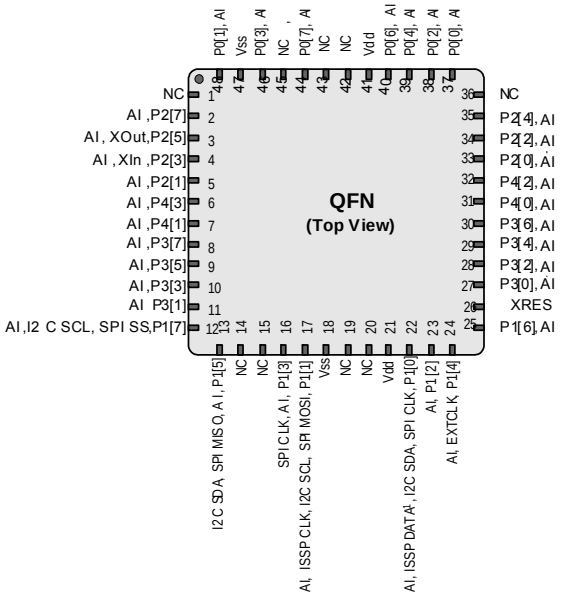
48-pin QFN (34 GPIOs) [14]

Table 5. Pin Definitions – CY8C24393, CY8C24693 [15, 16]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[17], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection
19			NC	No connection
20			NC	No connection
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[17], I^2C SDA, SPI CLK[18]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36			NC	No connection
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45			NC	No connection
46	IOH	I	P0[3]	
47	Power		V_{SS}	Ground connection
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 5. CY8C24393, CY8C24693 Device



Notes

14. 38 GPIOs.
15. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
16. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
17. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
18. Alternate SPI clock.

AC Chip-Level Specifications (CY8C24193/493)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

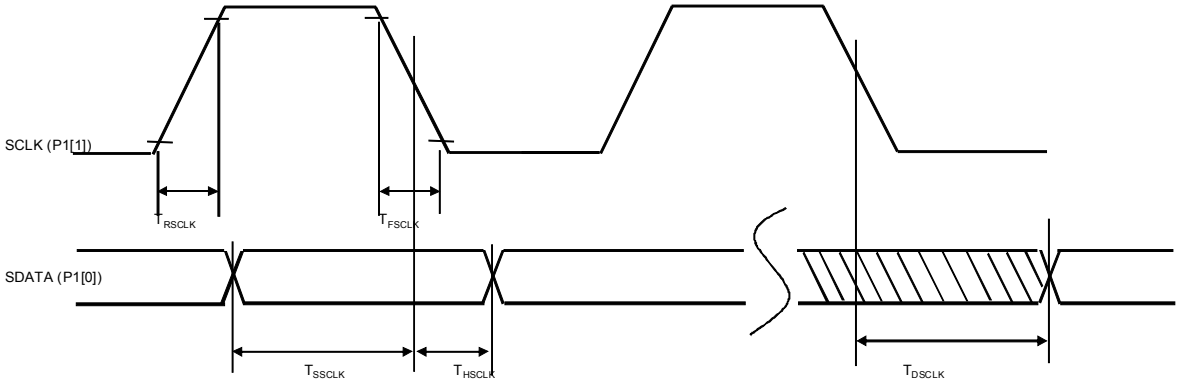
Table 25. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F_{IMO12}	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F_{IMO6}	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency	–	0.75	–	25.20	MHz
F_{32K1}	ILO frequency	–	15	32	50	kHz
F_{32K_U}	ILO untrimmed frequency	–	13	32	82	kHz
DC_{IMO}	Duty cycle of IMO	–	40	50	60	%
DC_{ILO}	ILO duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	V_{DD} slew rate during power-up	–	–	250	V/ms
t_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t_{XRST2}	External reset pulse width after power-up[50]	Applies after part has booted	10	–	–	µs
t_{JIT_IMO}[39]	6 MHz IMO cycle-to-cycle jitter (RMS)	–	–	0.7	6.7	ns
	6 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	4.3	29.3	ns
	6 MHz IMO period jitter (RMS)	–	–	0.7	3.3	ns
	12 MHz IMO cycle-to-cycle jitter (RMS)	–	–	0.5	5.2	ns
	12 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	2.3	5.6	ns
	12 MHz IMO period jitter (RMS)	–	–	0.4	2.6	ns
	24 MHz IMO cycle-to-cycle jitter (RMS)	–	–	1.0	8.7	ns
	24 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	1.4	6.0	ns
	24 MHz IMO period jitter (RMS)	–	–	0.6	4.0	ns

Note
38. The minimum required XRES pulse length is longer when programming the device (see Table 55 on page 42).
39. See the Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

AC Programming Specifications (CY8C24193/493)

Figure 10. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
t_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	–	40	–	–	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
t_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
t_{WRITE}	Flash block write time	–	–	–	25	ms
t_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \le V_{DD} \le 3.0$	–	–	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	µs
t_{XRES}	XRES pulse length	–	300	–	–	µs
$t_{VDDWAIT}$	V_{DD} stable to wait-and-poll hold off	–	0.1	–	1	ms
$t_{VDDXRES}$	V_{DD} stable to XRES assertion delay	–	14.27	–	–	ms
t_{POLL}	SDAT high pulse time	–	0.01	–	200	ms
t_{ACQ}	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
$t_{XRESINI}$	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	µs

Table 31. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	60 100	– –	– –	ns ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_H}	MOSI high time	–	40	–	–	ns

Figure 12. SPI Master Mode 0 and 2

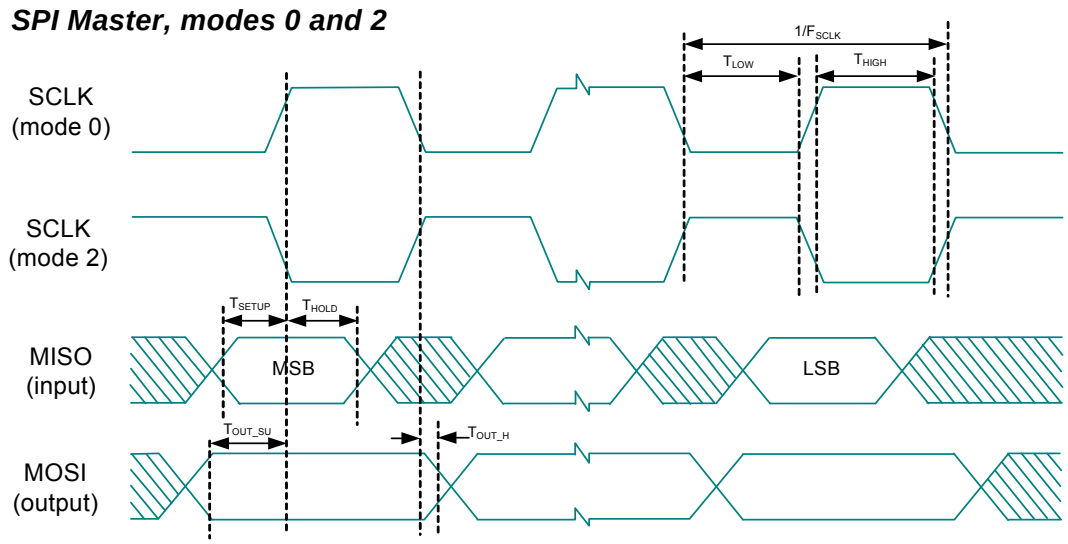
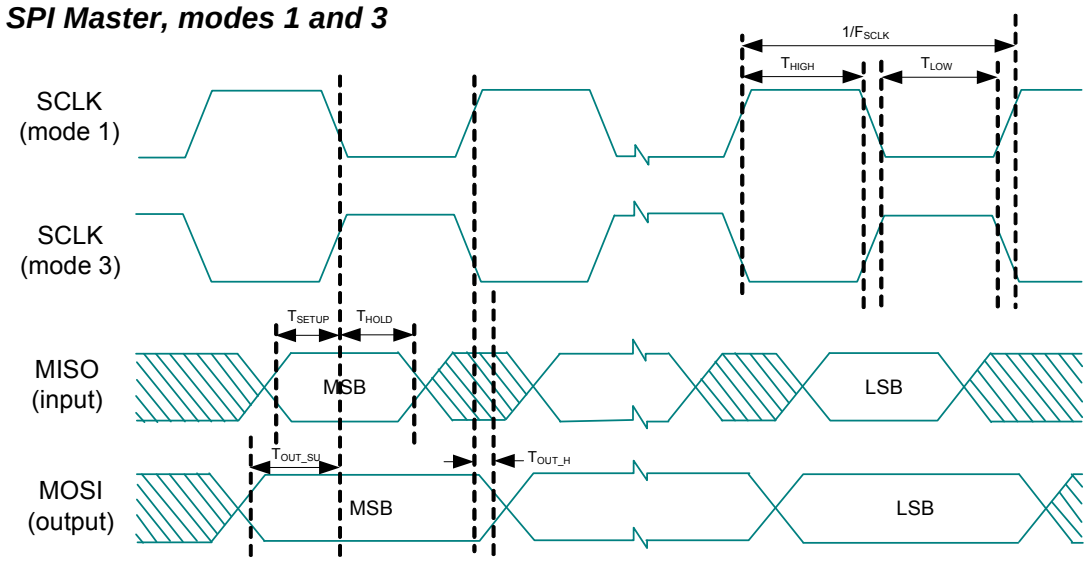


Figure 13. SPI Master Mode 1 and 3



Comparator User Module Electrical Specifications (CY8C24093/293/393/693)

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ T_A ≤ 85 °C, 1.71 V ≤ V_{DD} ≤ 5.5 V.

Table 42. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to V_{DD} – 0.2 V	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	µA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0		1.5	V

ADC Electrical Specifications (CY8C24093/293/393/693)

Table 43. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	VREFADC	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^Resolution/Data Clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2^resolution/data clock)	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V_{DD} > 3.0 V)	–	24	–	dB
		PSRR (V_{DD} < 3.0 V)	–	30	–	dB

AC GPIO Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 50. AC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode Port 0, 1	0 0	– –	6 MHz for 1.71 V <V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD}< 5.50 V	MHz MHz
t_{RISE23}	Rise time, strong mode, Cload = 50 pF Port 2 or 3 or 4 pins	V_{DD} = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
$t_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, Port 2 or 3 or 4 pins	V_{DD} = 1.71 to 3.0 V, 10% to 90%	15	–	80	ns
t_{RISE01}	Rise time, strong mode, Cload = 50 pF Ports 0 or 1	V_{DD} = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
$t_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	V_{DD} = 1.71 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
t_{FALL}	Fall time, strong mode, Cload = 50 pF all ports	V_{DD} = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
t_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	V_{DD} = 1.71 to 3.0 V, 10% to 90%	10	–	70	ns

Figure 17. GPIO Timing Diagram

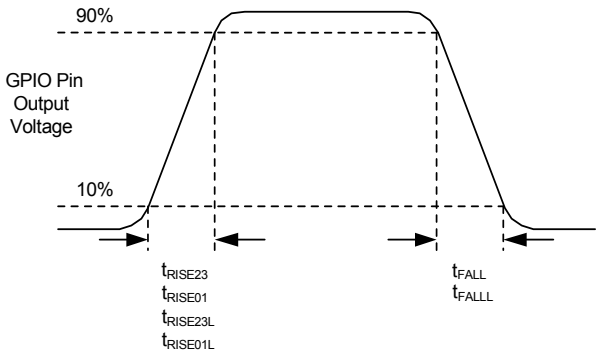


Table 51. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DRATE}	Full speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
t_{JR1}	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
t_{JR2}	Receiver jitter tolerance	To pair transition	–9.0	–	9	ns
t_{DJ1}	FS Driver jitter	To next transition	–3.5	–	3.5	ns
t_{DJ2}	FS Driver jitter	To pair transition	–4.0	–	4.0	ns
t_{FDEOP}	Source jitter for differential transition	To SE0 transition	–2.0	–	5	ns
t_{FEOPT}	Source SE0 interval of EOP	–	160.0	–	175	ns
t_{FEOPR}	Receiver SE0 interval of EOP	–	82.0	–	–	ns
t_{FST}	Width of SE0 interval during differential transition	–	–	–	14	ns

Table 52. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{FR}	Transition rise time	50 pF	4	–	20	ns
t_{FF}	Transition fall time	50 pF	4	–	20	ns
t_{FRFM}[52]	Rise/fall time matching	–	90	–	111	%
V_{CRS}	Output signal crossover voltage	–	1.30	–	2.00	V

AC Comparator Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 53. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

AC External Clock Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 54. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	µs

Note

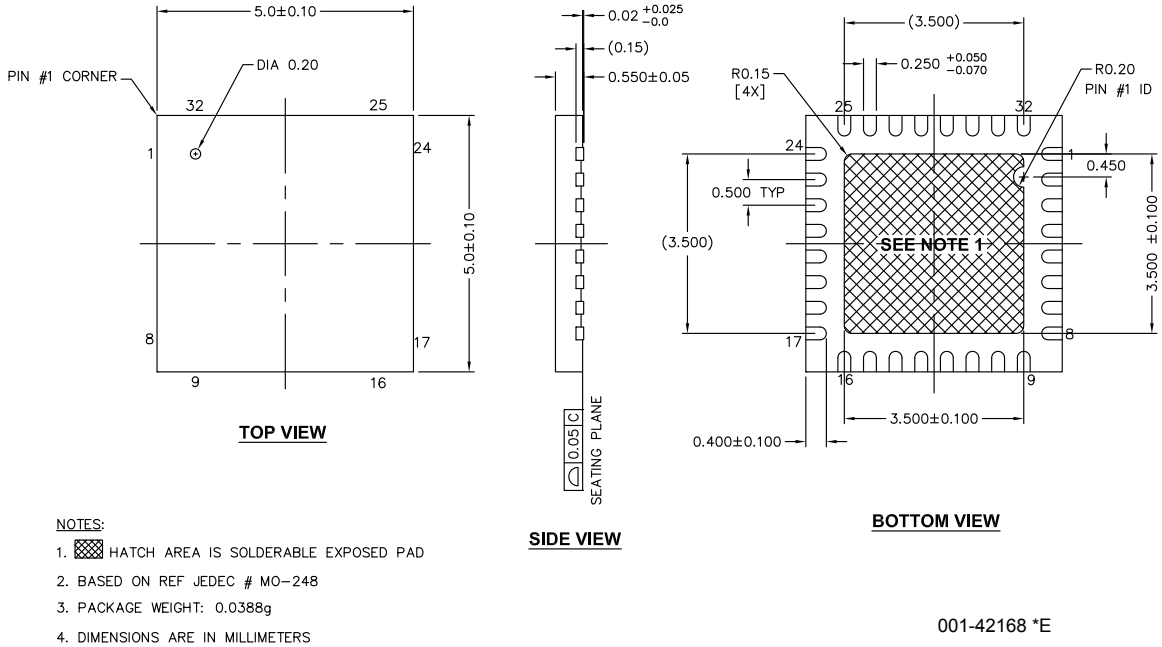
52. T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.

Packaging Information

This section illustrates the packaging specifications for the CY8C24X93 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

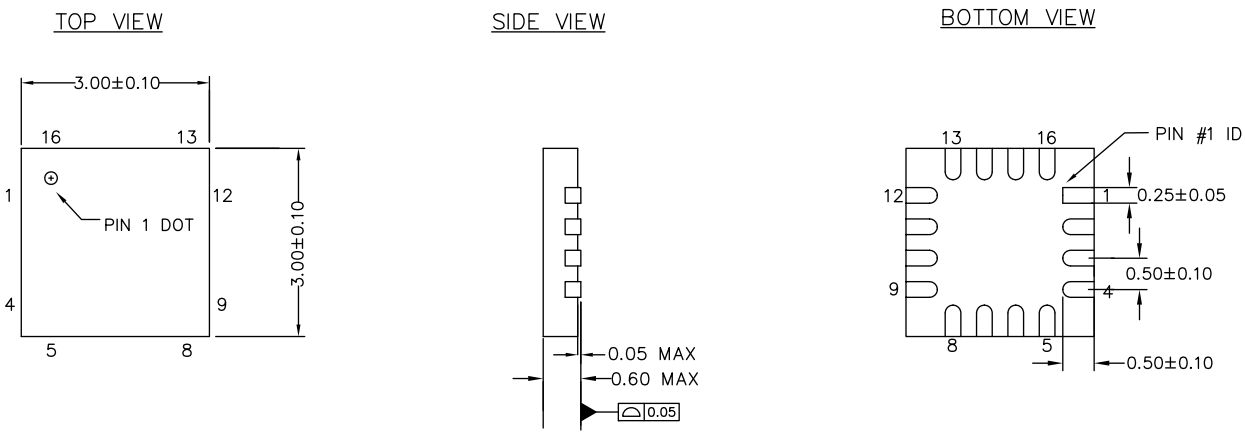
Figure 24. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

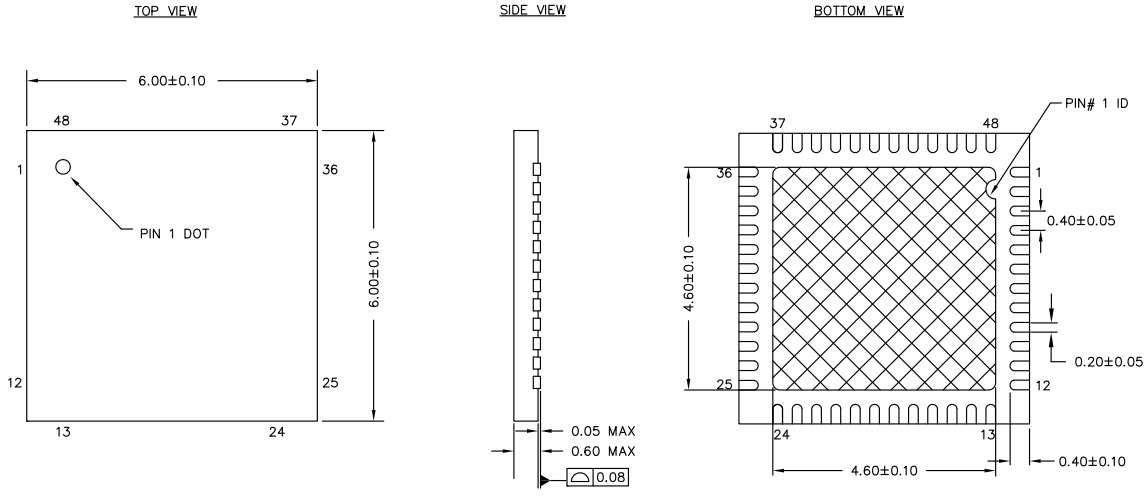
Figure 25. 16-pin Chip On Lead (3 × 3 × 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116



NOTES
1. REFERENCE JEDEC # MO−220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Figure 26. 48-pin QFN (6 × 6 × 0.6 mm) LQ48A 4.6 × 4.6 E-Pad (Sawn) Package Outline, 001-57280



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT: 68 ±7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Acronyms

Table 63. Acronyms Used in this Document

Acronym	Description
AC	Alternating Current
ADC	Analog-to-Digital Converter
API	Application Programming Interface
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DC	Direct Current
EOP	End Of Packet
FSR	Full Scale Range
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
I^2C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
IDAC	Digital Analog Converter Current
ILO	Internal Low Speed Oscillator
IMO	Internal Main Oscillator
I/O	Input/Output
ISSP	In-System Serial Programming
LCD	Liquid Crystal Display
LDO	Low Dropout (regulator)
LSB	Least-Significant Bit
LVD	Low Voltage Detect
MCU	Micro-Controller Unit
MIPS	Mega Instructions Per Second
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most-Significant Bit
OCD	On-Chip Debugger
POR	Power On Reset
PPOR	precision power on reset
PSRR	Power Supply Rejection Ratio
PWRSYS	Power System
PSoC®	Programmable System-on-Chip
SLIMO	Slow Internal Main Oscillator
SRAM	Static Random Access Memory
SNR	Signal to Noise Ratio
QFN	Quad Flat No-lead
SCL	Serial I2C Clock
SDA	Serial I2C Data
SDATA	Serial ISSP Data
SPI	Serial Peripheral Interface
SS	Slave Select
SSOP	Shrink Small Outline Package
TC	Test Controller
USB	Universal Serial Bus
USB D+	USB Data+
USB D–	USB Data–
WLCSP	Wafer Level Chip Scale Package
XTAL	Crystal

5. Wake-up from Sleep with Hardware I2C Address match on Pins P1[0], P1[1]

■ **Problem Definition**

I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL, to wake-up from sleep using I2C hardware address match event.

■ **Parameters Affected**

$t_{HD;DAT}$ increased to 20 ns from 0 ns

■ **Trigger Condition(S)**

This is an issue only when all these three conditions are met:

1) P1.0 and P1.1 are used as I2C pins,

2) Wakeup from sleep with hardware address match feature is enabled, and

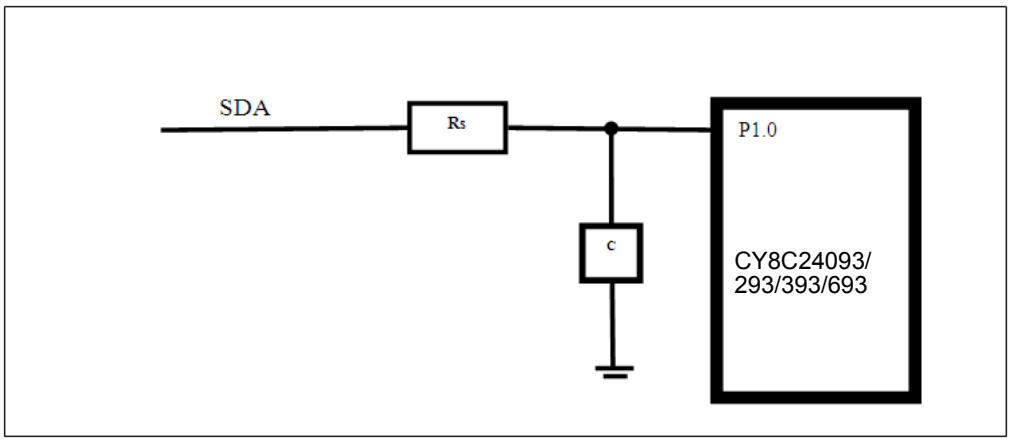
3) I2C master does not provide 20 ns hold time on SDA with respect to falling edge of SCL.

■ **Scope of Impact**

These trigger conditions cause the device to never wake-up from sleep based on I2C address match event

■ **Workaround**

For a design that meets all of the trigger conditions, the following suggested circuit has to be implemented as a work-around. The R and C values proposed are 100 ohm and 200 pF respectively.



■ **Fix Status**

Will not be fixed

■ **Changes**

None

6. I2C Port Pin Pull-up Supply Voltage

■ **Problem Definition**

Pull-up resistor on I2C interface cannot be connected to a supply voltage that is greater than 0.7 V of CY8C24093/293/393/693 V_{DD}.

■ **Parameters Affected**

None.

■ **Trigger Condition(S)**

This problem occurs only when the I2C master is powered at a higher voltage than CY8C24093/293/393/693.

■ **Scope of Impact**

This trigger condition will corrupt the I2C communication between the I2C host and the CY8C24093/293/393/693 controller.

■ **Workaround**

I2C master cannot be powered at a supply voltage that is greater than 0.7 V compared to CY8C24093/293/393/693 supply voltage.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

7. Port1 Pin Voltage

■ **Problem Definition**

Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C24093/293/393/693 V_{DD}.

■ **Parameters Affected**

None.

■ **Trigger Condition(S)**

This problem occurs only when port1 pins are at voltage 0.7 V higher than V_{DD} of CY8C24093/293/393/693.

■ **Scope of Impact**

This trigger condition will not allow CY8C24093/293/393/693 to drive the output signal on port1 pins, input path is unaffected by this condition.

■ **Workaround**

Port1 should not be connected to a higher voltage than V_{DD} of CY8C24093/293/393/693.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

2. I²C Errors

■ **Problem Definition**

The I²C block exhibits occasional data and bus corruption errors when the I²C master initiates transactions while the device is transitioning in to or out of sleep mode.

■ **Parameters Affected**

Affects reliability of I²C communication to device, and between I²C master and third party I²C slaves.

■ **Trigger Condition(S)**

Triggered by transitions into and out of the device's sleep mode.

■ **Scope of Impact**

Data errors result in incorrect data reported to the I²C master, or incorrect data received from the master by the device. Bus corruption errors can corrupt data in transactions between the I²C master and third party I²C slaves.

■ **Workaround**

Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the I²C block from the bus prior to going to sleep modes. I²C transactions during sleep are supported by a protocol in which the master wakes the device prior to the I²C transaction.

■ **Fix Status**

To be fixed in future silicon.

■ **Changes**

None

3. DoubleTimer0 ISR

■ **Problem Definition**

When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■ **Scope of Impact**

The ISR may be executed twice.

■ **Workaround**

In the ISR, firmware should clear the one-shot bit with a statement such as "`and reg[B0h], FDh`"

■ **Fix Status**

Will not be fixed

■ **Changes**

None

4. Missed GPIO Interrupt

■ **Problem Definition**

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■ **Scope of Impact**

The GPIO interrupt service routine will not be run.

■ **Workaround**

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

5. Missed Interrupt During Transition to Sleep

■ **Problem Definition**

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode just prior to an interrupt.

■ **Scope of Impact**

The relevant interrupt service routine will not be run.

■ **Workaround**

None.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

Document History Page

Document Title: CY8C24X93, PSoC® Programmable System-on-Chip Document Number: 001-86894				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3947416	AMKA	04/02/2013	New data sheet.
*A	3971208	AMKA	04/30/2013	Changed status from Preliminary to Final. Updated Features. Updated PSoC® Functional Overview (Updated Analog system (Updated IDAC), updated Additional System Resources). Updated Ordering Information (Updated part numbers).
*B	4009884	AMKA	05/24/2013	Updated Logic Block Diagram. Updated Getting Started (Updated Silicon Errata). Updated Development Tool Selection (Updated Evaluation Tools (Removed CY3210-PSoCEval1)). Updated Reference Documents. Added Appendix A: Silicon Errata for the CY8C24093/293/393/693 Family. Added Appendix B: Silicon Errata for the PSoC® CY8C24193/493 Families.
*C	5262060	ASRI	05/06/2016	Updated hyperlinks across the document. Added More Information. Updated Packaging Information: spec 001-09116 – Changed revision from *H to *J. spec 001-13191 – Changed revision from *G to *H. Updated to new template. Completing Sunset Review.