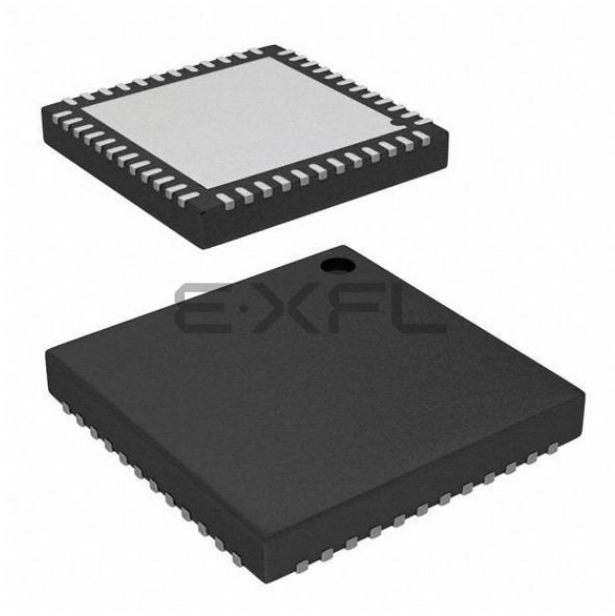

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24493-24ltxi

Pinouts

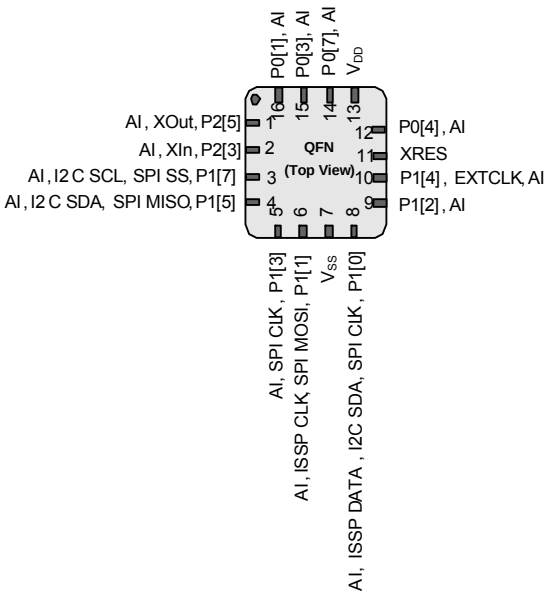
16-pin QFN (13 GPIOs) [2]

Table 2. Pin Definitions – CY8C24093 [3]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I^2C SCL, SPI SS
4	IOHR	I	P1[5]	I^2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK[4], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	IOHR	I	P1[0]	ISSP DATA[4], I^2C SDA, SPI CLK[5]
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	IOH	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	
16	IOH	I	P0[1]	

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 2. CY8C24093 Device



Notes
2. No center pad.
3. 13 GPIOs.
4. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I^2C bus. Use alternate pins if you encounter issues.
5. Alternate SPI clock.

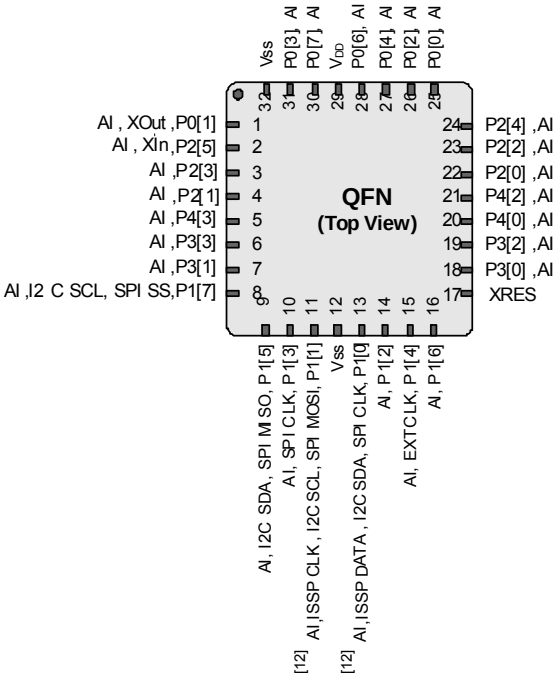
32-pin QFN (28 GPIOs) [10]

Table 4. Pin Definitions – CY8C24293 [11]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[1]	
2	I/O	I	P2[5]	Crystal output (XOut)
3	I/O	I	P2[3]	Crystal input (XIn)
4	I/O	I	P2[1]	
5	I/O	I	P4[3]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK [12], I^2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection
13	IOHR	I	P1[0]	ISSP DATA[12], I^2C SDA, SPI CLK[13]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P4[0]	
21	I/O	I	P4[2]	
22	I/O	I	P2[0]	
23	I/O	I	P2[2]	
24	I/O	I	P2[4]	
25	IOH	I	P0[0]	
26	IOH	I	P0[2]	
27	IOH	I	P0[4]	
28	IOH	I	P0[6]	
29	Power		V_{DD}	
30	IOH	I	P0[7]	
31	IOH	I	P0[3]	
32	Power		V_{SS}	Ground connection
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 4. CY8C24293 Device



Notes

10. 28 GPIOs.
11. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
12. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
13. Alternate SPI clock.

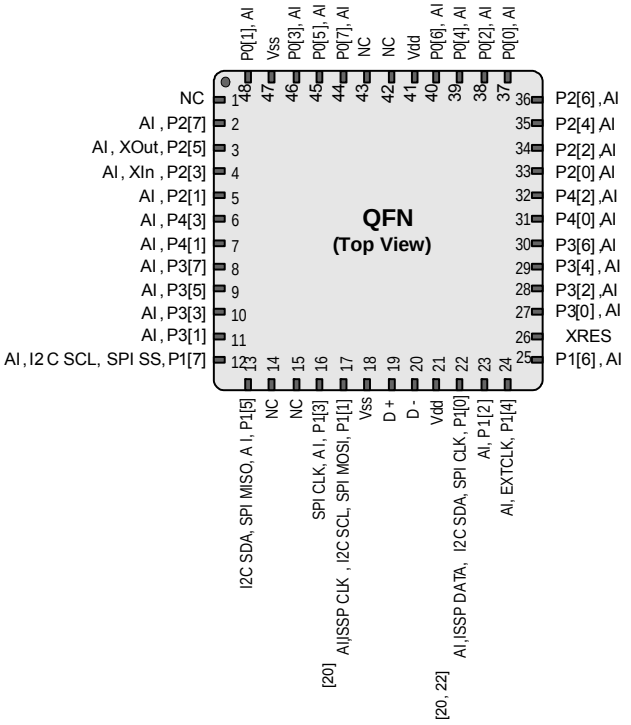
48-pin QFN (36 GPIOs (With USB)) [19]

Table 6. Pin Definitions – CY8C24493 [20, 21]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[20], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[20], I^2C SDA, SPI CLK[22]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	
47	Power		V_{SS}	Ground connection
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 6. CY8C24493



Notes

19. 36 GPIOs.
20. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
21. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
22. Alternate SPI clock.

Table 13. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V_{IL}	Input low voltage	–	–	–	0.30 × V_{DD}	V
V_{IH}	Input high voltage	–	0.65 × V_{DD}	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Table 14. GPIO Current Sink and Source Specifications

Supply Voltage	Mode	Port 1 per I/O (max)	Port 2/3/4 per I/O (max)	Total Current Even Pins (max)	Total Current Odd Pins (max)	Units
1.71 – 2.4	Sink	5	5	20	30	mA
	Source	2	0.5	10[31]		mA
2.4 – 3.0	Sink	10	10	30	30	mA
	Source	2	0.2	10[31]		mA
3.0 – 5.0	Sink	25	25	60	60	mA
	Source	5	1	20[31]		mA

Note
31. Total current (odd + even ports)

DC POR and LVD Specifications (CY8C24193/493)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR0}	1.66 V selected in PSoC Designer	V_{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V_{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	
V_{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	
V_{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	
V_{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64[46]	2.71	2.78	
V_{LVD2}	2.92 V selected in PSoC Designer		2.85[47]	2.92	2.99	
V_{LVD3}	3.02 V selected in PSoC Designer		2.95[48]	3.02	3.09	
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V_{LVD6}	1.80 V selected in PSoC Designer		1.75[49]	1.80	1.84	
V_{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

DC Programming Specifications (CY8C24193/493)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 20. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations	–	1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify	–	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	V_{IH}	–	–	V
I_{ILP}	Input current when Applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33. For V_{DD} > 3V use V_{OH4} in Table 36 on page 33.	V_{OH}	–	V_{DD}	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Notes
32. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
33. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
34. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
35. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

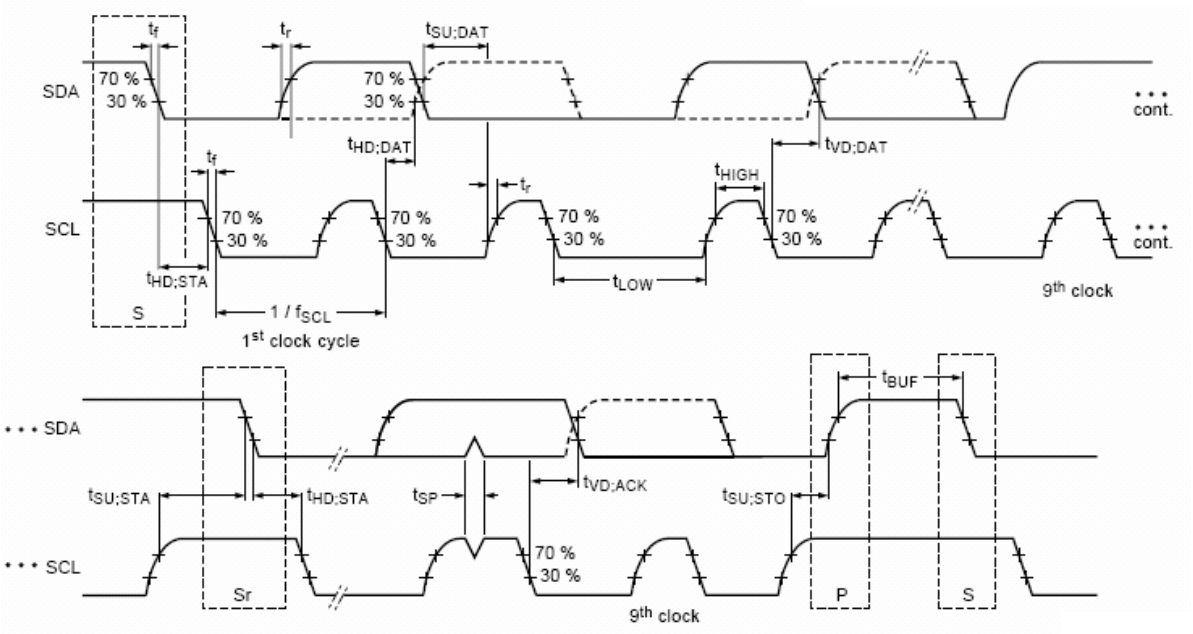
AC I²C Specifications (CY8C24193/493)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 30. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$[40]	Data hold time	20	3.45	20	0.90	µs
$t_{SU;DAT}$	Data setup time	250	–	100[53]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 11. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

40. To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. See the CY8C24x93 Silicon Errata document for more details.
41. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

DC Chip-Level Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 35. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}[43, 44, 45]	Supply voltage	No USB activity. Refer the table DC POR and LVD Specifications (CY8C24093/293/393/693) on page 37	1.71	–	5.50	V
V_{DDUSB}[43, 44, 45]	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
		USB activity, USB regulator bypassed	3.15	3.3	3.60	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. No I/O sourcing current	–	–	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. No I/O sourcing current	–	–	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. No I/O sourcing current	–	–	1.80	mA
I_{SB0}	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.05	µA
I_{SB1}	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C}	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	µA

Notes

43. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
44. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
    For the referenced registers, refer to the CY8C24x93 *Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1V/ms.
45. For USB mode, the V_{DD} supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application, V_{DD} should be 3.15 V–3.45 V.

Table 37. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.40	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	1.40	–		V
V_{H}	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT2.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
$V_{IHLVT2.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

Table 38. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V

Table 38. 1.71 V to 2.4 V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IL}	Input low voltage	–	–	–	0.30 × V_{DD}	V
V_{IH}	Input high voltage	–	0.65 × V_{DD}	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Table 39. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{USBI}	USB D+ pull-up resistance	With idle bus	900	–	1575	Ω
R_{USBA}	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	Ω
V_{OHUSB}	Static output high	–	2.8	–	3.6	V
V_{OLUSB}	Static output low	–	–	–	0.3	V
V_{DI}	Differential input sensitivity	–	0.2	–		V
V_{CM}	Differential input common mode range	–	0.8	–	2.5	V
V_{SE}	Single ended receiver threshold	–	0.8	–	2.0	V
C_{IN}	Transceiver capacitance	–	–	–	50	pF
I_{IO}	High Z state data line leakage	On D+ or D- line	–10	–	+10	µA
R_{PS2}	PS/2 pull-up resistance	–	3000	5000	7000	Ω
R_{EXT}	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 40. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus	–	–	–	800	Ω
R_{GND}	Resistance of initialization switch to V_{SS}	–	–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 41. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{DD}	0.0	–	1.8	V
I_{LPC}	LPC supply current	–	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	–	3	30	mV

DC POR and LVD Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 44. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR0}	1.66 V selected in PSoC Designer	V_{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V_{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	
V_{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	
V_{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	
V_{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64[46]	2.71	2.78	
V_{LVD2}	2.92 V selected in PSoC Designer		2.85[47]	2.92	2.99	
V_{LVD3}	3.02 V selected in PSoC Designer		2.95[48]	3.02	3.09	
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V_{LVD6}	1.80 V selected in PSoC Designer		1.75[49]	1.80	1.84	
V_{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

DC Programming Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 45. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations	–	1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify	–	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See the appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See the appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	V_{IH}	–	–	V
I_{ILP}	Input current when Applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify		–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33. For V_{DD} > 3 V use V_{OH4} in Table 34 on page 31.	V_{OH}	–	V_{DD}	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Notes
46. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
47. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
48. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
49. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

AC Chip-Level Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 49. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F_{IMO12}	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F_{IMO6}	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency	–	0.75	–	25.20	MHz
F_{32K1}	ILO frequency	–	15	32	50	kHz
F_{32K_U}	ILO untrimmed frequency	–	13	32	82	kHz
DC_{IMO}	Duty cycle of IMO	–	40	50	60	%
DC_{ILO}	ILO duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	V_{DD} slew rate during power-up	–	–	250	V/ms
t_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t_{XRST2}	External reset pulse width after power-up[50]	Applies after part has booted	10	–	–	µs
t_{OS}	Startup time of ECO	–	–	1	–	s
t_{JIT_IMO}[51]	N=32	6 MHz IMO cycle-to-cycle jitter (RMS)	–	0.7	6.7	ns
		6 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	4.3	29.3	ns
		6 MHz IMO period jitter (RMS)	–	0.7	3.3	ns
		12 MHz IMO cycle-to-cycle jitter (RMS)	–	0.5	5.2	ns
		12 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	2.3	5.6	ns
		12 MHz IMO period jitter (RMS)	–	0.4	2.6	ns
		24 MHz IMO cycle-to-cycle jitter (RMS)	–	1.0	8.7	ns
		24 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	1.4	6.0	ns
		24 MHz IMO period jitter (RMS)	–	0.6	4.0	ns

Notes

50. The minimum required XRES pulse length is longer when programming the device (see Table 55 on page 42).
51. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products for more information.

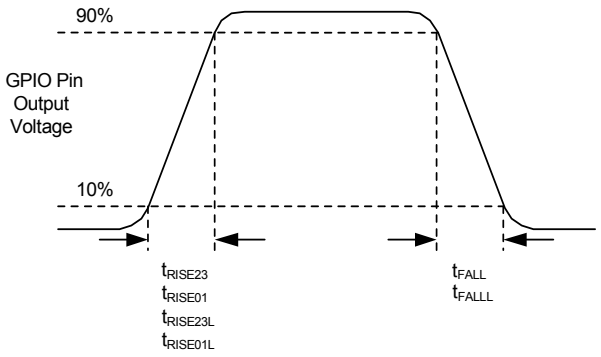
AC GPIO Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 50. AC GPIO Specifications

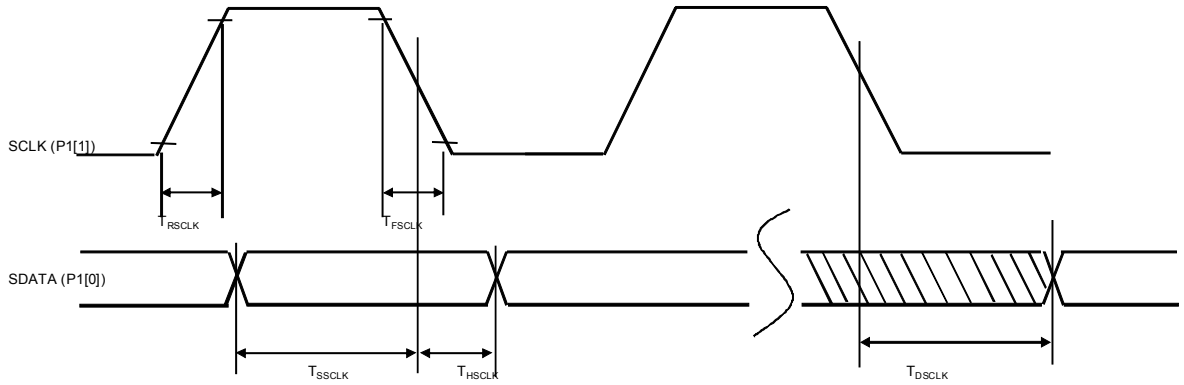
Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GPIO}	GPIO operating frequency	Normal strong mode Port 0, 1	0 0	– –	6 MHz for 1.71 V <V_{DD} < 2.40 V 12 MHz for 2.40 V < V_{DD}< 5.50 V	MHz MHz
t_{RISE23}	Rise time, strong mode, Cload = 50 pF Port 2 or 3 or 4 pins	V_{DD} = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
$t_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, Port 2 or 3 or 4 pins	V_{DD} = 1.71 to 3.0 V, 10% to 90%	15	–	80	ns
t_{RISE01}	Rise time, strong mode, Cload = 50 pF Ports 0 or 1	V_{DD} = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
$t_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	V_{DD} = 1.71 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
t_{FALL}	Fall time, strong mode, Cload = 50 pF all ports	V_{DD} = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
t_{FALLL}	Fall time, strong mode low supply, Cload = 50 pF, all ports	V_{DD} = 1.71 to 3.0 V, 10% to 90%	10	–	70	ns

Figure 17. GPIO Timing Diagram



AC Programming Specifications (CY8C24093/293/393/693)

Figure 18. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 55. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
t_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	–	40	–	–	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
t_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
t_{WRITE}	Flash block write time	–	–	–	25	ms
t_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \le V_{DD} \le 3.0$	–	–	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	µs
t_{XRES}	XRES pulse length	–	300	–	–	µs
$t_{VDDWAIT}$	V_{DD} stable to wait-and-poll hold off	–	0.1	–	1	ms
$t_{VDDXRES}$	V_{DD} stable to XRES assertion delay	–	14.27	–	–	ms
t_{POLL}	SDATA high pulse time	–	0.01	–	200	ms
t_{ACQ}	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
$t_{XRESINI}$	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	µs

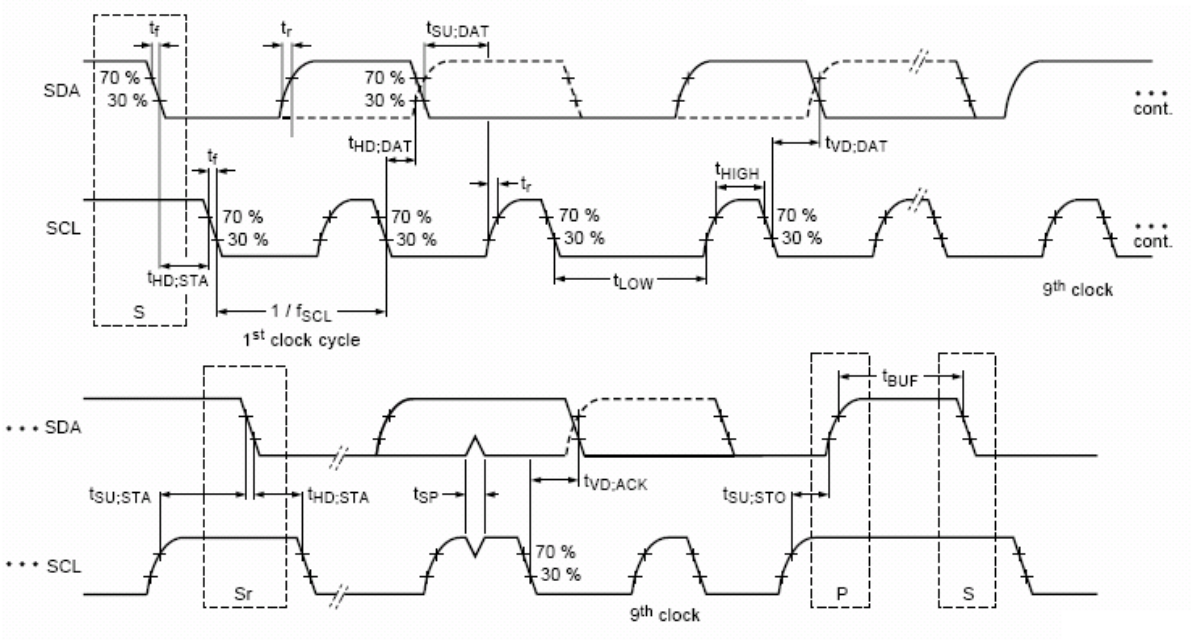
AC I²C Specifications (CY8C24093/293/393/693)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 56. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.90	µs
$t_{SU;DAT}$	Data setup time	250	–	100[53]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 19. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

53. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Table 58. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	42	–	–	ns
t_{HIGH}	SCLK high time	–	42	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 22. SPI Slave Mode 0 and 2

SPI Slave, modes 0 and 2

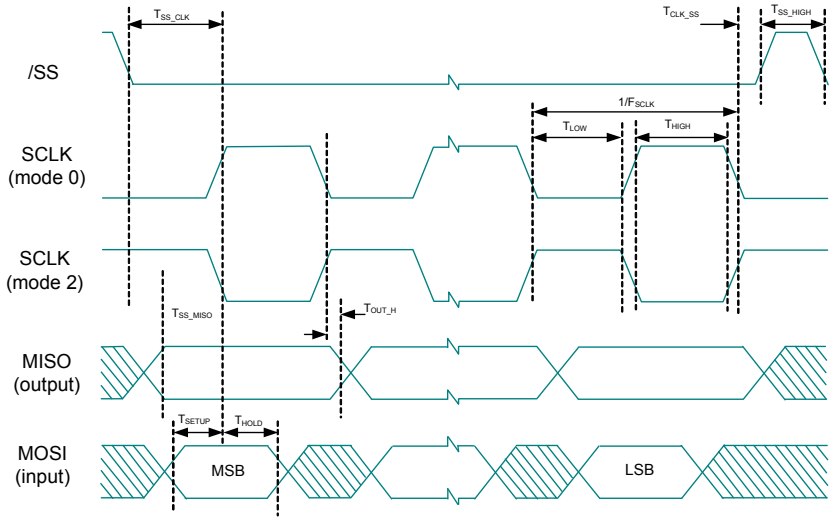
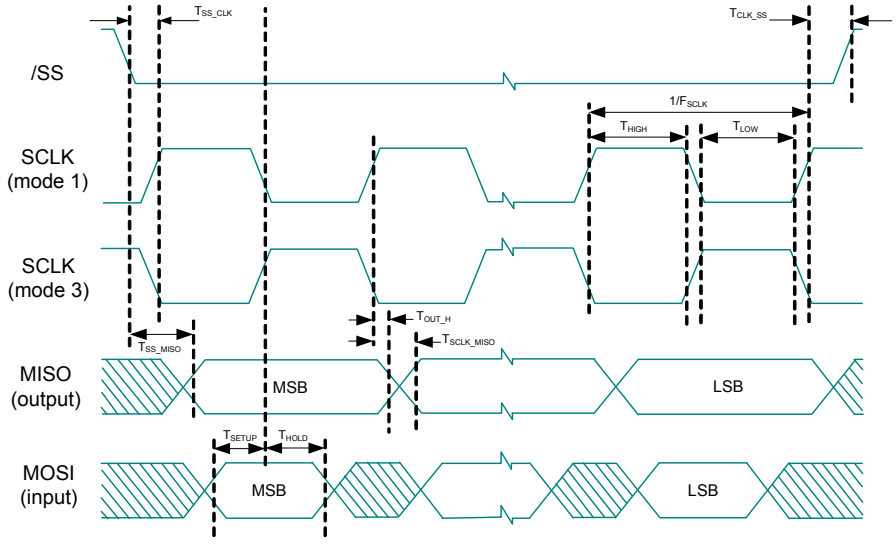


Figure 23. SPI Slave Mode 1 and 3

SPI Slave, modes 1 and 3



Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at http://www.cypress.com.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29X66A Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466A-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store. For more information on PSoC 1 kits, visit the link http://www.cypress.com/?rID=63754

Device Programmers

All device programmers are purchased from the Cypress Online Store.

2. Missed GPIO Interrupt

■ **Problem Definition**

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■ **Scope of Impact**

The GPIO interrupt service routine will not be run.

■ **Workaround**

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

3. Missed Interrupt During Transition to Sleep

■ **Problem Definition**

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode just prior to an interrupt.

■ **Scope of Impact**

The relevant interrupt service routine will not be run.

■ **Workaround**

None.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

Appendix B: Silicon Errata for the PSoC® CY8C24193/493 Families

This section describes the errata for the PSoC® CY8C24193/493 families. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

CY8C24193/493 Qualification Status

Product Status: Production released.

CY8C24193/493 Errata Summary

The following Errata items apply to the CY8C24193/493 datasheet 001-86894.

1. Wakeup from sleep may intermittently fail

■ **Problem Definition**

When the device is put to sleep in Standby or I2C_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received.

■ **Parameters Affected**

None

■ **Trigger Condition(S)**

By default, when the device is in the Standby or I2C_USB sleep modes, the bandgap circuit is powered-up approximately every 8 ms to facilitate detection of POR or LVD events. This interval can be lengthened or the periodic power-up disabled to reduce sleep current by setting the ALT_BUZZ bits in the SLP_CFG2 register or the Disable Buzz bit in the OSC_CR0 register respectively. If the bandgap circuit refresh interval is set longer than the default 8 ms, the device may fail to wakeup from sleep and enter a locked up state that can only be recovered by Watchdog Reset, XRES, or POR.

■ **Scope of Impact**

The trigger conditions outlined above may cause the device to never wakeup.

■ **Workaround**

Prior to entering Standby or I2C_USB sleep modes, do not lengthen or disable the bandgap refresh interval by manipulating the ALT_BUZZ bits in the SLP_CFG2 register or the Disable Buzz bit in the OSC_CR0 register respectively.

■ **Fix Status**

This issue will not be corrected in the next silicon revision.

2. I²C Errors

■ **Problem Definition**

The I²C block exhibits occasional data and bus corruption errors when the I²C master initiates transactions while the device is transitioning in to or out of sleep mode.

■ **Parameters Affected**

Affects reliability of I²C communication to device, and between I²C master and third party I²C slaves.

■ **Trigger Condition(S)**

Triggered by transitions into and out of the device's sleep mode.

■ **Scope of Impact**

Data errors result in incorrect data reported to the I²C master, or incorrect data received from the master by the device. Bus corruption errors can corrupt data in transactions between the I²C master and third party I²C slaves.

■ **Workaround**

Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the I²C block from the bus prior to going to sleep modes. I²C transactions during sleep are supported by a protocol in which the master wakes the device prior to the I²C transaction.

■ **Fix Status**

To be fixed in future silicon.

■ **Changes**

None

3. DoubleTimer0 ISR

■ **Problem Definition**

When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■ **Scope of Impact**

The ISR may be executed twice.

■ **Workaround**

In the ISR, firmware should clear the one-shot bit with a statement such as "`and reg[B0h], FDh`"

■ **Fix Status**

Will not be fixed

■ **Changes**

None

6. Wakeup from sleep with analog interrupt

■ **Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

■ **Scope of Impact**

Device unexpectedly wakes up from sleep

■ **Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wakeup.

■ **Fix Status**

Will not be fixed

■ **Changes**

None