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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l100rbt6atr

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L100x6/8/B-A ultra-low-power ARM® Cortex®-M3 based microcontrollers product line.

The ultra-low-power STM32L100x6/8/B-A microcontroller family includes devices in 2 different package types: 48 or 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L100x6/8/B-A microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, Wired and wireless sensors, Video intercom
- Utility metering

This STM32L100x6/8/B-A datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The document "Getting started with STM32L1xxxx hardware development" AN3216 gives a hardware implementation overview.

Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the ARM website.

Figure 1 shows the general block diagram of the device family.

Caution: This datasheet does not apply to:

– STM32L100x6/8/B

covered by a separate datasheet.

2 Description

The ultra-low-power STM32L100x6/8/B-A devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 128 Kbytes and RAM up to 16 Kbytes) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

All the devices offer a 12-bit ADC, 2 DACs and 2 ultra-low-power comparators, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L100x6/8/B-A devices contain standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs and a USB.

They also include a real-time clock with sub-second counting and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with contrast independent of the supply voltage.

The ultra-low-power STM32L100x6/8/B-A devices operate from a 1.8 to 3.6 V power supply. They are available in the -40 to +85 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From a proprietary 8-bit core up to the Cortex-M3, including the Cortex-M0+, the STM8Lx and STM32Lx series offer the best range of choices to meet your requirements in terms of ultra-low-power features. The STM32 Ultra-low-power series is an ideal fit for applications like gas/water meters, keyboard/mouse, or wearable devices for fitness and healthcare. Numerous built-in features like LCD drivers, dual-bank memory, low-power Run mode, op-amp, AES-128bit, DAC, crystal-less USB and many others, allow to build highly cost-optimized applications by reducing the BOM.

Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lx and STM32Lx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, your existing applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-Low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx and STM32L1xxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy

To offer flexibility and optimize performance, the STM8L15xxx and STM32L1xxxx families use a common architecture:

- Common power supply range from 1.8 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultra-safe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector.

2.2.4 Features

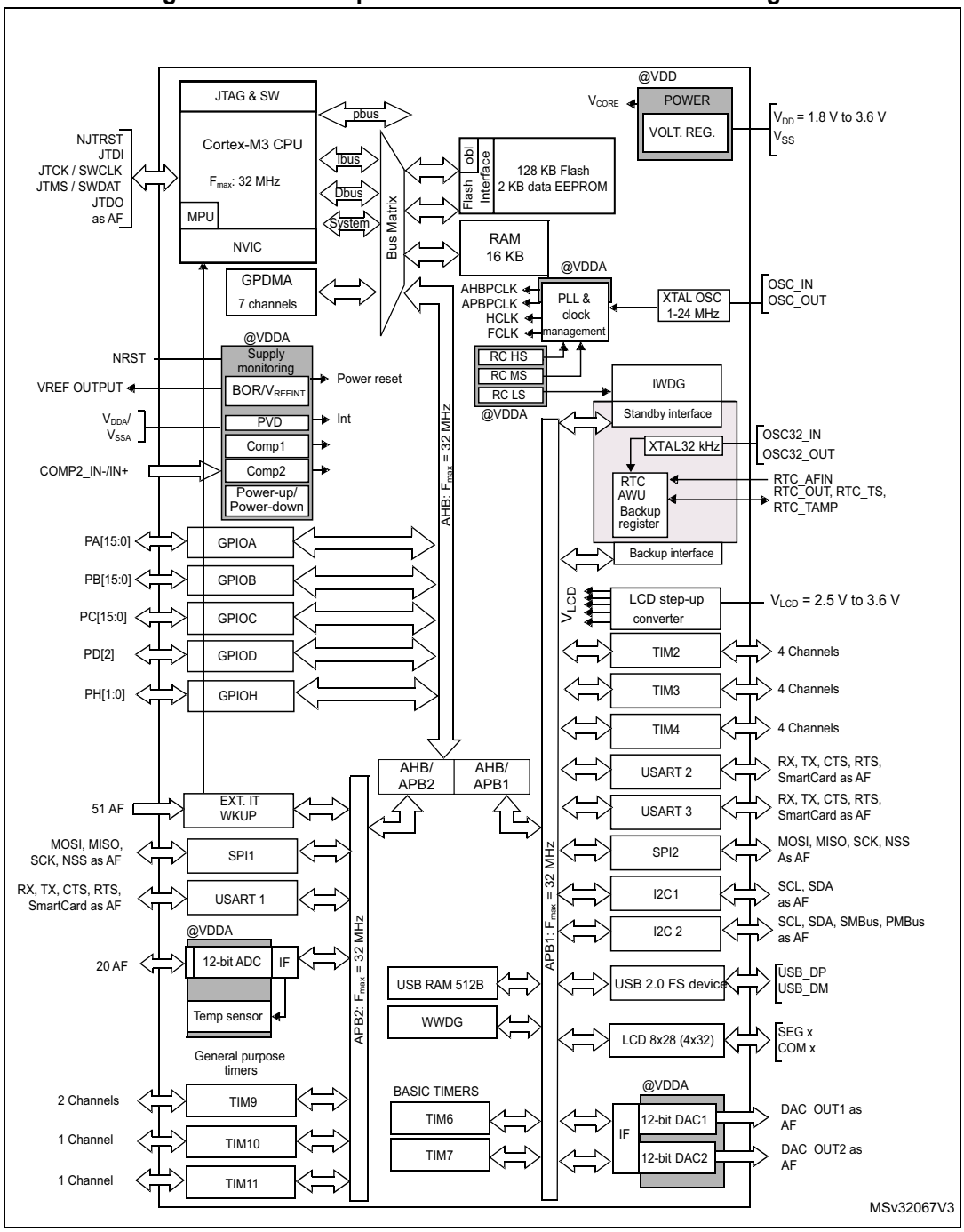
ST ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 512 Kbytes

3 Functional overview

Figure 1 shows the block diagram.

Figure 1. Ultra-low-power STM32L100x6/8/B-A block diagram



1. AF = alternate function on I/O port pin.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1 MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.3.3 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32K osc, RCC_CSR).

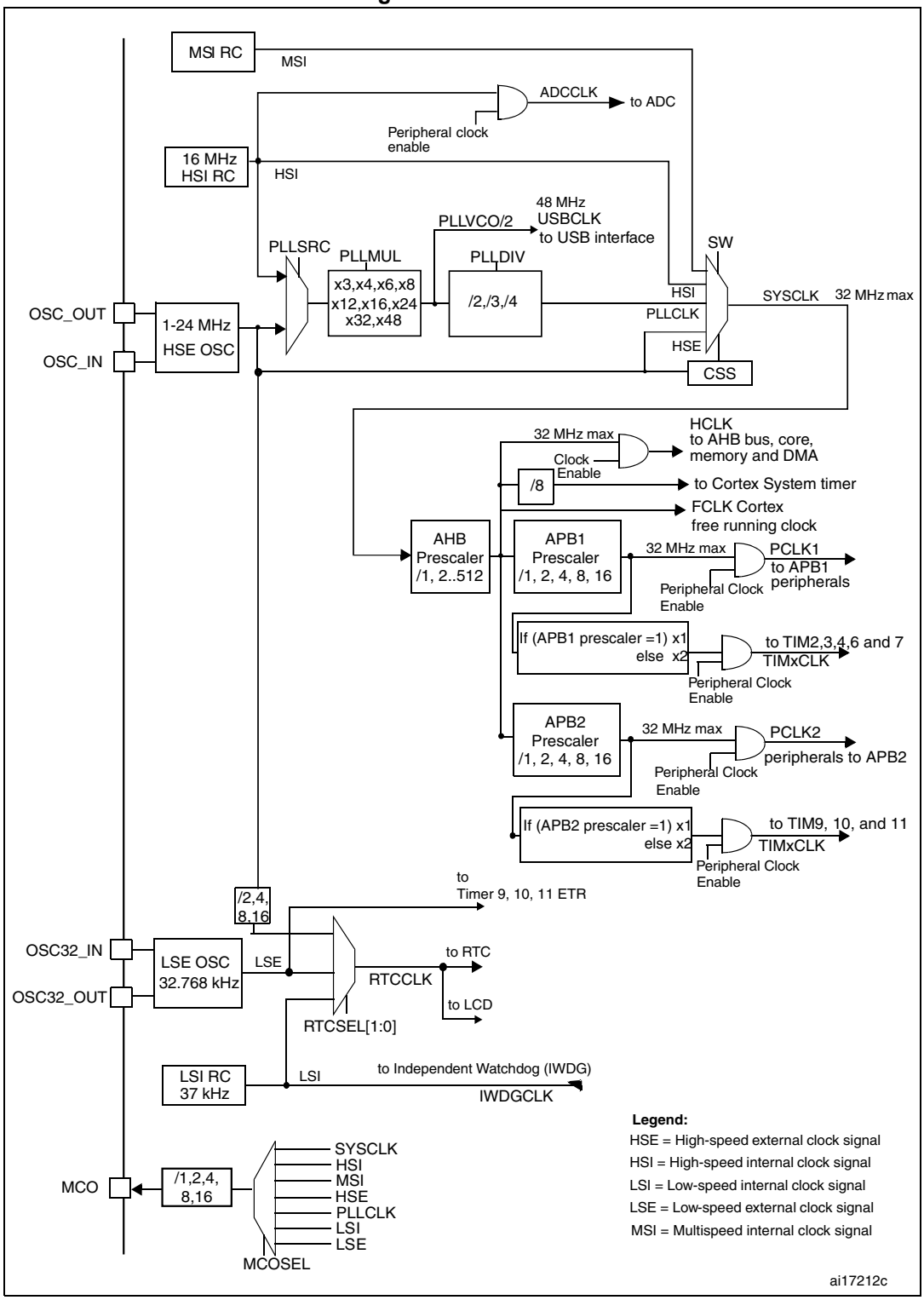
3.3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from Flash memory
- Boot from System Memory
- Boot from embedded RAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1 or USART2. See the application note “STM32 microcontroller system memory boot mode” (AN2606) for details.

Figure 2. Clock tree



3.7 Memories

The STM32L100x6/8/B-A devices have the following features:

- Up to 16 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32, 64 or 128 Kbyte of embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - Options bytes

  The options bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose timers and ADC.

Table 9. STM32L100x6/8/B-A pin definitions

Pins		Pin name	Pin type(1)	I/O structure	Main function(2) (after reset)	Pin functions	
LQFP64	UFQFPN48					Alternate functions	Additional functions
1	1	V_{LCD}	S	-	V_{LCD}	-	-
2	2	PC13-WKUP2	I/O	FT	PC13	-	RTC_TAMP1/ RTC_TS/ RTC_OUT/WKUP2
3	3	PC14-OSC32_IN(3)	I/O	TC	PC14	-	OSC32_IN
4	4	PC15-OSC32_OUT(4)	I/O	TC	PC15	-	OSC32_OUT
5	5	PH0-OSC_IN(4)	I/O	TC	PH0	-	OSC_IN
6	6	PH1-OSC_OUT	I/O	TC	PH1	-	OSC_OUT
7	7	NRST	I/O	RST	NRST	-	-
8	-	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP
9	-	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP
10	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
11	-	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP
12	8	V_{SSA}	S	-	V_{SSA}	-	-
13	9	V_{DDA}	S	-	V_{DDA}	-	-
14	10	PA0-WKUP1	I/O	FT	PA0	USART2_CTS/ TIM2_CH1_ETR	WKUP1/ADC_IN0/ COMP1_INP
15	11	PA1	I/O	FT	PA1	USART2_RTS/TIM2_CH2/ LCD_SEG0	ADC_IN1/ COMP1_INP
16	12	PA2	I/O	FT	PA2	USART2_TX/TIM2_CH3/ TIM9_CH1/LCD_SEG1	ADC_IN2/ COMP1_INP
17	13	PA3	I/O	TC	PA3	USART2_RX/TIM2_CH4/ TIM9_CH2/LCD_SEG2	ADC_IN3/ COMP1_INP
18	-	V_{SS_4}	S	-	V_{SS_4}	-	-
19	-	V_{DD_4}	S	-	V_{DD_4}	-	-

Table 10. Alternate function input/output

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFOI6	AFIO7	AFIO8	AFIO9	AFIO11	AFIO12	AFIO13	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4	TIM9/10/11	I2C1/2	SPI1/2	N/A	USART 1/2/3	N/A	N/A	LCD	N/A	N/A	RI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
NRST	NRST	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PA0-WKUP1	-	TIM2_CH1_ETR	-	-	-	-	-	USART2_CTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA1	-	TIM2_CH2	-	-	-	-	-	USART2_RTS	-	-	[SEG0]	-	-	TIMx_IC2	EVENTOUT
PA2	-	TIM2_CH3	-	TIM9_CH1	-	-	-	USART2_TX	-	-	[SEG1]	-	-	TIMx_IC3	EVENTOUT
PA3	-	TIM2_CH4	-	TIM9_CH2	-	-	-	USART2_RX	-	-	[SEG2]	-	-	TIMx_IC4	EVENTOUT
PA4	-	-	-	-	-	SPI1_NSS	-	USART2_CK	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA6	-	-	TIM3_CH1	TIM10_CH1	-	SPI1_MISO	-	-	-	-	[SEG3]	-	-	TIMx_IC3	EVENTOUT
PA7	-	-	TIM3_CH2	TIM11_CH1	-	SPI1_MOSI	-	-	-	-	[SEG4]	-	-	TIMx_IC4	EVENTOUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-	-	[COM0]	-	-	TIMx_IC1	EVENTOUT
PA9	-	-	-	-	-	-	-	USART1_TX	-	-	[COM1]	-	-	TIMx_IC2	EVENTOUT
PA10	-	-	-	-	-	-	-	USART1_RX	-	-	[COM2]	-	-	TIMx_IC3	EVENTOUT
PA11	-	-	-	-	-	SPI1_MISO	-	USART1_CTS	-	-	-	-	-	TIMx_IC4	EVENTOUT
PA12	-	-	-	-	-	SPI1_MOSI	-	USART1_RTS	-	-	-	-	-	TIMx_IC1	EVENTOUT
PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENTOUT
PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENTOUT
PA15	JTDI	TIM2_CH1_ETR	-	-	-	SPI1_NSS	-	-	-	-	SEG17	-	-	TIMx_IC4	EVENTOUT
PB0	-	-	TIM3_CH3	-	-	-	-	-	-	-	[SEG5]	-	-	-	EVENTOUT
PB1	-	-	TIM3_CH4	-	-	-	-	-	-	-	[SEG6]	-	-	-	EVENTOUT
PB2	BOOT1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO	TIM2_CH2	-	-	-	SPI1_SCK	-	-	-	-	[SEG7]	-	-	-	EVENTOUT

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all different ground pins(3)	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 12* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	100	mA
ΣI_{VSS}(2)	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD_x} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS_x} ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4) RST and B pins	-5/+0	
	Injected current on any other pin(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.17*.

4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 64: Thermal characteristics on page 98*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in the following table.

Table 15. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	V
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.60	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	

6.3.3 Embedded internal reference voltage

The parameters given in the following table are based on characterization results, unless otherwise specified.

Table 16. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C, V_{DDA}= 3 V ±10 mV	0x1FF8 0078-0x1FF8 0079

Table 17. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(1)	Internal reference voltage	– 40 °C < T_J < +85 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value (2)	Including uncertainties due to ADC and V_{DDA} values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +85 °C	-	25	100	ppm/°C
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(3)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
T_{ADC_BUF}(3)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current(5)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple interactions.
5. To guarantee less than 1% VREF_OUT deviation.

Table 21. Current consumption in Low power run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$I_{DD\ (LP\ Run)}$	Supply current in Low power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.8 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	10.9	12	µA
				T_A = 85 °C	16.5	23	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	15	16	
				T_A = 85 °C	22	29	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	29	37	
				T_A = 55 °C	32.5	40	
				T_A = 85 °C	35.5	54	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.8 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	23	24	
				T_A = 85 °C	31	34	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	29	31	
				T_A = 85 °C	38	41	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	46	55	
				T_A = 55 °C	48	59	
				T_A = 85 °C	53.5	72	
I_{DD} Max (LP Run)(2)	Max allowed current in Low power run mode	V_{DD} from 1.8 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.
2. This limitation is related to the consumption of the CPU core and the peripherals that are powered by the regulator. Consumption of the I/Os is not included in this limitation.

Table 29. HSE oscillator characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$ (4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 13*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Table 55. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN}	Signal source impedance(2)	-	-	-	50	κΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

1. V_{SSA} must be tied to ground.
2. See *Table 57: Maximum source impedance RAIN max* for R_{AIN} limitations

Table 56. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions	Min(3)	Typ	Max(3)	Unit
ET	Total unadjusted error	2.4 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 8 MHz, R_{AIN} = 50 Ω T_A = -40 to 85 °C	-	2.5	4	LSB
EO	Offset error		-	1	2	
EG	Gain error		-	1.5	3.5	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	2	3	
ENOB	Effective number of bits	2.4 V ≤ V_{DDA} ≤ 3.6 V f_{ADC} = 16 MHz, R_{AIN} = 50 Ω T_A = -40 to 85 °C F_{input} =10 kHz	9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio		59	62	-	dB
SNR	Signal-to-noise ratio		60	62	-	
THD	Total harmonic distortion		-	-72	-69	
ENOB	Effective number of bits	1.8 V ≤ V_{DDA} ≤ 2.4 V f_{ADC} = 8 MHz or 4 MHz, R_{AIN} = 50 Ω T_A = -40 to 85 °C F_{input} =10 kHz	9.5	10	-	bits
SINAD	Signal-to-noise and distortion ratio		59	62	-	dB
SNR	Signal-to-noise ratio		60	62	-	
THD	Total harmonic distortion		-	-72	-69	
ET	Total unadjusted error	1.8 V ≤ V_{DDA} ≤ 2.4 V f_{ADC} = 4 MHz, R_{AIN} = 50 Ω T_A = -40 to 85 °C	-	2	3	LSB
EO	Offset error		-	1	1.5	
EG	Gain error		-	1.5	2.5	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-		3	

1. ADC DC accuracy values are measured after internal calibration.

Figure 24. Maximum dynamic current consumption on V_{DDA} supply pin during ADC conversion

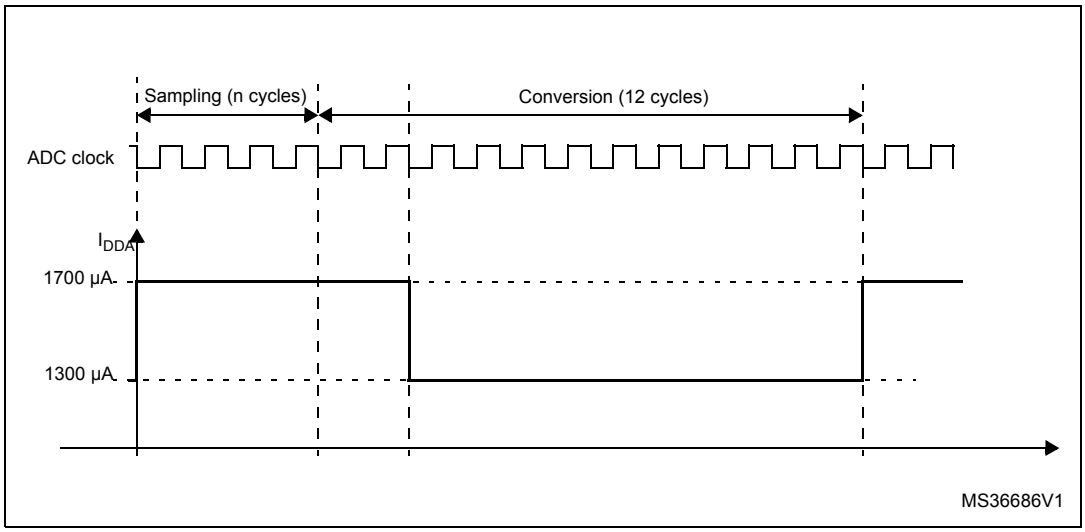


Table 57. Maximum source impedance R_{AIN} max(1)

Ts (µs)	R_{AIN} max (kOhm)				Ts (cycles) f_{ADC}= 16 MHz(2)
	Multiplexed channels		Direct channels		
	2.4 V < V_{DDA}< 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA}< 3.3 V	1.8 V < V_{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.
2. Number of samples calculated for **f_{ADC} = 16 MHz. F**or **f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (us).**

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 8*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Table 58. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dGain/dT(1)	Gain error temperature coefficient	V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V, T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE(1)	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	12	30	LSB
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(7)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Difference between two consecutive codes - 1 LSB.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x800) and the ideal value = $V_{DDA}/2$.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
7. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

9 Revision history

Table 66. Document revision history

Date	Revision	Changes
25-Mar-2014	1	Initial release.
27-Oct-2014	2	Updated DMIPS features in cover page and *Section 2: Description* Updated current consumption in *Table 20: Current consumption in Sleep mode*. Updated *Table 25: Peripheral current consumption* with new measured values. Updated *Table 57: Maximum source impedance RAIN max* adding note 2.
03-Feb-2015	3	Updated *Section 7: Package information* with new package device markings. Updated *Figure 5: Memory map*.
30-Apr-2015	4	Updated *Section 7: Package information* structure: Paragraph titles and paragraph heading level. Updated *Table 62: LQFP64 10 x 10 mm, 64-pin low-profile quad flat package mechanical data*. Updated *Section 7: Package information* for LQFP64 and UFQFPN48 package device markings, adding text for device orientation versus pin 1 identifier. Updated *Table 17: Embedded internal reference voltage* temperature coefficient at 100ppm/°C and table footnote 3: “guaranteed by design” changed by “guaranteed by characterization results”. Updated *Table 60: Comparator 2 characteristics* new maximum threshold voltage temperature coefficient at 100ppm/°C.
25-Apr-2016	5	Updated *Table 40: ESD absolute maximum ratings* CDM class. Updated all the notes, removing ‘not tested in production’. Updated *Table 11: Voltage characteristics* adding note about V_{REF-} pin. Updated *Table 3: Functionalities depending on the operating power supply range* LSI and LSE functionalities putting “Y” in Standby mode. Removed note 1 below *Figure 2: Clock tree*. Updated *Section 7: Package information* replacing “Marking of engineering samples” by “device marking”. Updated *Table 58: DAC characteristics* resistive load.