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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 27x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk22fn1m0avlk12r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	_	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	_	3	_	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

1.4 Voltage and current operating ratings

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Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	185	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
Ι _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V
V _{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V _{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
V _{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

- 1. output pins
 - have C_L=30pF loads,
 - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
 - are configured for high drive strength (PORTx_PCRn[DSE]=1)
- 2. input pins
 - have their passive filter disabled (PORTx_PCRn[PFE]=0)



5. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	_	300	μs	
	• VLLS0 → RUN	—	183	μs	
	• VLLS1 → RUN	—	183	μs	
	• VLLS2 \rightarrow RUN	_	105	μs	
	• VLLS3 → RUN	_	105	μs	
	• LLS → RUN	—	5.0	μs	
	• VLPS → RUN	—	4.4	μs	
	• STOP \rightarrow RUN	—	4.4	μs	

2.2.5 Power consumption operating behaviors

 Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
		—	33.57	36.2	mA	
		_	33.51	36.1	mA	

Table continues on the next page...



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	• @ 1.8V					
	• @ 3.0V					
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	46.36	50.1	mA	
	• @ 3.0V		46.01	40.0		
	• @ 25°C	_	40.31	49.9	mA mA	
	• @ 125°C	—	57.4		ma	
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	_	18.2	_	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	_	7.2	—	mA	5
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	_	1.21	-	mA	6
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	_	1.88		mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.80	_	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ -40 to 25°C	—	0.528	2.25	mA	
	• @ 70°C	_	1.6	8	mA	
	• @ 105°C	_	5.2	20	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ -40 to 25°C	—	78	700	μA	
	• @ 70°C	—	498	2400	μA	
	• @ 105°C	—	1300	3600	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V					
	● @ -40 to 25°C	_	5.1	15	μA	
	• @ 70°C	—	28	80	μA	
	• @ 105°C	—	124	300	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ -40 to 25°C	—	3.1	7.5	μA	
	• @ 70°C	—	14.5	45	μA	
	• @ 105°C	—	63.5	195	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ -40 to 25°C	—	2.0	5	μA	
		—	6.9	32	μA	

Table 6. Power consumption operating behaviors (continued)

Table continues on the next page ...



Symbol	Description	Min.	Max.	Unit	Notes
	• 1.71 ≤ V _{DD} ≤ 2.7V	_	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	

Table 10. General switching specifications

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater synchronous and asynchronous timing must be met.
- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 75 pF load
- 5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C

2.4.2 Thermal attributes

Board type	Symbol	Description	80 LQFP	Unit	Notes	
Single-layer (1s)	R _{0JA}	Thermal resistance, junction to ambient (natural convection)	50	59	°C/W	1
Four-layer (2s2p)	R _{0JA}	Thermal resistance, junction to ambient	35	41	°C/W	1

Table continues on the next page ...



Symbol	Description		Min.	Тур.	Max.	Unit	Notes
		$2197 \times f_{fll_ref}$					
		High range (DRS=11)	—	95.98	—	MHz	
		$2929 \times f_{fll_ref}$					
J _{cyc_fll}	FLL period jitter		_	180	_	ps	
	 f_{DCO} = 48 N f_{DCO} = 98 N 	1Hz 1Hz	_	150	_		
t _{fll_acquire}	FLL target freque	ncy acquisition time	—	—	1	ms	7
		P	ĹĹ				
f _{vco}	VCO operating fre	equency	48.0	_	120	MHz	
I _{pll}	PLL operating current • PLL @ 96 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 48)		_	1060	_	μA	8
I _{pll}	PLL operating cur PLL @ 48 N = 2 MHz, V	_	600	_	μΑ	8	
f _{pll_ref}	PLL reference fre	quency range	2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS)					9
	• f _{vco} = 48 MH	Hz	_	120	_	ps	
	• f _{vco} = 120 M	1Hz	_	75	_	ps	
J _{acc_pll}	PLL accumulated	jitter over 1µs (RMS)					9
	• f _{vco} = 48 MH	Hz	_	1350	_	ps	
	• f _{vco} = 120 N	1Hz	_	600	_	ps	
D _{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D _{unl}	Lock exit frequent	cy tolerance	± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector det	ection time	_	_	150 × 10 ⁻⁶ + 1075(1/ f _{pll_ref})	S	10

Table 15. MCG specifications (continued)

- 1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2. 2 V <= VDD <= 3.6 V.
- 3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
- The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
- 5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
- 6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- 8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
- This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
		—	0	—	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	_	0.6		V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

Table 16. Oscillator DC electrical specifications (continued)

- 1. V_{DD} =3.3 V, Temperature =25 °C, Internal capacitance = 20 pf
- 2. See crystal or resonator manufacturer's recommendation
- 3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
- 4. When low power mode is selected, R_F is integrated and must not be attached externally.
- 5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal or resonator frequency — low- frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f _{osc_hi_1}	Oscillator crystal or resonator frequency — high- frequency mode (low range) (MCG_C2[RANGE]=01)	3	_	8	MHz	
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	_	32	MHz	
f _{ec_extal}	Input clock frequency (external clock mode)	_	—	50	MHz	1, 2
t _{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t _{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	_	750	_	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	_	0.6	_	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	_	1	_	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.

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3.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFE to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

Writes_subsystem =
$$\frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write_efficiency} \times n_{\text{nvmcycee}}$$

where

- Writes_subsystem minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcvcee} EEPROM-backup cycling endurance





Figure 14. FlexBus write timing diagram

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog



Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
	ADC	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t _{ADACK} =
	asynchronous clock source	• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	1/f _{ADACK}
f _{ADACK}		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for	sample time	es			
TUE	Total	 12-bit modes 	—	±4	±6.8	LSB ⁴	5
	unadjusted error	 <12-bit modes 	_	±1.4	±2.1		
DNL	Differential non- linearity	12-bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
		 <12-bit modes 	—	±0.2	–0.3 to 0.5		
INL	Integral non-	12-bit modes	—	±1.0	-2.7 to +1 9	LSB ⁴	5
		• <12-bit modes	_	±0.5	-0.7 to +0.5		
E _{FS}	Full-scale error	12-bit modes	_	-4	-5.4	LSB ⁴	V _{ADIN} =
		 <12-bit modes 	_	-1.4	-1.8		V _{DDA} ⁵
EQ	Quantization	16-bit modes	—	-1 to 0	_	LSB ⁴	
	error	 ≤13-bit modes 	_	_	±0.5		
ENOB	Effective	16-bit differential mode				hits	6
	number of bits	• Avg = 32	12.8	14.5		bits	
		• Avg = 4	11.9	13.8	_	Dita	
		16 bit single anded made			_	bits	
		ro-bit single-ended mode				bits	
		• $Avg = 32$	12.2	13.9	—		
		• Avg = 4	11.4	13.1	—		
SINAD	Signal-to-noise plus distortion	See ENOB	6.02	× ENOB +	1.76	dB	
THD	Total harmonic	16-bit differential mode				dB	7
	distortion	• Avg = 32	_	-94	—	dB	
		16-bit single-ended mode		05			
		• Avg = 32	_	-85	_		
SFDR	Spurious free	16-bit differential mode		_		dB	7
	dynamic range	• Avg = 32	82	95			
					_	dB	
		16-bit single-ended mode	78	90			
		• Avg = 32					

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Table continues on the next page...



Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
EIL	Input leakage error			$I_{ln} \times R_{AS}$		mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V _{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

- 1. All accuracy numbers assume the ADC is calibrated with $V_{\text{REFH}} = V_{\text{DDA}}$
- Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- 8. ADC conversion clock < 3 MHz

Typical ADC 16-bit Differential ENOB vs ADC Clock



Figure 16. Typical ENOB vs. ADC_CLK for 16-bit differential mode





Figure 17. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DD}	Supply voltage	1.71	—	3.6	V
I _{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	_	_	200	μA
I _{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	_	20	μA
V _{AIN}	Analog input voltage	V _{SS} – 0.3	_	V _{DD}	V
V _{AIO}	Analog input offset voltage	_	_	20	mV
V _H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	_	5	—	mV
	 CR0[HYSTCTR] = 01 	_	10	_	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	_	30	_	mV
V _{CMPOh}	Output high	V _{DD} – 0.5		_	V
V _{CMPOI}	Output low	_	_	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)	—	7	_	μA
INL	6-bit DAC integral non-linearity	-0.5	_	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	_	0.3	LSB



Figure 19. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements Table 30. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
V _{DACR}	Reference voltage	1.13	3.6	V	1
CL	Output load capacitance	—	100	pF	2
١L	Output load current	_	1	mA	

1. The DAC reference can be selected to be V_{DDA} or $V_{\text{REFH}}.$

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.



USB electrical specifications 3.8.1

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The MCGFLLCLK does not meet the USB jitter specifications for certification.

3.8.2 USB DCD electrical specifications Table 36. USB0 DCD electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μA
I _{DM_SINK}	USB_DM sink current	50	100	150	μA
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

3.8.3 USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit
VREGIN	Input supply voltage	2.7	—	5.5	V
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	_	125	186	μA
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA
I _{DDoff}	Quiescent current — Shutdown mode				

Table 37 USB VREG electrical specifications

VREGIN	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	μA	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	_	1.1	10	μA	
I _{DDoff}	 Quiescent current — Shutdown mode VREGIN = 5.0 V and temperature=25 °C Across operating voltage and temperature 	_	650 —	 4	nA μA	
I _{LOADrun}	Maximum load current — Run mode	_	_	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	_	_	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V					
		3	3.3	3.6	V	

Table continues on the next page ...

Notes



Num	Description	Min.	Max.	Unit	Notes
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

Table 38. Master mode DSPI timing (limited voltage range) (continued)

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 22. DSPI classic SPI timing — master mode

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid		17.4	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven		16	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	16	ns

Table 39. Slave mode DSPI timing (limited voltage range)





Figure 27. I²S timing — master mode

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	80	_	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	4.5	—	ns
S14	I2S_FS input hold after I2S_BCLK	2	_	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	18	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	4.5	_	ns
S18	I2S_RXD hold after I2S_BCLK	2	_	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹		21	ns

Table 44. I²S slave mode timing

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





Figure 29. I2S/SAI timing — master modes

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	23.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	_	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	_	25	ns

Table 46. I2S/SAI slave mode timing

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





Figure 32. I2S/SAI timing — slave modes

3.8.10.3 Ordering parts

3.8.10.3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK22 and MK22

3.8.10.4 Part identification

3.8.10.4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.8.10.4.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

3.8.10.4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):



Pinout

80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
58	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK		
59	VSS	VSS	VSS								
60	VDD	VDD	VDD								
61	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
62	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT	FTM0_CH2	
63	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9	I2S0_MCLK		
64	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS	FB_AD8			
65	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7			
66	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_ BCLK	FB_AD6	FTM2_FLT0		
67	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5			
68	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b			
69	VSS	VSS	VSS								
70	VDD	VDD	VDD								
71	PTC16	DISABLED		PTC16		UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_ 16_BLS15_8_ b			
72	PTC17	DISABLED		PTC17		UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_ 24_BLS7_0_b			
73	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_ RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b			
74	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_ CTS_b	FTM3_CH1	FB_CS0_b			
75	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4		I2C0_SCL	
76	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3		I2C0_SDA	
77	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UARTO_ RTS_b	FTM0_CH4	FB_AD2	EWM_IN		
78	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_ CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b		
79	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
80	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		





Figure 33. K22 80 LQFP Pinout Diagram

6 Revision History

The following table provides a revision history for this document.