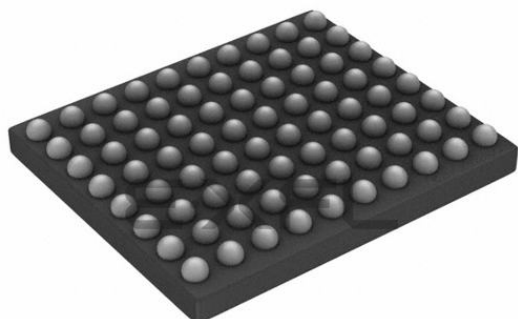




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 2x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-UFBGA, WLCSP
Supplier Device Package	80-WLCSP (4.13x3.56)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22fn512cap12r

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	−55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	1	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	−2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	−500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	−100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{OL}	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 5 mA	—	—	0.5	V	1
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 2.5 mA	—	—	0.5	V	
V _{OL}	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 20 mA	—	—	0.5	V	1
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 10 mA	—	—	0.5	V	
V _{OL}	Output low voltage — RESET_B					
	2.7 V ≤ V _{DD} ≤ 3.6 V, I _{OL} = 3 mA	—	—	0.5	V	
	1.71 V ≤ V _{DD} ≤ 2.7 V, I _{OL} = 1.5 mA	—	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	μA	1, 2
	High drive port pins	—	0.004	0.5	μA	
I _{IN}	Input leakage current (total all pins) for full temperature range	—	—	1.0	μA	2
R _{PU}	Internal pullup resistors	20	—	50	kΩ	3
R _{PD}	Internal pulldown resistors	20	—	50	kΩ	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.

2. Measured at V_{DD}=3.6V

3. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}

4. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 80 MHz
- Bus clock = 40 MHz
- FlexBus clock = 20 MHz
- Flash clock = 20 MHz
- MCG mode: FEI

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V @ -40°C to 25°C	—	0.73	1.42	μA	
	@ 70°C	—	1.8	3.90	μA	
	@ 85°C	—	3.0	5.25	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	—	0.43	0.55	μA	
	@ 70°C	—	1.4	2.45	μA	
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.14	0.24	μA	
	@ 70°C	—	1.1	2.15	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	@ -40°C to 25°C	—	0.18	0.21	μA	
	@ 70°C	—	0.66	0.86	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	@ 85°C	—	1.52	2.24	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers					15
	@ 1.8V					
	• @ -40°C to 25°C	—	0.59	0.70	μA	
	• @ 70°C	—	1.00	1.3	μA	
	• @ 85°C	—	1.76	2.59	μA	
	@ 3.0V					
	• @ -40°C to 25°C	—	0.71	0.84	μA	
	• @ 70°C	—	1.22	1.59	μA	
	• @ 85°C	—	2.08	3.06	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. Cache on and prefetch on, low compiler optimization.
4. Coremark benchmark compiled using IAR 7.2 with optimization level low.
5. 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
6. 80 MHz core and system clock, 40 MHz bus clock, and 26.67 MHz flash clock. MCG configured for PEE mode. Compute operation.
7. 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.

Table 7. Low power mode peripheral adders—typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

2.2.5.1 Diagram: Typical $I_{\text{DD_RUN}}$ operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz. MCG in PEE mode at frequencies greater than 100 MHz.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

General

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: M $\leq$ 18dBmV, L $\leq$ 24dBmV, K $\leq$ 30dBmV, I $\leq$ 36dBmV, H $\leq$ 42dBmV .

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to nxp.com
- Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	—	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f _{SYS}	System and core clock	—	120	MHz	
f _{BUS}	Bus clock	—	60	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f _{SYS}	System and core clock	—	80	MHz	
f _{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f _{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	30	MHz	
f _{FLASH}	Flash clock	—	26.67	MHz	
f _{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode ¹					

Table continues on the next page...

Table 14. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 15. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG	0	10	MHz
		0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG and CJTAG	50	—	ns
		33	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

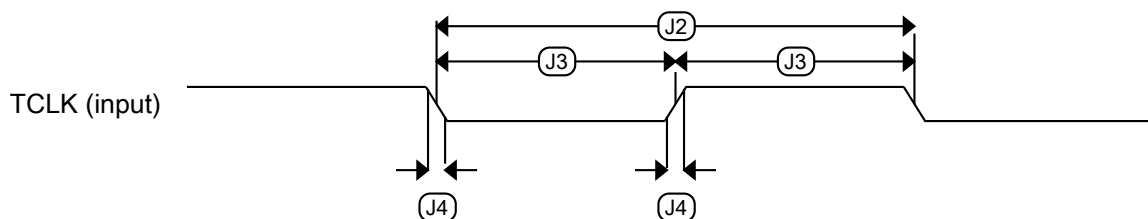
**Figure 7. Test clock input timing**

Table 16. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	—	—	kHz	
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll_ref}	80	83.89	100	MHz	
f _{dco_t_DMx3 2}	DCO output frequency	Low range (DRS=00) 732 × f _{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f _{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fll_ref}	—	95.98	—	MHz	
J _{cyc_fll}	FLL period jitter • f _{VCO} = 48 MHz • f _{VCO} = 98 MHz		— —	— 180 150	— —	ps	
t _{fll_acquire}	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f _{vco}	VCO operating frequency		48.0	—	120	MHz	
I _{pll}	PLL operating current • PLL @ 96 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	μA	8
I _{pll}	PLL operating current • PLL @ 48 MHz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	μA	8
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS) • f _{vco} = 48 MHz • f _{vco} = 100 MHz		— —	120 75	— —	ps ps	9
J _{acc_pll}	PLL accumulated jitter over 1μs (RMS)						9

Table continues on the next page...

Table 17. IRC48M specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta f_{irc48m_ol_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	— —	± 0.4 ± 0.5	± 1.0 ± 1.5	$\%f_{irc48m}$	1
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	2
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	μs	3

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma).
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
 - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1 or
 - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10 or MCG_C5[PLLCLKEN0]=1, or
 - SIM_SOPT2[PLLFLSEL]=11

3.3.3 Oscillator electrical specifications

3.3.3.1 Oscillator DC electrical specifications

Table 18. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0) • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz	— — — — — —	500 200 300 950 1.2 1.5	— — — — — —	nA μA μA μA mA mA	1
I_{DDOSC}	Supply current — high-gain mode (HGO=1) • 32 kHz	— —	25 400	— —	μA μA	1

Table continues on the next page...

3.4.2 EzPort switching specifications

Table 26. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP_CS}}$ negation to next $\overline{\text{EZP_CS}}$ assertion	$2 \times t_{\text{EZP_CK}}$	—	ns
EP3	$\overline{\text{EZP_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	25	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP_CS}}$ negation to EZP_Q tri-state	—	12	ns

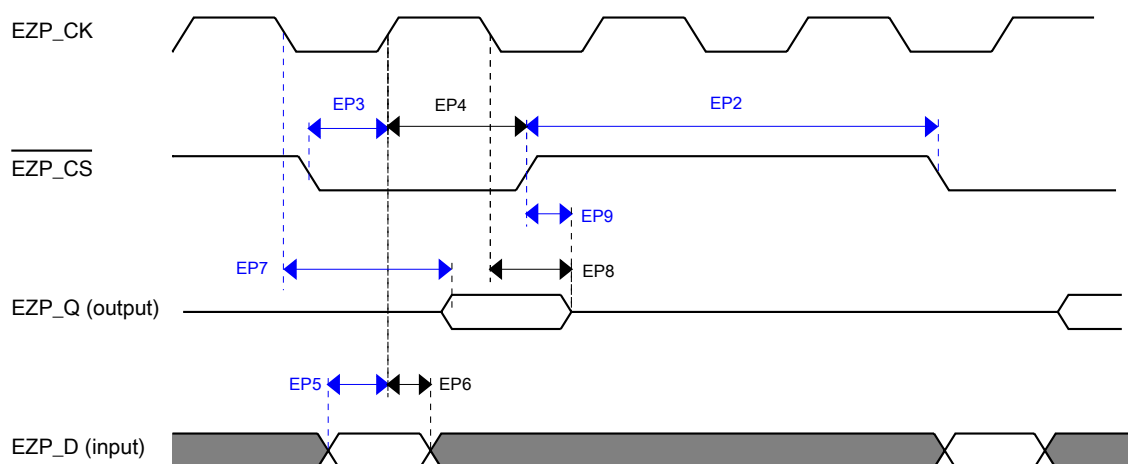


Figure 11. EzPort Timing Diagram

3.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 27. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	15	ns	
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	14.5	—	ns	
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWEn}}$, $\overline{\text{FB_CSn}}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

Table 28. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	21.5	ns	
FB3	Address, data, and control output hold	–1.0	—	ns	1
FB4	Data and $\overline{\text{FB_TA}}$ input setup	20.0	—	ns	
FB5	Data and $\overline{\text{FB_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB_BE/BWEn}}$, $\overline{\text{FB_CSn}}$, $\overline{\text{FB_OE}}$, FB_R/W, $\overline{\text{FB_TBST}}$, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB_TA}}$.

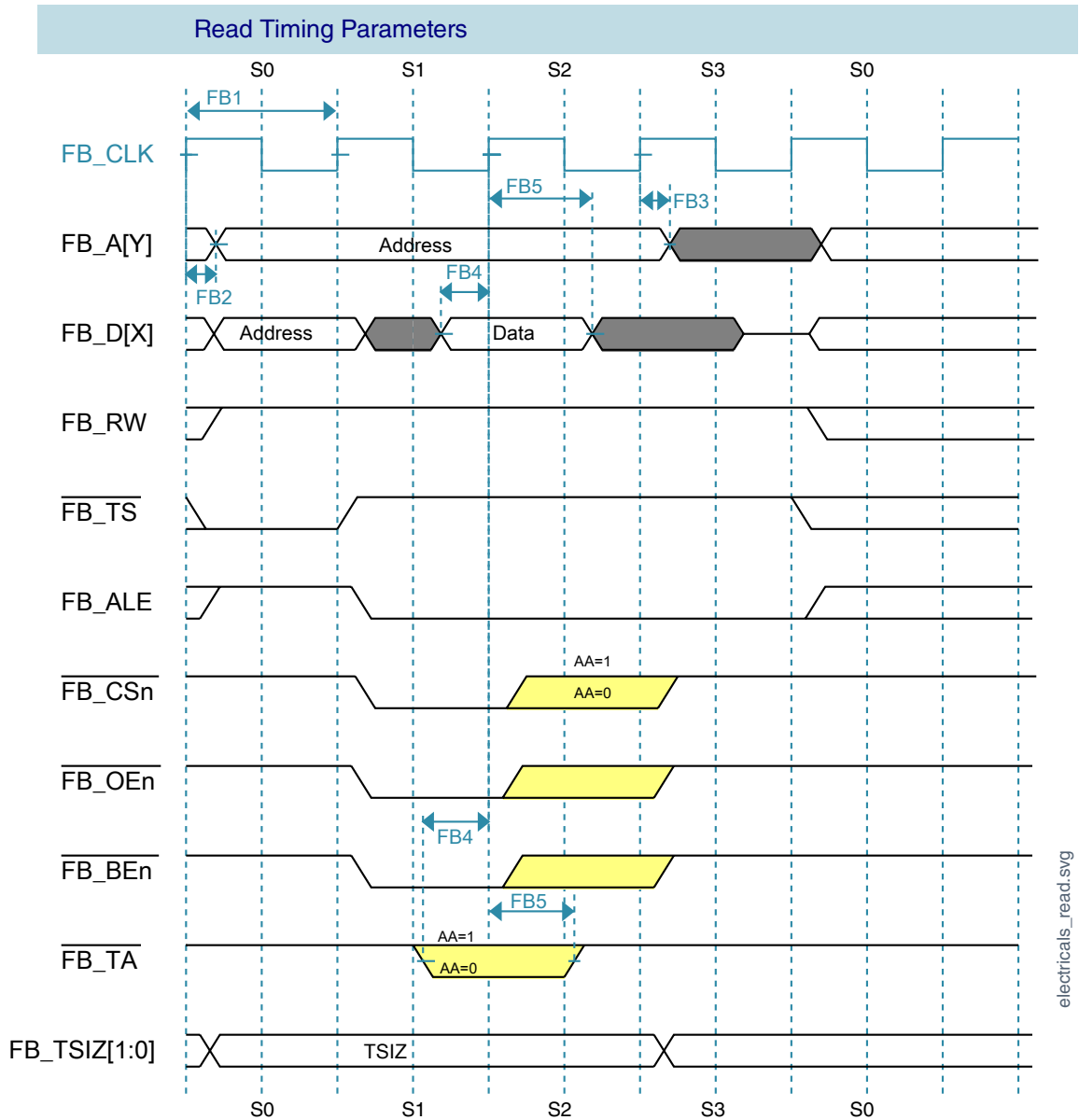


Figure 12. FlexBus read timing diagram

3.6.3.2 12-bit DAC operating behaviors

Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	1200	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2 V$	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4 V$	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
R_{op}	Output resistance (load = 3 k Ω)	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h - High power (SP_{HP}) - Low power (SP_{LP})	1.2 0.05	1.7 0.12	— —	V/ μs	
BW	3dB bandwidth - High power (SP_{HP}) - Low power (SP_{LP})	550 40	— —	— —	kHz	

- Settling within ± 1 LSB
- The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
- The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4 V$
- Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
- $V_{DDA} = 3.0 V$, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

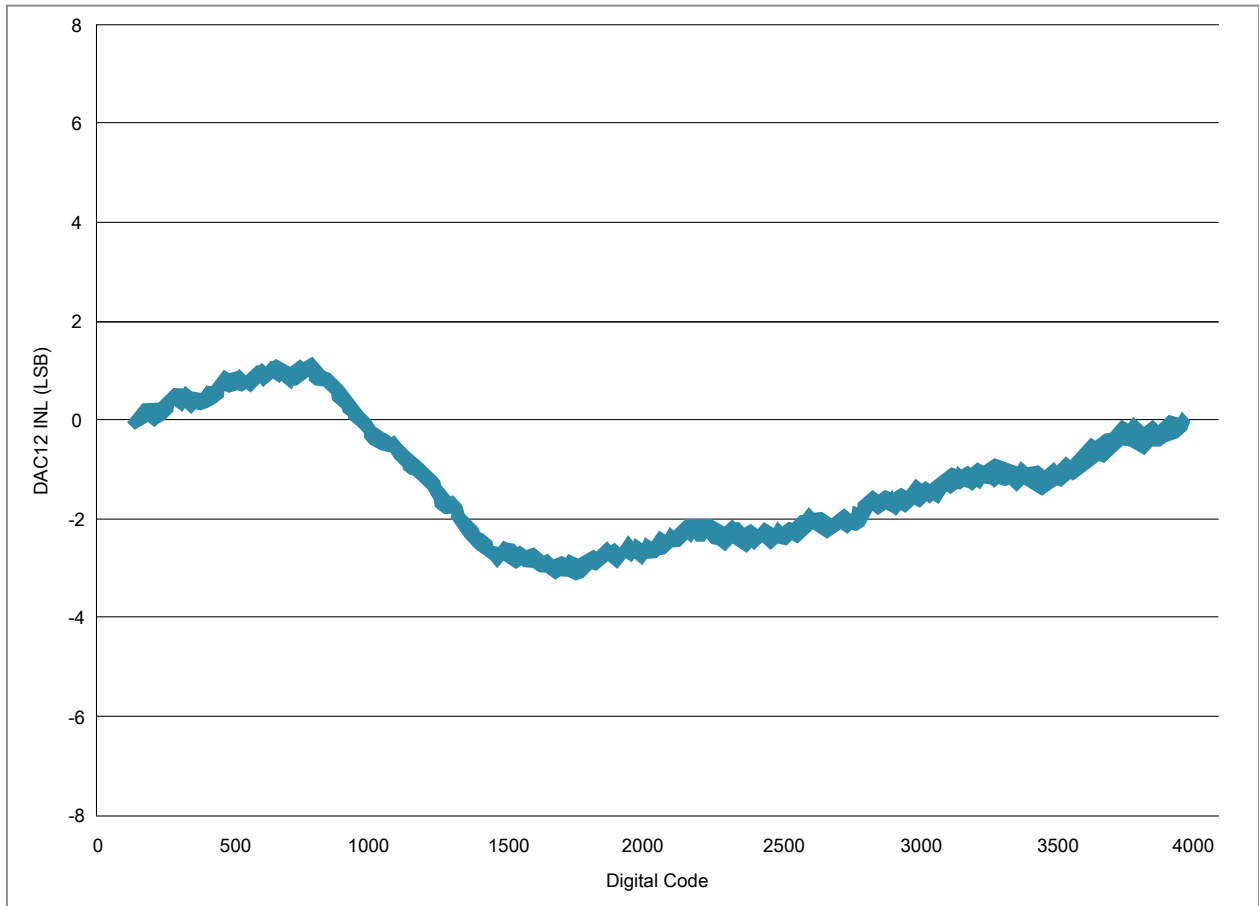


Figure 19. Typical INL error vs. digital code

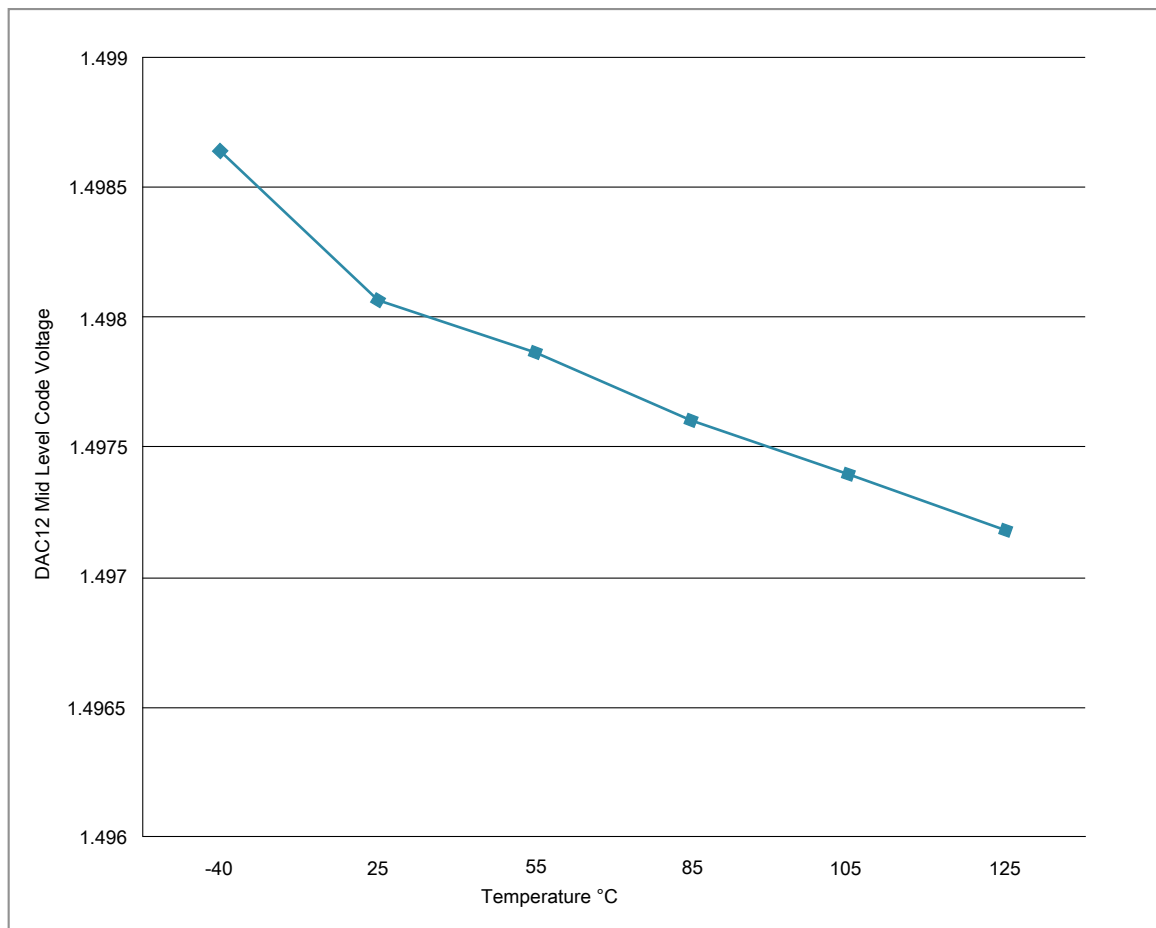


Figure 20. Offset at half scale vs. temperature

3.6.4 Voltage reference electrical specifications

Table 34. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

NOTE

The MCGPLLCLK meets the USB jitter and signaling rate specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The MCGFLLCLK does not meet the USB jitter or signaling rate specifications for certification.

The IRC48M meets the USB jitter and signaling rate specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB signaling rate specifications for certification in Host mode operation.

3.8.2 USB VREG electrical specifications

Table 38. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	μA	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I _{DDoff}	Quiescent current — Shutdown mode - VREGIN = 5.0 V and temperature=25 °C - Across operating voltage and temperature	—	650	—	nA	
		—	—	4	μA	
I _{LOADrun}	Maximum load current — Run mode	—	—	120	mA	
I _{LOADstby}	Maximum load current — Standby mode	—	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V - Run mode - Standby mode	3	3.3	3.6	V	
		2.1	2.8	3.6	V	

Table continues on the next page...

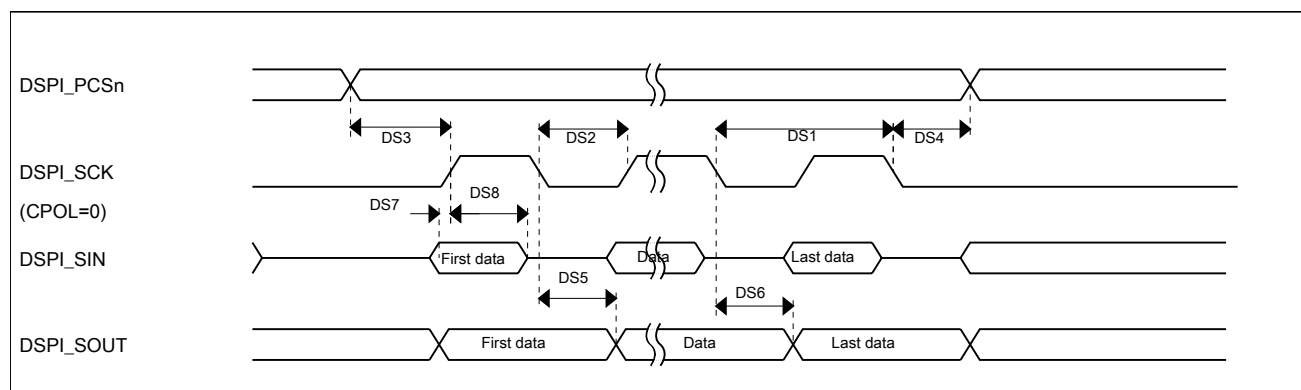


Figure 21. DSPI classic SPI timing — master mode

Table 40. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	15	MHz	1
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns	
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS13	DSPI_SS active to DSPI_SCK input setup	2.6	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns	
DS15	DSPI_SS active to DSPI_SOUT driven	—	17	ns	
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	17	ns	

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

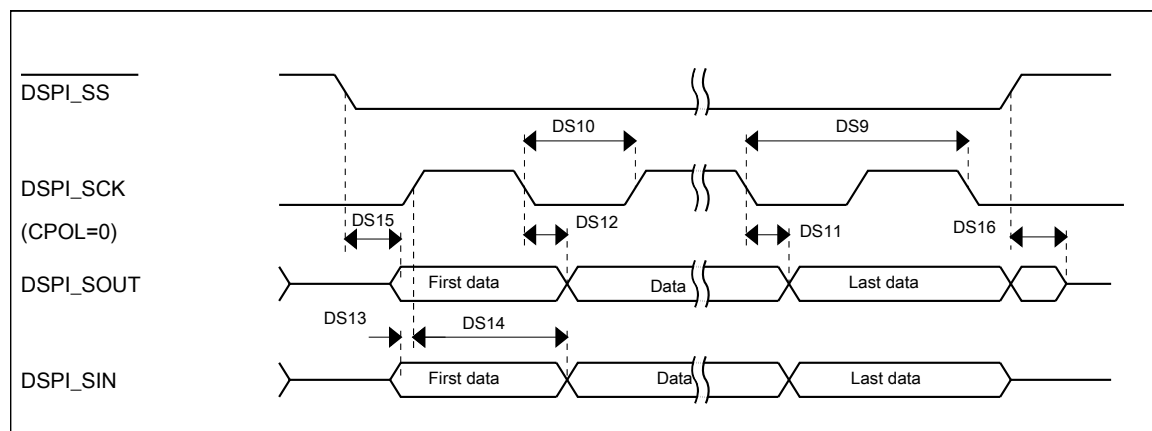
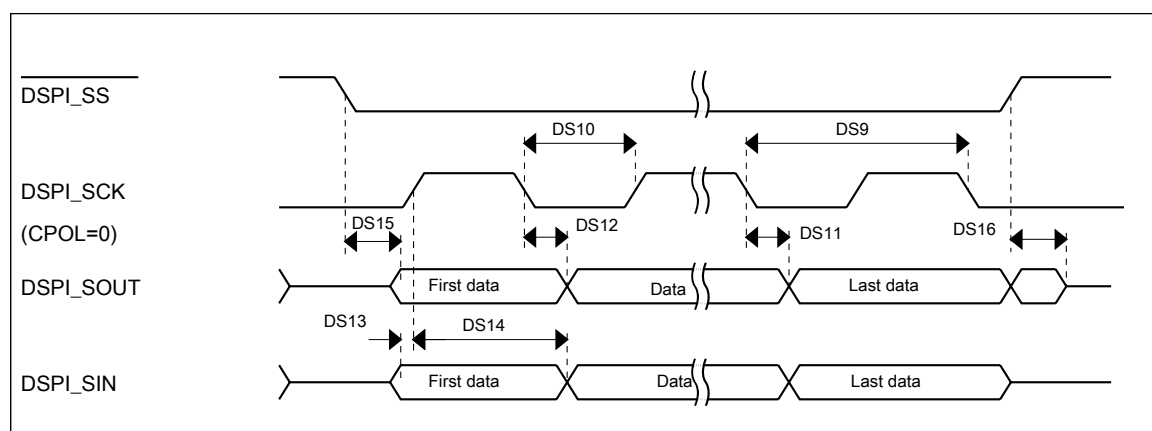


Figure 22. DSPI classic SPI timing — slave mode

Table 42. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	25	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	25	ns

**Figure 24. DSPI classic SPI timing — slave mode**

3.8.5 Inter-Integrated Circuit Interface (I²C) timing

Table 43. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400 ¹	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD} ; STA	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	t_{SU} ; STA	4.7	—	0.6	—	μs

Table continues on the next page...

Table 43. I²C timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Data hold time for I ² C bus devices	t _{HD} ; DAT	0 ²	3.45 ³	0 ⁴	0.9 ²	μs
Data set-up time	t _{SU} ; DAT	250 ⁵	—	100 ^{3, 6}	—	ns
Rise time of SDA and SCL signals	t _r	—	1000	20 + 0.1C _b ⁷	300	ns
Fall time of SDA and SCL signals	t _f	—	300	20 + 0.1C _b ⁶	300	ns
Set-up time for STOP condition	t _{SU} ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t _{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD}; DAT must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU}; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

Table 44. I²C 1 Mbps timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f _{SCL}	0	1 ¹	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD} ; STA	0.26	—	μs
LOW period of the SCL clock	t _{LOW}	0.5	—	μs
HIGH period of the SCL clock	t _{HIGH}	0.26	—	μs
Set-up time for a repeated START condition	t _{SU} ; STA	0.26	—	μs
Data hold time for I ² C bus devices	t _{HD} ; DAT	0	—	μs
Data set-up time	t _{SU} ; DAT	50	—	ns
Rise time of SDA and SCL signals	t _r	20 + 0.1C _b ²	120	ns
Fall time of SDA and SCL signals	t _f	20 + 0.1C _b ²	120	ns
Set-up time for STOP condition	t _{SU} ; STO	0.26	—	μs
Bus free time between STOP and START condition	t _{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	0	50	ns

Pinout

80 WLC SP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
G10	VREFH	VREFH	VREFH								
H10	VREFL	VREFL	VREFL								
H9	VSSA	VSSA	VSSA								
E8	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
F8	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
G7	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
G8	XTAL32	XTAL32	XTAL32								
H8	EXTAL32	EXTAL32	EXTAL32								
H7	VBAT	VBAT	VBAT								
F7	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_ CTS_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
F6	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
F5	PTA2	JTAG_TDO/ TRACE_ SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
F4	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_ RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
G6	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
H5	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2			I2S0_TX_ BCLK	JTAG_TRST_ b	
H6	PTA12	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
H4	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
G5	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK		
G4	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
H3	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_ CTS_b			I2S0_RX_FS		
G3	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_MCLK		
E6	VDD	VDD	VDD								
G2	VSS	VSS	VSS								
H2	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				

Part identification

	1	2	3	4	5	6	7	8	9	10	
A	PTC4/ LLWU_P8	PTC6/ LLWU_P10	PTC8	PTC11/ LLWU_P11	PTC17	PTD2/ LLWU_P13	PTD5	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTE3	A
B	PTC1/ LLWU_P6	PTC5/ LLWU_P9	PTC7	PTC10	PTC16	PTD1	PTD4/ LLWU_P14	PTE4/ LLWU_P2	VDD	VSS	B
C	PTC0	PTC2	PTC3/ LLWU_P7	PTC9	PTD0/ LLWU_P12	PTD3	PTD6/ LLWU_P15	PTE5	VOUT33	USB0_DP	C
D	PTB16	PTB17	PTB18	PTB19	VDD	VDD	PTD7	VSS	VREGIN	USB0_DM	D
E	PTB11	PTB10	PTB1	VSS	VSS	VDD	PTE0/ CLKOUT32K	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	ADC0_DP0/ ADC1_DP3	ADC1_DP1/ ADC0_DP2	E
F	PTB3	PTB2	PTB0/ LLWU_P5	PTA3	PTA2	PTA1	PTA0	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	ADC0_DM0/ ADC1_DM3	ADC1_DM1/ ADC0_DM2	F
G	RESET_b	VSS	PTA17	PTA15	PTA14	PTA4/ LLWU_P3	RTC_ WAKEUP_B	XTAL32	VDDA	VREFH	G
H	PTA19	PTA18	PTA16	PTA13/ LLWU_P4	PTA5	PTA12	VBAT	EXTAL32	VSSA	VREFL	H

Figure 32. K22F 80 WLCSP pinout diagram (transparent top view)

6 Part identification

6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

6.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N