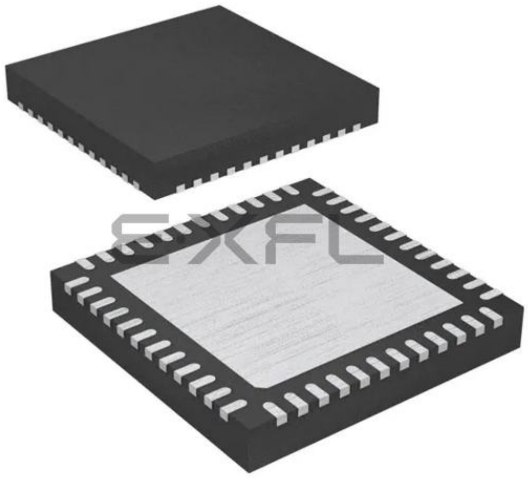

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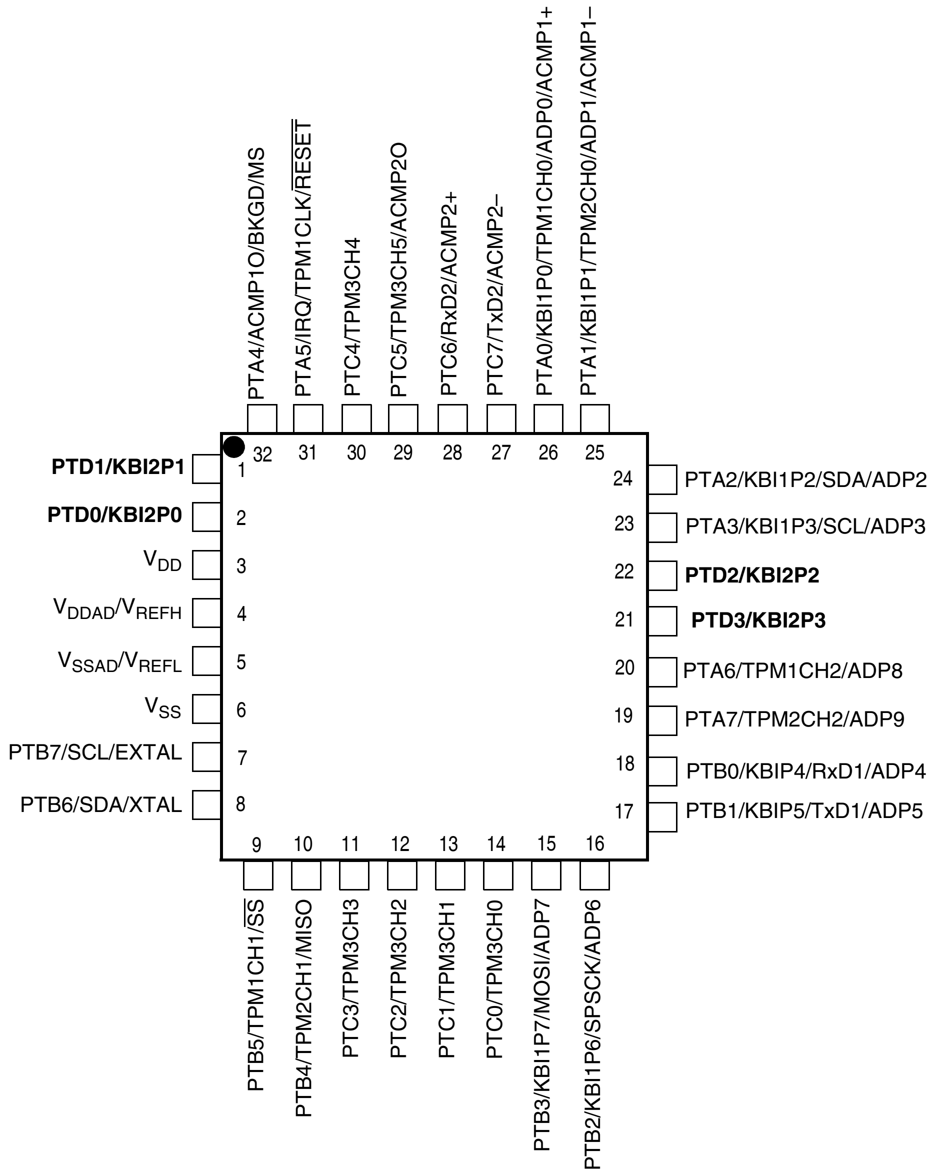
Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	50MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe16cft



Pins in **bold** are lost in the next lower pin count package.

Figure 4. 32-Pin LQFP/QFN

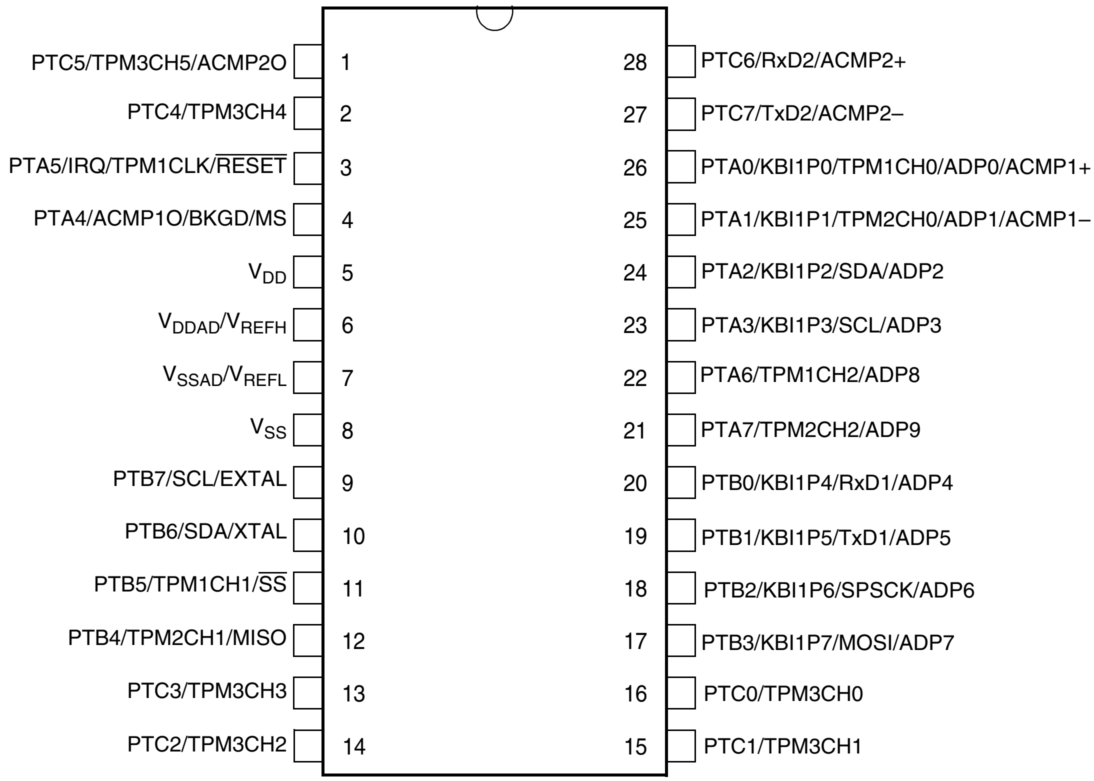


Figure 5. 28-Pin SOIC

Table 1. MC9S08QE32 Series Pin Assignment by Package and Pin Sharing Priority

Pin Number				<-- Lowest	Priority	--> Highest		
48	**44**	**32**	**28**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	—	PTD1	KBI2P1			
2	2	2	—	PTD0	KBI2P0			
3	3	—	—	PTE7	TPM3CLK			
4	4	3	5					V_{DD}
5	5	4	6					V_{DDAD}
6	6							V_{REFH}
7	7	5	7					V_{REFL}
8	8							V_{SSAD}
9	9	6	8					V_{SS}
10	10	7	9	PTB7	SCL[1]			EXTAL
11	11	8	10	PTB6	SDA[1]			XTAL
12	—	—	—	PTE6				
13	—	—	—	PTE5				
14	12	9	11	PTB5	TPM1CH1	SS[2]		
15	13	10	12	PTB4	TPM2CH1	MISO[2]		
16	14	11	13	PTC3	TPM3CH3			
17	15	12	14	PTC2	TPM3CH2			
18	16	—	—	PTD7	KBI2P7			

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE32 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	±100	—	mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typical[1]	Max	Unit
16	D	POR re-arm time	t_{POR}		10	—	—	μs
17	P	Low-voltage detection threshold — high range	V_{LVDH}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
18	P	Low-voltage detection threshold — low range	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.88	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis	V_{hys}		—	80	—	mV
22	P	Bandgap Voltage Reference[7]	V_{BG}		1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

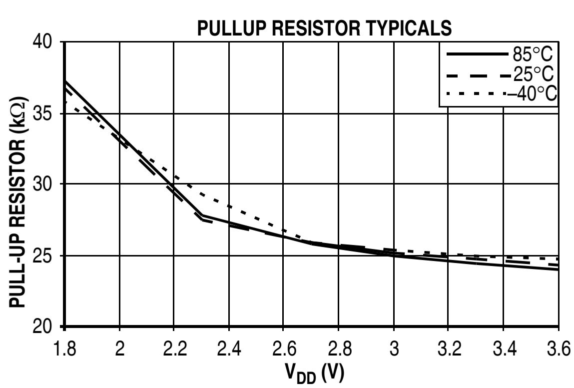
3 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C



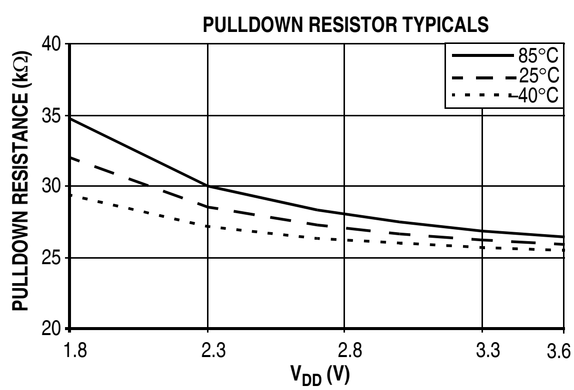


Figure 6. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

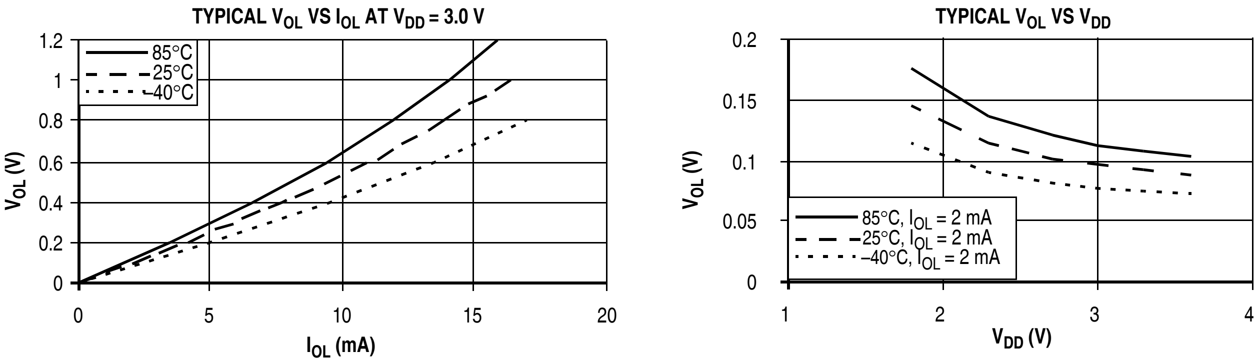


Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

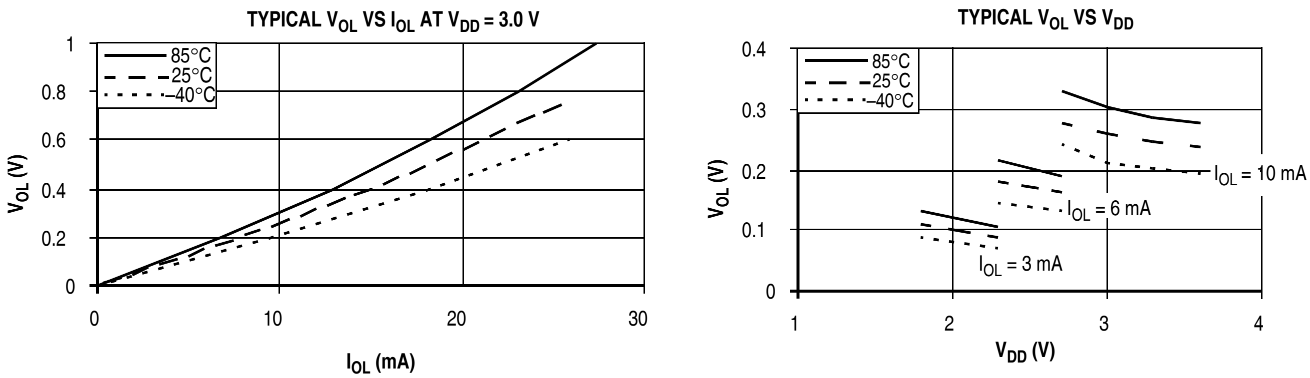


Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

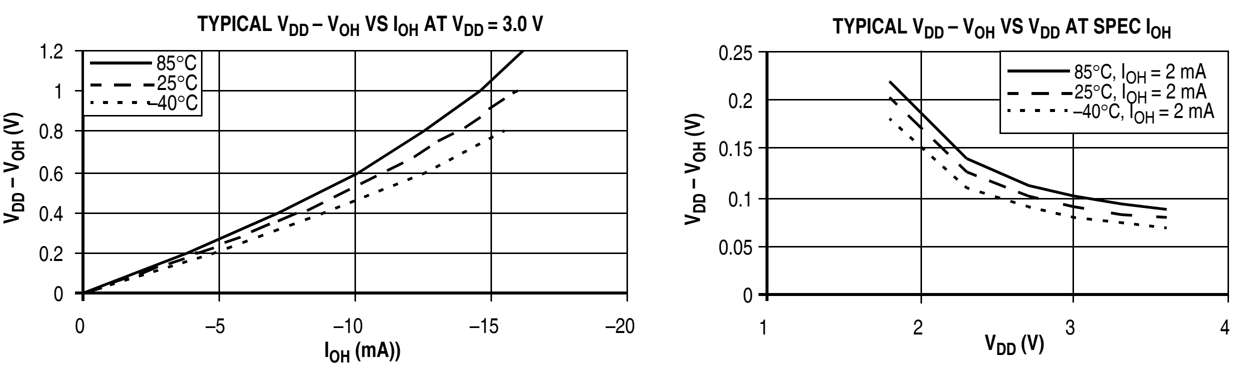


Figure 9. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

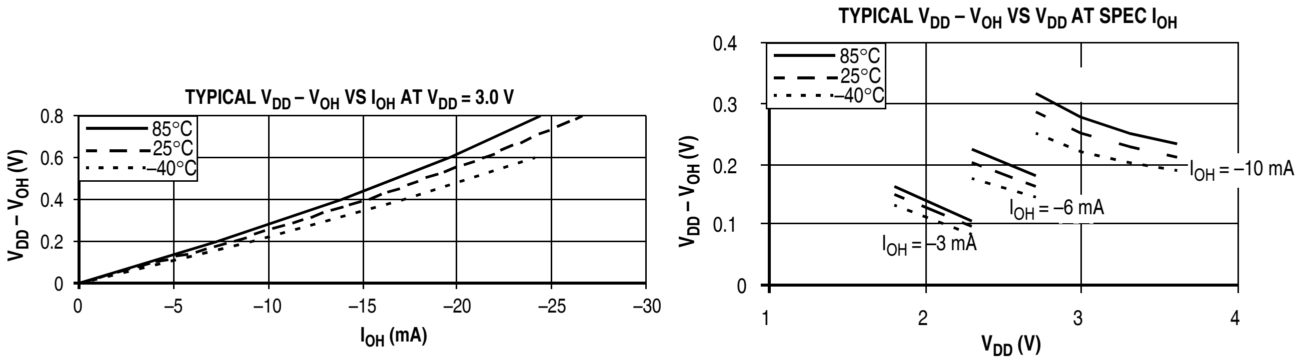


Figure 10. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 8. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25.165 MHz	3	13	14	mA	–40 to 25
	P					14	15		85
	T			20 MHz		13.75	—		–40 to 85
	T			8 MHz		5.59	—		
	T			1 MHz		1.03	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25.165 MHz	3	11.5	12.3	mA	–40 to 85
	T			20 MHz		9.5	—		
	T			8 MHz		4.6	—		
	T			1 MHz		1.0	—		
3	T	Run supply current LPRS = 0, all modules off	RI_{DD}	16 kHz FBILP	3	152	—	µA	–40 to 85
	T			16 kHz FBELP		115	—		
4	T	Run supply current LPRS = 1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3	21.9	—	µA	–40 to 85
	T	Run supply current LPRS = 1, all modules off, running from RAM				7.3	—		
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25.165 MHz	3	5.74	6.00	mA	--40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		

Table 8. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
6	P	Stop2 mode supply current		$S2I_{DD}$	—	3	0.35	0.65	µA	–40 to 25C
	C				—		0.8	1.0		70
	P				—		2.0	4.5		85
	C				—	2	0.25	0.50		–40 to 25
	C				—		0.65	0.85		70
	C				—		1.5	3.5		85
7	P	Stop3 mode supply current no clocks active		$S3I_{DD}$	—	3	0.45	1.00	µA	–40 to 25
	C				—		1.5	2.3		70
	P				—		4	8		85
	C				—	2	0.35	0.70		–40 to 25
	C				—		1	2		70
	C				—		3.5	6.0		85
8	T	Low power mode adders:	EREFSTEN=1		32 kHz	3	500	—	nA	–40 to 85
9	T		IREFSTEN=1		32 kHz		70	—	µA	
10	T		TPM PWM		100 Hz		12	—	µA	
11	T		SCI, SPI, or IIC		300 bps		15	—	µA	
12	T		RTC using LPO		1 kHz		200	—	nA	
13	T		RTC using ICSERCLK		32 kHz		1	—	µA	
14	T		LVD		n/a		100	—	µA	
15	T		ACMP		n/a		20	—	µA	

[1] Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

Table 9. Stop Mode Adders

Num	C	Parameter	Condition	Temperature				Units
				–40°C	**25**°C	**70**°C	**85**°C	
1	T	LPO	—	50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN[1]	—	63	70	77	81	µA
4	T	RTC	Does not include clock source current	50	75	100	150	nA
5	T	LVD[1]	LVDSE = 1	90	100	110	115	µA
6	T	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	22	23	µA
7	T	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	95	106	114	120	µA

1 Not available in stop2 mode.

3.8 External Oscillator (XOSCVLP) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1 C_2	See Note [2] See Note [3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 100 0 0 0 0	 — — — 0 10 20	kΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	t_{CSTL} t_{CSTH}	 — — — —	 200 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	 0.03125 0	 — —	 40 40	 MHz MHz

1 Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.
2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.
3 See crystal or resonator manufacturer's recommendation.
4 Proper PC board layout procedures must be followed to achieve specifications.

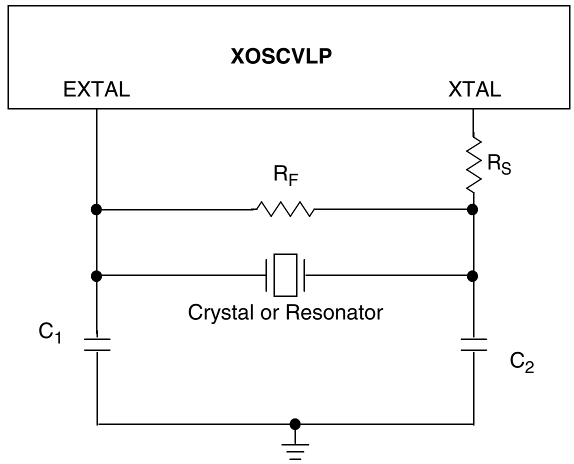


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

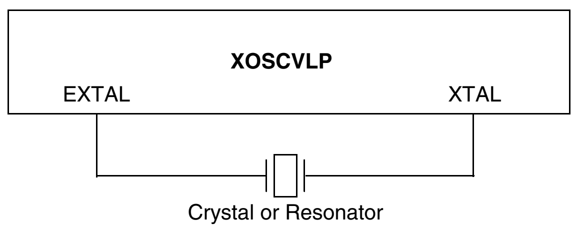


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed		f_{int_t}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	5	10	μs
4	P	DCO output frequency trimmed[2]	Low range (DFR = 00)	f_{dco_u}	16	—	20	MHz
	P		Mid range (DFR = 01)		32	—	40	
	P		High range (DFR = 10)		48	—	60	
5	P	DCO output frequency[2] reference = 32768 Hz and DMX32 = 1	Low range (DFR = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DFR = 01)		—	39.85	—	
	P		High range (DFR = 10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C	Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column is characterized at 3.0 V, 25 °C or is typical recommended value.
2 The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.
3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$) $V_{DD} \leq 2.1V$ $2.1 < V_{DD} \leq 2.4V$ $V_{DD} > 2.4Vs$	f_{Bus}	DC	—	10 20 25.165	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns

Table 12. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[5]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	8 31	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	7 24	— —	ns
10	C	Voltage regulator recovery time	t_{VRR}	—	4	—	μs

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 To enter BDM mode following a POR, BKGD/MS must be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

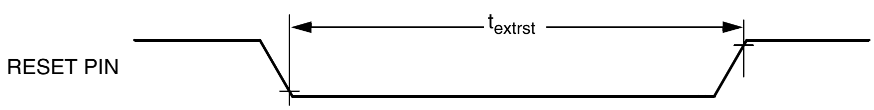


Figure 13. Reset Timing

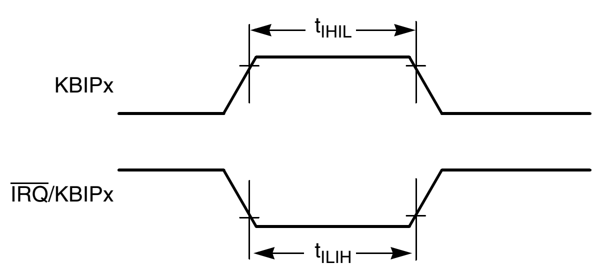


Figure 14. $\overline{IRQ}$/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

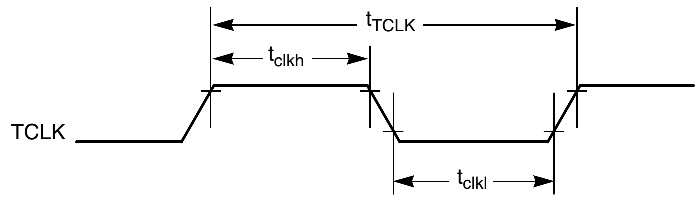


Figure 15. Timer External Clock

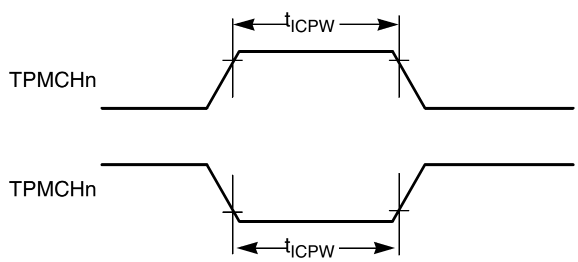


Figure 16. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 14 and Figure 17 through Figure 20 describe the timing requirements for the SPI system.

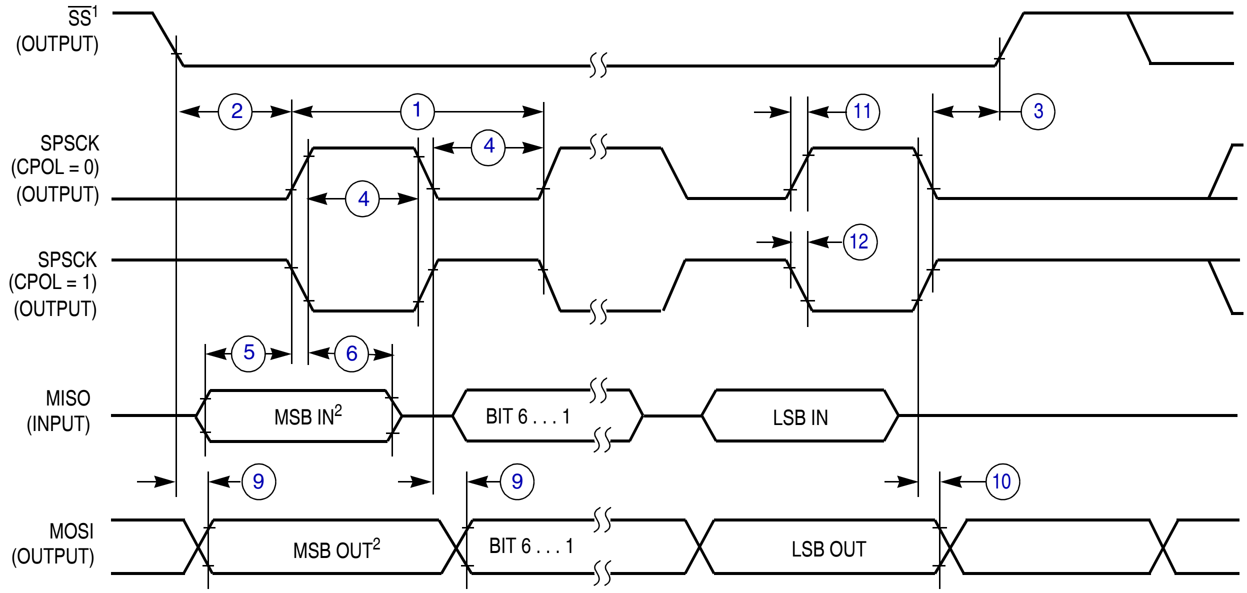
Table 14. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$[1] $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}

Table 14. SPI Timing (continued)

No.	C	Function	Symbol	Min	Max	Unit
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} – 30$ $t_{cyc} – 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} – 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} – 25$ 25	ns ns

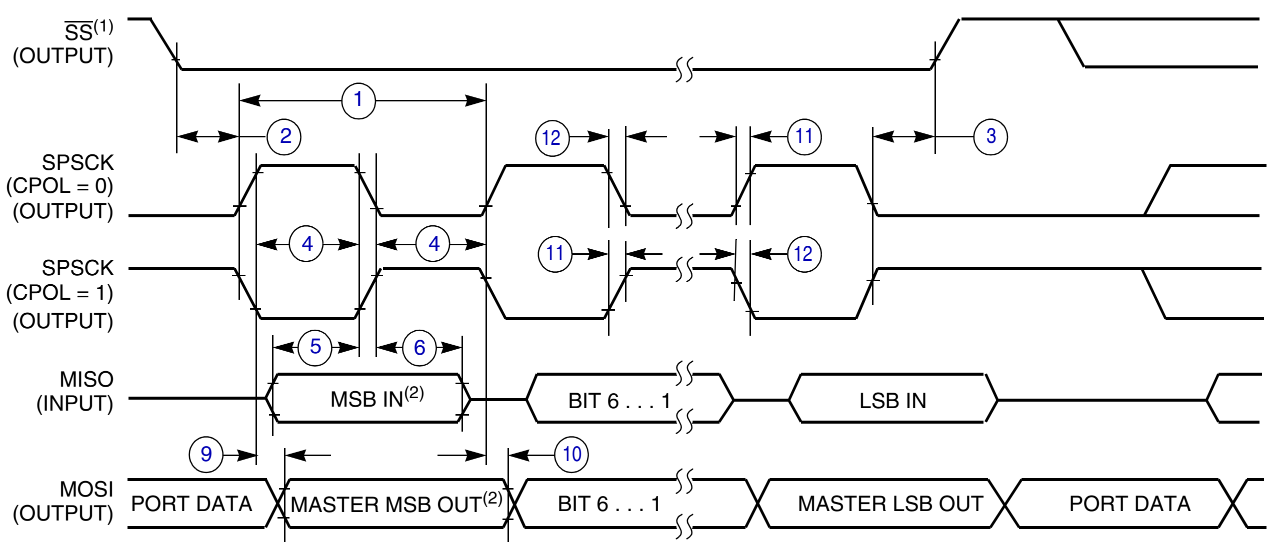
[1] Max operating frequency limited to 8 MHz when input filter disabled and high output drive strength enabled. Max operating frequency limited to 5 MHz when input filter enabled and high output drive strength disabled.



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

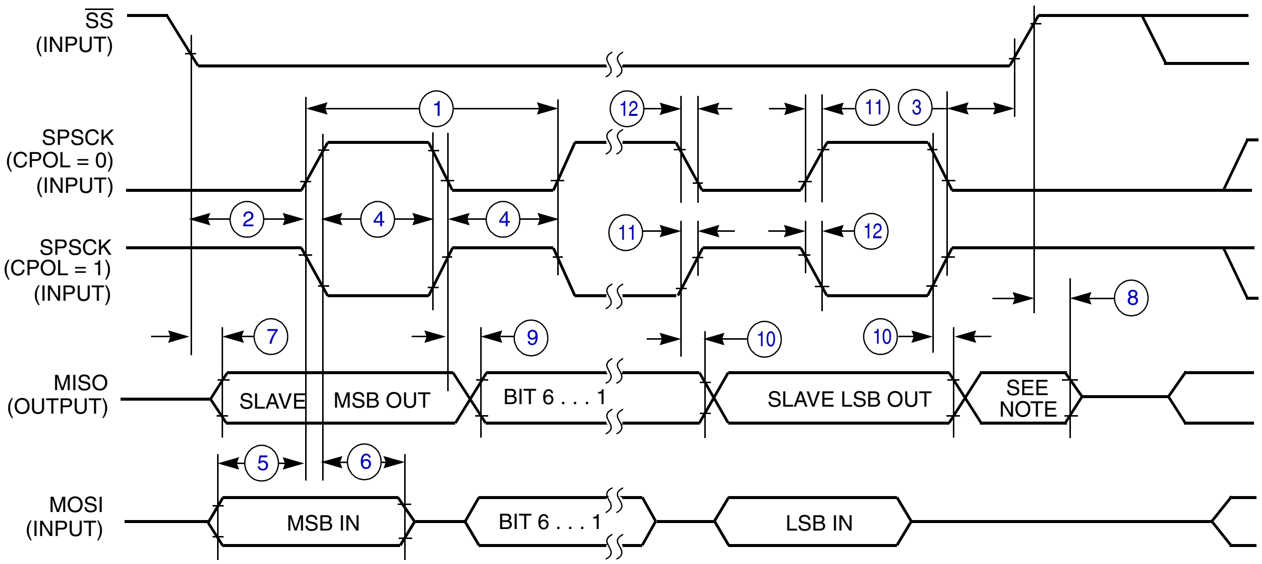
Figure 17. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

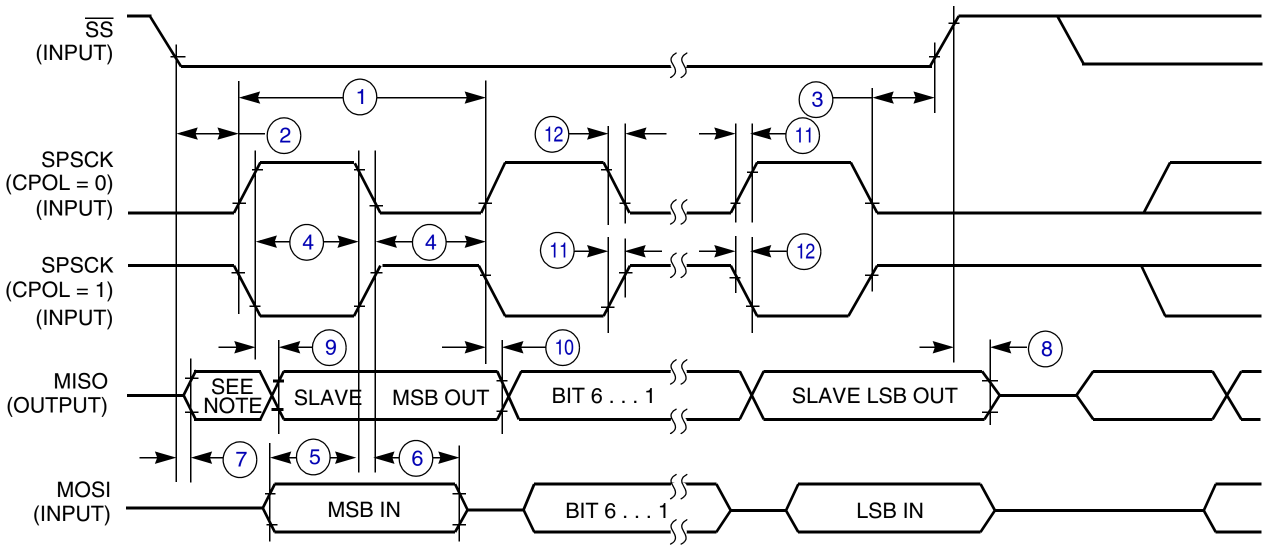
Figure 18. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 19. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 20. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	μA
D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
P	Analog input offset voltage	V_{AIO}	—	20	40	mV
C	Analog comparator hysteresis	V_H	3.0	9.0	15.0	mV
P	Analog input leakage current	I_{ALKG}	—	—	1.0	μA
C	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	μs

3.12 ADC Characteristics

Table 16. 12-Bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	—
		Delta to V_{DD} (V_{DD} – V_{DDAD})[2]	ΔV_{DDAD}	–100	0	100	mV	—
D	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSAD})[2]	ΔV_{SSAD}	–100	0	100	mV	—
D	Input voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
C	Input capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
C	Input resistance	—	R_{ADIN}	—	5	7	kΩ	—
C	Analog source resistance	12-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
		10-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz		— —	— —	5 10		
		8-bit mode (all valid f_{ADCK})		—	—	10		
D	ADC conversion clock freq.	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
		Low power (ADLPC = 1)		0.4	—	4.0		

[1] Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

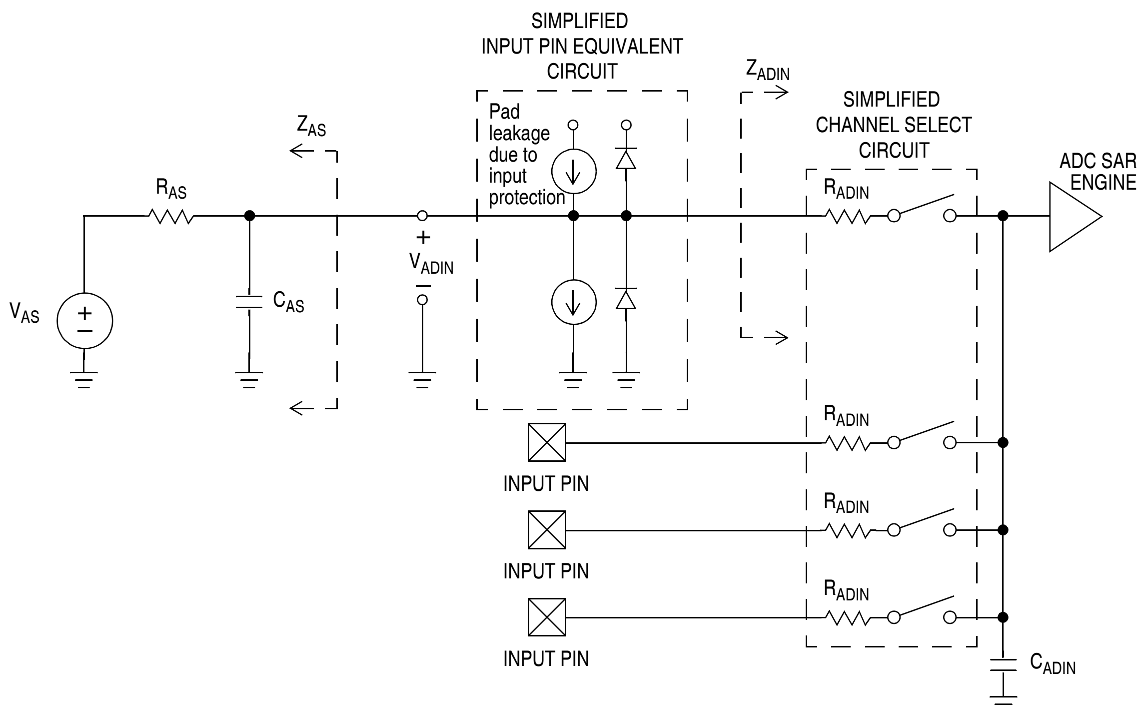


Figure 21. ADC Input Impedance Equivalency Diagram

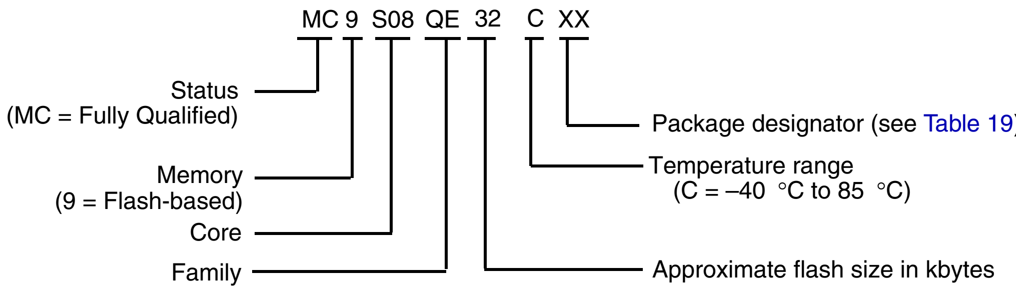
Table 17. ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	120	—	µA	
T	Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	202	—	µA	
T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDAD}	—	288	—	µA	
P	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDAD}	—	0.532	1	mA	
P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
		Low power (ADLPC = 1)		1.25	2	3.3		

4 Ordering Information

This section contains ordering information for the MC9S08QE32 series of MCUs.

Example of the device numbering system:



5 Package Information

Table 19. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
48	Quad Flat No-Leads	QFN	FT	1314	98ARH99048A
44	Low Quad Flat Package	LQFP	LD	824D	98ASS23225W
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A
32	Quad Flat No-Leads	QFN	FM	1582	98ARE10566D
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B

5.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 19. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.